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Algebraic Modeling of New Enhanced Linearity Threshold Comparator based Flash ADC

Prachi Palsodkar[1], Dr. P.K. Dakhole[2]
[1] *Research Scholar, Dept. of Electronics Engineering, Yeshwantrao Chavan College of Engineering, Nagpur, India*
[2]*Professor, Dept. of Electronics Engineering, Yeshwantrao Chavan College of Engineering, Nagpur, India*

Abstract: *This paper describes flash ADC design using linearity improved threshold quantized comparator. Here, the need for a reference voltage generation network has been eliminated in a 4 bit flash ADC; with completely digital cell based comparators. Output generated from comparator called thermometer code is related mathematically with binary conversion. This conversion property is used for mathematical modeling and complexity reduction of decoder circuitry by semi-parallel structuring of comparators. Circuit is designed in 250nm technology and it exhibits satisfactory performance even in temperature and process variation.*
Keywords: *Flash ADC, threshold, thermometer code, multiplexer, encoder, algebraic*

I. Introduction

In the real world, most data is characterized by analog signals. In order to manipulate the data using processor, we need to convert the analog signals to the digital signals. For conversion of ADC into digital domain, interfacing between the domains is needed. Such components design needs certain level of expertise and requires analog signal components which results into non-functional designs. To reduce the required design time and the risk of having non functional designs, it is therefore interesting to investigate ways to migrate these designs into more digital form by using standard-cells [1].

Threshold inverter Quantized (TIQ) comparator proposed in literature [1] [2] [3] eliminates the need of reference generating resistive ladder and analog comparators circuit. But the limitation of TIQ comparator is, it needs feature size variation for generating different reference voltage. In addition to that it generates non linear reference voltage if reference selection is not proper. In this paper, different standard cell based designs are discussed in terms of their linearity. This design is independent of process variation and no need to change feature size for reference variation.

In conventional Flash ADC number of comparator required are $(2^N -1)$ where N is the resolution i.e. comparator increases exponentially with increase in resolution. Thermometer code generated by comparator also increases exponentially with increase in resolution which leads to increase in complexity of thermometer to binary encoder circuit. Here thermometer to binary conversion is related mathematically using algebraic division theorem and remodeled the comparator assembly in semi parallel fashion. Thus algebraic model reduces complexity of comparator by divide and conquer approach.

II. Digital Comparator Design

Flash converters include 2^N-1 comparators for N-bit resolution and have the advantage of having a very high sampling frequency. However, this structure occupies a large area and consumes a large amount of power when its resolution becomes high. This is not desirable for low power applications [5] [6]. To improve the design of flash type converters, several architectures have been proposed such as the two-stage architecture [7] [8], the folding and averaging converters [9, 10]. The major issue with these approaches is that it uses analog components that are difficult to integrate and whose performances are degraded as technology scales down. Furthermore, these ADCs need high gain differential comparators that are inherently more complex and require a resistor ladder circuit to deliver reference voltages. Other disadvantages of this approach are the reduction in throughput and poor differential linearity. Recently, some authors have proposed simple and faster flash converters based on the TIQ technique (Threshold Inverter Quantization) [1][2][3][11][12][13]. Although this technique reduces the complexity of the converter, it is sensitive to process variation and consumes considerable power. Feature size variation is the basic design methodology of TIQ flash ADC which leads to non linear transfer characteristics. Thus nonlinear reference voltage is available for comparison which generates nonlinear DNL and INL. In order to overcome overheads of traditional analog design and to retain digital design strategy a new approach is proposed in next section.

III Methodology of Comparator Design

In this section three designs are discussed, which are inverters based comparator. Inverter is constructed from inverter, NAND and NOR cells. In design I basic principle of standard cell based comparator assembly is discussed. Due to non linearity limitation design (I) is modified as design (II). Design (II) provides linear characteristics but reference voltage range is small. Again, design (I) and design (II) assembly re-modified by summarising their pros and cons as design (III) which is more linear than design (I) and provides greater reference span than design (II).

3.1 Design I of basic Standard cell based comparator for 4 bit flash ADC [14]

Design (I) assembly is shown in Figure 1. This design consists of parallel combination of inverter and inverters designed from NAND and NOR cells of CMOS gates. Flash ADC generates output by comparing input signal with internal threshold of each comparator. The input of all gates are connected together and given a common input (Vin). In this Design feature size variation is not required due to device property. Reference voltage generation principle is explained in section below.

Working principle [14]:

For CMOS, threshold of a gate is the input voltage that generates an output of $V_{DD}/2$, it is mandatory that all PMOS and NMOS be conducting. This condition is satisfied when:

$$V_{TH} < V_G < V_{DD} - V_{TH} \quad (1)$$

In addition, we know that the NMOS will be in saturation when $V_{DS} > V_{GS} - V_{TH}$. Since V_{DS} is equal to $V_{DD}/2$ at the threshold voltage, V_{GS} needs to be smaller than $V_{DD}/2 + V_{TH}$ for the transistor to be in saturation. Similarly, the PMOS is in saturation when V_{SD} is greater than $V_{SG}-V_{TH}$. Since V_{SD} is equal to $V_{DD}/2$ at the threshold voltage, the PMOS is in saturation when $V_{DD}/2 > V_{DD} - V_G - V_{TH}$. Thus, both networks will be in saturation if the following condition is satisfied:

$$(V_{DD}/2)-V_{TH} < V_G < (V_{DD}/2) + V_{TH} \quad (2)$$

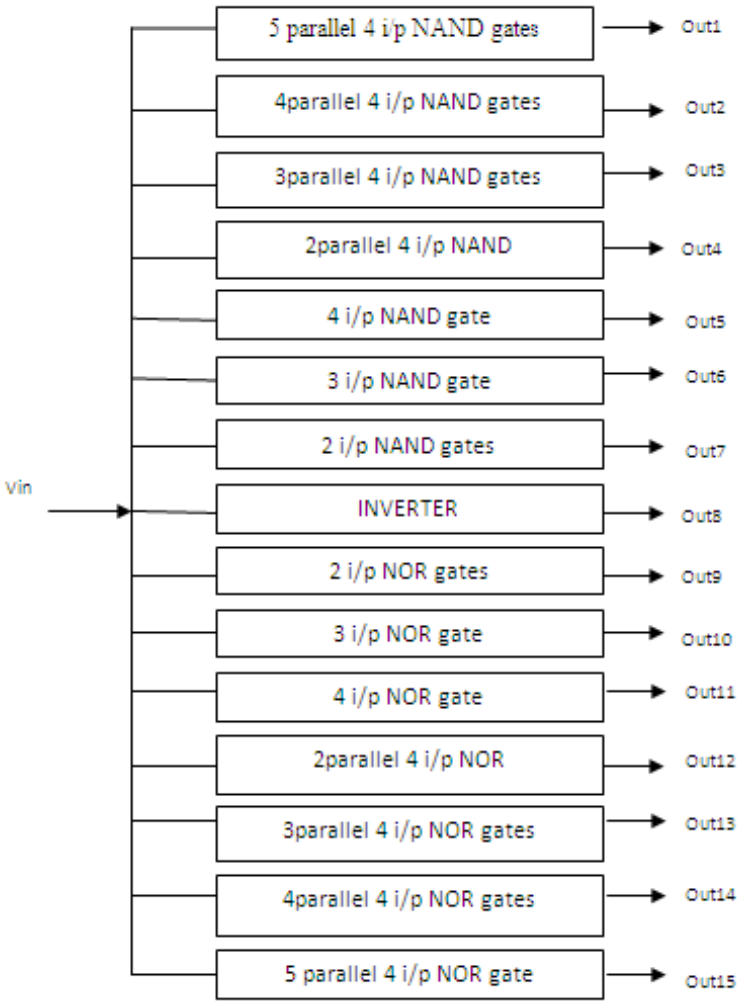

Figure 1: Design I comparator structure for 4 bit ADC

It can be shown that when $(V_{DD}/2)<2\ V_{TH}$, both conditions in Equations (1) and (2) will be simultaneously satisfied. In this case, it means that at the threshold voltage of the gate, all transistors will be in saturation. Since the region of operation of these transistors is saturation and their current is equal, it is possible to write the following equation for NAND gate:

$$(M)(1/2)\mu C_{ox}\,(W/L)\,(V_{GS} - V_{TH})^2 = (1/M)\,(1/2)\,\mu C_{ox}\,(W/L)\,(V_{SG} - V_{TH})^2 \quad (3)$$

Above equation shows modeling for NAND gate, Where M is the number of transistors in parallel. For Series M is inverted.

When Equation (3) is solved for V_{th}, the threshold voltage of the gate (known as V_{GTH}) is obtained:

$$Vth(NAND) = (V_{DD} - V_{TH} + M.V_{TH})/\,(M + 1) \quad (4)$$

Equation (4) shows how the threshold voltage of a gate changes as a function of M. Thus NAND have higher threshold and NOR have lower threshold than Inverter. Again, by using NAND and NOR gates with higher fan-ins, the value of M changes which, in turn, changes the threshold voltage of the gate. It is therefore possible to create a set of inverters having different threshold voltages to create a flash ADC using only standard cells. This basic principle of different threshold generation is used in design I as shown in figure 1.

3.2 Design II of improved linearity comparator for 4 bit flash ADC

In design I, comparator has different threshold voltage but it varies nonlinearly. In addition to that increase in fan in beyond four is not feasible, thus parallel combination of gate is used which creates overlapped references. To improve linearity in reference selection combination of NOR and INVERTER is chosen to design a comparator. Four input NOR parallel combination is chosen thus threshold of comparator will vary depending upon equation (5) of NOR threshold and linearly changing inverter combination. Thus designed circuit gives highly linear reference selection as shown in Fig. 4 and Fig.5. In this Design hardware complexity is (2^N-1) inverters needed in each comparator .Thus total hardware complexity of comparator is $(2^N-1)^2$Inverters. Since complete design is by using standard cells, independent of process variation and feature size change, hence its complexity is tolerable.

$$Vth(NOR) = [V_{DD}\text{-}Vth+(1/M)\ Vth] / [(1/M) + 1] \quad (5)$$

Design II Comparator Assembly for 4 bit ADC:

Comparator 1: Parallel combination of 15 NOR cells
Comparator 2: 14 NOR cells and 1 inverter
Comparator 3: 13 NOR cells and 2 inverters
Comparator 4: 12 NOR cells and 3 inverters
Comparator 5: 11 NOR cells and 4 inverters
Comparator 6: 10 NOR cells and 5 inverters
Comparator 7:9 NOR cells and 6 inverters
Comparator 8: 8 NOR cells and 7 inverters
Comparator 9: 7 NOR cells and 8 inverters
Comparator 10: 6 NOR cells and 9 inverters
Comparator 11: 5 NOR cells and 10 inverters
Comparator 12: 4 NOR cells and 11 inverters
Comparator 13: 3 NOR cells and 12 inverters
Comparator 14: 2 NOR cells and 13 inverters
Comparator 15:1NOR cells and 14 inverters
Comparator 16: 15 inverters

All comparators are connected with the common input same as Design I assembly.

3.3 Design III NAND NOR cell comparator

In design III every inverter is replaced by a NAND cell as shown in Figure 2. It increases threshold voltage span. Thus this assembly provides linearity with wide range reference span.

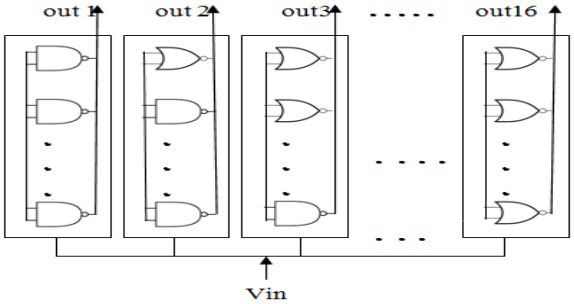

Figure 2: NAND NOR Cell comparator [14]

The threshold voltage of each gate serves as a reference voltage. We define the threshold as the input voltage at which the output voltage is $V_{DD}/2$. The comparators with a threshold voltage above the input value will output '0' whereas the ones with lower threshold voltages will output '1' [15]. This is what generates the thermometer code output.

IV. Algebraic Modelling of Flash ADC using semi parallel structure of comparators

4.1 Mathematical Model

Bit resolution increases decoder complexity exponentially. In order to reduce decoder complexity folding based Algebraic model is used. This technique utilizes basic algebra division theorem for bit partitioning. In this technique comparators are separated in two sets. One set is used to generate MSB's and other set is used to generate LSB's. Transistor level converted mathematical model uses hardware sharing. Decoder sharing is used among the LSB comparators.

Mathematical modeling for comparator partitioning [16]

Let's consider N number of bits or resolution, I is an integer value and its value is ranging from $0 \le z \le 2^N$-1
Then according to algebraic remainder theorem

$$D = (d \times q) + r \tag{6}$$

Where D -divident
d -divisior
q -quotient
r -remainder

Binary to decimal conversion is given by

$$I = b_0 2^0 + b_1 2^1 + - - - - - + b_{N-1} 2^{N-1} \tag{7}$$

Remodify equation (7) in the form of equation (6), it gives

$$I = b_0 2^0 + b_1 2^1 + - - + b_{x-1} 2^{x-1} + 2^x (b_x 2^0 + b_{x+1} 2^1 + - - + b_{N-1} 2^{N-1}) \tag{8}$$

Where, x is the partitioning factor

Now, Equation (8) can be written as

$$I = V_{LSB}(I) + 2^x \times V_{MSB}(I) \tag{9}$$

Where $V_{LSB}(I)$ is $b_0 2^0 + b_1 2^1 + - - + b_{x-1} 2^{x-1} = r$

$V_{MSB}(I)$ is $b_x 2^0 + b_{x+1} 2^1 + - - + b_{N-1} 2^{N-1} = q$

Consider an example I = 13 and $0 \le z \le 2^N$-1. So I in binary form is 001101 . x = N/2 = 2. Then d = 2^2 = 4, q = 3 , r = 1. It is seen that $V_{MSB}(I)$ = 3 = 1101 and r = 1 =01

Thermometer code of integer I is given by

$$I = T_0 + T_1 + - - - - - - - - + T_{2^N - 1} \quad (10)$$

We know that,

$$\text{Thermometer code } Ti = 1, \quad \begin{matrix} if\ 0 \le i \le (q \times d + r) \\ = 0, otherwise \end{matrix} \quad (11)$$

Modify Equation (10) as

$$I = (\sum_{i=1}^{2^{(N-x)}} T_{(id-1)} \times d) + \sum_{j=0}^{d-1} T_{(qd+j)} \quad (12)$$

Equate equation (12) with equation (6) implies

$$V_{MSB}(I) = \sum_{i=1}^{2^{(N-x)}} T_{(id-1)} \quad (13)$$

$$V_{LSB}(I) = \sum_{j=0}^{d-1} T_{(qd+j)} \quad (14)$$

Since in our design comparator count starts from 0^{th} position. Therefore, modify formula (14) as

$$V_{LSB}(I) = \sum_{j=0}^{d-2} T_{(qd+j)} \quad (15)$$

4.2 Algebraic to circuit model conversion

An implementation of 4 bit ADC is shown in Figure 3, Where Design III comparators are used for modeling the circuit. Comparator C_0 contain $2^N - 2$ NOR gate then in C_1 last NOR is replaced by 1 NAND and this process is continue till all NOR is replaced by NAND as shown in Figure 2. In this design each column has d comparator so there will be four comparator in one column for 4 bit resolution.

For 4 bit design equation (13) =>

$$V_{MSB}(I) = \sum_{i=1}^{2^3} T_{(4i-1)} \quad (16)$$

Where x =1, single partition and d = 4 Hence, (14)=>

$$V_{MSB}(I) = T_3 + T_7 + T_{11} \quad (17)$$

&

$V_{LSB}(I) = \sum_{j=0}^{2} T_{(qd+j)}$, where q is equal to 0,1,2,3. LSB's we will be folded here by factor d =4.

Hence, above equation will changes as

$$V_{LSB}(I) = T_0 + T_1 + T_2, q = 0$$
$$V_{LSB}(I) = T_4 + T_5 + T_6, q = 1$$
$$V_{LSB}(I) = T_8 + T_9 + T_{10}, q = 2$$
$$V_{LSB}(I) = T_{11} + T_{12} + T_{13}, q = 3$$

Just for differentiation of LSB and MSB, we rename here MSB as U_3 U_7 U_{11}. Thus here we need two multiplexer based encoder, one for MSB and other for LSB whereas conventional assembly requires 11 multiplexers in decoding.

The comparator which generate lower bit in a row is connected to one line of the bus through transmission gate. The output of the comparator in one column can be fed to lower bit decoder simultaneously because control pin of transmission gate in one column are connected together. P_0, P_1 ,P2 and P3 can be used to select one and only one column whose output are given to the lower bit decoder through the bus. Complete hardware assembly is shown in Figure 3.

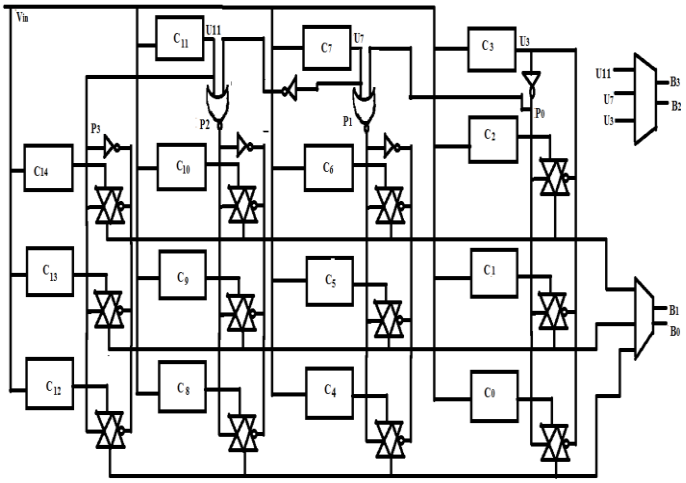

Figure 3: Design of Flash ADC using algebraic partitioning

Table I Comparison between conventional flash ADC and partitioned semi-parallel flash ADC

Conventional Design	Partitioned Design
1. It work parallel	1. At a time 1 block is work
2. Complexity of decoder is more	2. Complexity of decoder is reduced
3. No. of Mux required for 4 bit – 11 Mux 6 bit – 57 Mux	3. No. of Mux required for 4 bit – 2 Mux 6 bit – 8 Mux

V. Multiplexer Based Decoder

The performance of a decoder is one of the factor that dominate the performance of flash ADC. In this paper after comparing different decoders Mux based decoder is selected for design. Simple algorithm behind MUX based decoder is for N bit flash ADC MSB is same as thermometer output at level 2^{N-1}. To find the value of second most significant bit original thermometer scale is divided by the output at level 2^{N-1}. This partial scale is decoded by a set of 2:1 multiplexer, where the previous decoded binary output is connected to the control input of multiplexers. MSB-1 bit is found from the chosen scale in the same way as MSB was found. If the output at level 2^{N-1} is logic zero lower partial thermometer scale is selected otherwise upper partial scale is selected. This is continued recursively until only one 2:1 multiplexer remains. Its output is the least significant bit of the binary output. The regular structure of multiplexer based decoder can be easily expanded for higher resolution bits. It requires less hardware & has a short critical path. The decoder has a hardware cost

$$\Gamma_{Mux-decoder} = \Gamma_{Mux} \sum_{i=1}^{N-1} (2^{N-i} - 1) \tag{18}$$

The critical path in units of t_{Mux} is

$$t_{cp-Mux} = (N-1) t_{Mux} \tag{19}$$

A comparison of the performance between Wallace tree decoder, 4 level folded Wallace tree decoder & multiplexer based decoder for 6 bit ADC is given in the Table II. The performance is measured in terms of hardware & length of critical path [17][18].

Table II: Performance comparison of Decoders for 6 bit ADC

Type of decoder	Hardware cost	Critical path
Wallace tree	171 Γ_{Mux}	18 t_{Mux}
4 level folded Wallace tree	81 Γ_{Mux}	12 t_{Mux}
Multiplexer based	57 Γ_{Mux}	5 t_{Mux}

Comparative analysis between four different types of decoder is provided in terms of hardware required, propagation delay & power consumption for 6 bit Flash ADC. Figures given below summarizes the simulation result. Figure 4 shows the comparison in terms of power requirement. Figure 5 & Figure 6 shows the

comparison in terms of pad to pad delay & hardware required. From Table II and Figure 4, 5 and 6 we can conclude that in terms of hardware cost and conversion speed, Multiplexer based decoder is the best solution. Hence, we have used Multiplexer based decoder for the design.

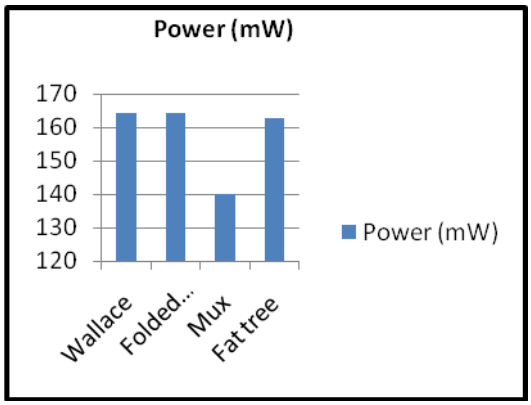

Figure 4: Power Consumption

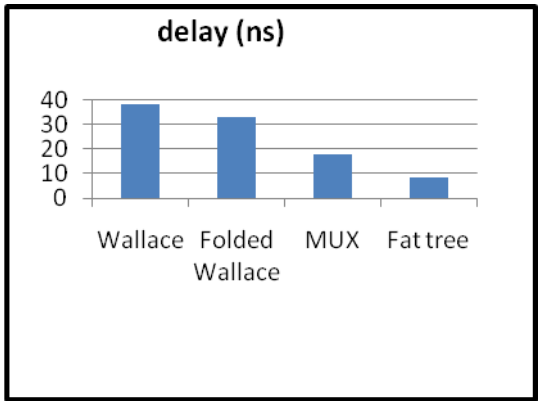

Figure 5 : Propagation delay

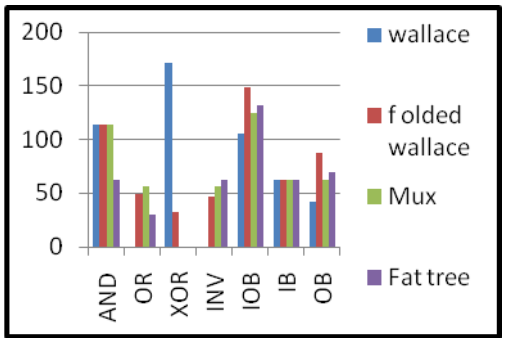

Figure 6: Hardware required

VI. Results And Discussion

6.1 Comparator Analysis

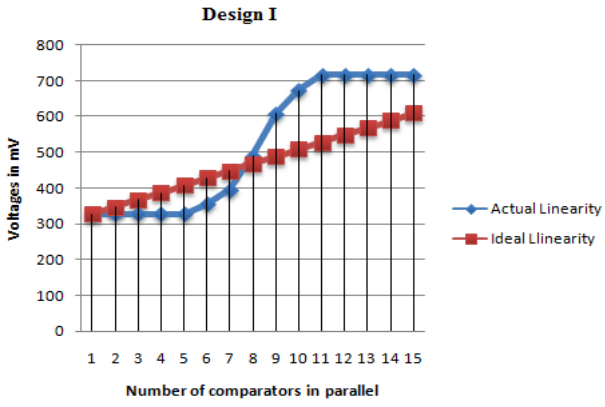

Figure 7: linearity characteristics of Design I

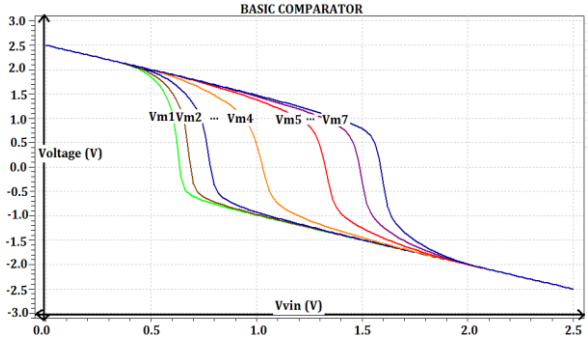

Figure 8: Transfer characteristics of Design I

The basic comparator design has been given in Figure 1. The transfer characteristics of basic comparator are shown in Figure 8, shows that the reference voltage selected by each comparator (Vm = voltage (v)/2) is different for each comparator & obtained without changing feature size. Thus the limitation of TIQ comparator is overcome in this design on the cost of increase in number of transistors. But, the limitation of this design is highly nonlinear reference selection as shown in figure 7, which leads to nonlinearity in DNL, INL calculation. To overcome this modified design II is proposed.

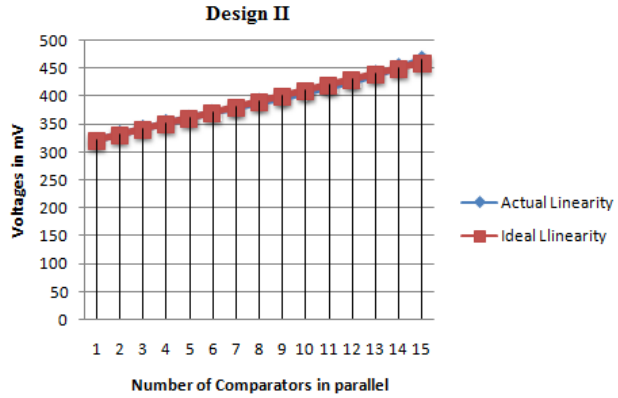

Figure 9: Linearity Characteristics of Design II

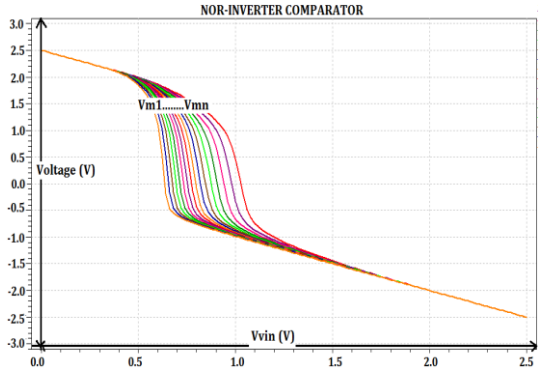

Figure10: Transfer Characteristics of Design II

The linearity issue is solved in NOR-INVERTER (Design II) comparator as shown in Figure 9. Figure 9 shows ideal curve is almost superimposing on reference curve. But the limitation of this design is that it has 0.6-1.0 volts reference range as shown in Figure 10.

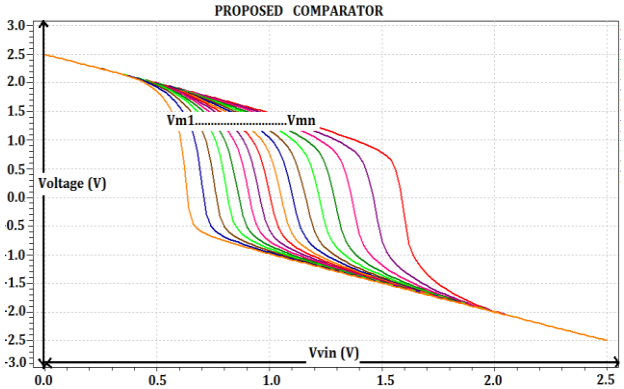

Figure 11: Reference Voltage Selection of Comparator

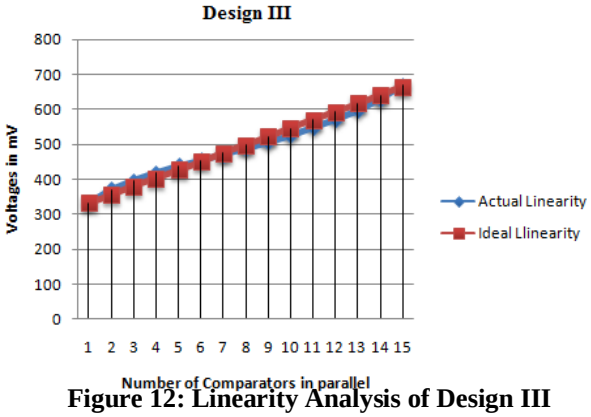

Figure 12: Linearity Analysis of Design III

In design III NAND NOR combination is used. This design shows improvement in reference range as shown in Figure 11, keeping linearity constraint. Figure 11 shows reference voltage range wider than Figure 10. Figure 12 shows linearity of design III is less than design II put the variation is very less. The number of gates requirement is less in design I but linearity issues are vital. In design II, linearity is improved but analog range is less which can be used in small range analog signal applications only. In design III linearity as well as analog range of input is increased at the cost of number of gates. After comparing Vm selection in this Figure 12; we can conclude that Design III shows better linearity over wider reference range. Thus here for ADC design we are selecting design III.

6.2 Semi-Parallel Partitioned Flash ADC Analysis

Complexity of decoder increases exponentially with bit resolution is shown in figure 13. By using algebraic remodelling decoder complexity is reduces. Hardware cost and critical path of multiplexer based decoder discussed in section II as equation 18 and 19. After using partitioning of LSB and MSB bits Hardware cost of decoder modifies as

$$\Gamma_{Mux-decoder} = \Gamma_{Mux} 2 \times \sum_{i=1}^{N/2-1} (2^{N/2-i} - 1) \tag{20}$$

And critical path equation modifies as

$$t_{cp-Mux} = (N/2-1) t_{Mux} \tag{21}$$

Equation 18, 19, 20, 21is represented graphically as shown in Figure 13 and 14. Figure 13 and 14 shows that hardware cost reduces exponentially as resolution increases. Figure 14 shows large reduction in delay after partitioning.

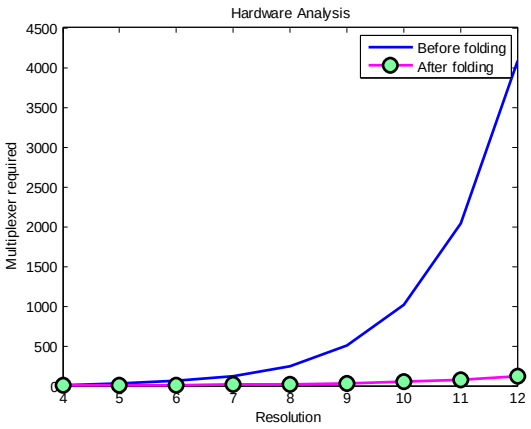

Figure 13: Comparison of Hardware Cost

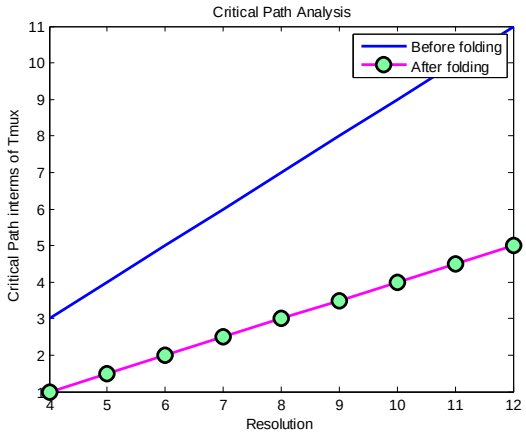

Figure 14: Delay Analysis

VI. Conclusion

Design of comparator proposed in this paper provides better linearity over TIQ comparator at the cost of increase in cost. Still the cost and power consumption is less compared to conventional resistive ladder and analog comparator based design. Comparator design tested for four corners and temperature variation provides less than 10% variation in referance voltage range. Partitioning method reduces decoder complexity reduction exponentially. Proposed design III comparator based partioned assembly provides better low cost, high speed solution for Flash ADC design.

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