

Coignof vantage of Transistor Stack and Input Vector Control Method in Leakage Current Reduction

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Abstract: Leakage current has become a regime in deep sub micrometer circuits. When we move from one technology generation to another technology generation leakage current component is increasing. Out of the total power dissipation majority is the leakage power. The dominant component of leakage power is sub threshold leakage current. Minimizing leakage current is very important in battery powered applications since the leakage drains the battery when circuit is idle. In this paper a survey is done in such a manner so as to outline what so far has done to reduce the leakage power. The paper is organized in such manner that it gives a brief description about standby leakage mechanisms, various standby leakage reduction techniques and what all are the existing technique's available.

Keywords: Leakage current, Standby leakage, Transistor stack, IVC, PBS, SAT solver.

I. Introduction

Earlier the leakage power was only minimized when the circuit was on standby mode. This is mainly because the percentage of leakage power during the active mode is very less compared to that of standby mode. The key parameter in reducing the leakage power is threshold voltage- V_{th} . Leakage reduction techniques can be broadly classified into two types, Standby leakage reduction and Run-time leakage reduction. The standby leakage reduction can be achieved by the well-known Transistor stack, Variable-threshold-voltage CMOS (VTCMOS), Multi-threshold-voltage CMOS (MTCMOS), Power gating, Combining power gating from DVFS [1]. Out this circuit techniques the most significant one is the Transistor stack. In the transistor stack by adding nmos and pmos it is possible to increase the controllability which in turn helps to reduce the leakage current and the phenomenon is known to be as "Stack effect".

It is possible to reduce the leakage current in combinatorial circuit applying an input vector to the transistor stack which is buried in the Cmos gates. The method is particularly designated as "Input vector control" (IVC). The technique is applicable once the circuit is in standby mode.

The paper organized as follows. In Section II standby leakage reduction techniques are explained, Transistor stack and what makes this technique high ground compared to other techniques are outlined in section III. Section IV deals with the various existing methods that are available in IVC technique and finally section V concludes the paper.

II. Standby Leakage Reduction Techniques

Here we describes the various standby leakage reduction techniques viz Transistor stack, VTCMOS, MTCMOS, Power gating, Combining power gating with DVFS

A. Transistor stack

Sub threshold leakage current will be reduced if more than one transistor in the transistor stack is made off. This finicky effect is known to be as stacking effect. The leakage associated with n-transistor stack is off less magnitude when compared with the leakage of a single transistor. Because of the stacking effect dainty sub threshold leakage depends on the input vector. When all the transistors are on the leakage current is at its zenith. For a nand gate once we measure the leakage associated with the primary inputs the highest leakage is 99 times higher than that of lowest leakage current. Roy has explained 3 reasons for this problem in his paper [1]. First due to exponential dependence of sub threshold leakage current on gate to source voltage, the leakage current is greatly reduced because of negative gate to source voltage. Secondly leakage current is reduced since body of

the transistors is reverse biased w.r.t source. Third is that sub threshold current due to DIBL effect is less since source to drain voltages are reduced.

B. Variable threshold CMOS(VTCMOS)

The main objective of this technique is to achieve different threshold voltages and hence it can be defined as body-biasing design technique. A self-substrate bias circuit is used to control the body bias in order to achieve different threshold voltages. Zero body bias is applied during the active mode operation whereas a reverse body bias is applied during the standby mode of operation. It has additional area and higher circuit complexity.

C. Multi-threshold-voltage CMOS (MTCMOS)

MTCMOS power gating technique is where the power gating transistors are added in the stack between the transistors and either power or ground thus creating virtual power supply rail or virtual ground rail. The logic block comprised of all low - V_{th} transistors. This is mainly for fast switching speed. To minimize the leakage current the switch transistor footer and header are made up of high- V_{th} transistors. The main peculiarities of MTCMOS are it can be easily implemented using existing circuits. It only reduces standby power. The main limitations are large inserted MOSFET increases area and delay. To maintain data in standby mode extra - V_{th} circuit is needed.

D. Power gating

It has mainly two modes of operation. Active mode and Low power mode. Power gating is exactly power management. It is necessary to switch between this two operations in an appropriate time in an appropriate manner. The main goal is to optimize power reduction and to minimize the impact on performance. The approach affects interface communication and much invasive than clock gating. Significant time delay is added to enter and leave the power gating mode.

E. Combining power gating with DVFS

Power management system is based on the idea that not all the parts of the circuit will function at the same time. Power management systems are able to identify parts of the circuits which are idle for certain conditions and shut them to reduce the leakage current. DVFS stand for dynamic voltage and frequency scaling. DVFS is also possible to apply in runtime conditions and power gating applicable standby mode. So if we couple this together means it is possible to reduce leakage current abruptly. By applying power gating a linear leakage reduction is possible. In DVFS according to the activity level it is possible to reduce the supply voltage and frequency. DVFS is only applicable for certain voltage level.

III. Vantage Of Transistor Stack

It is possible to demote the leakage current in single- V_t design by stacking low- V_t transistors [2]. Since the sub threshold current exponentially depends on the gate voltage and a substantial reduction in leakage current is possible through "stacking effect". If we consider the body effect and DIBL (Drain induced barrier lowering) since DIBL significant in sub-micron devices leakage current in transistor stack depends on weightiness of DIBL. The main hazard to leakage control using transistor stack is exactly the, gate induced drain leakage. GIDL is dependent on drain to source voltage - V_D s and gate to source voltage - V_G s.

The consequences of sub threshold current are delicate to many parameters. But dependent on threshold voltage and the temperature variations are greater. For the sub threshold leakage current the small change in length width and gate oxide thickness leads to a comparative change in sub threshold current. Sub threshold current increases exponentially with temperature. The leakage saving ratio has weightiness on temperature variations.

For the estimation of leakage current and leakage savings sub threshold slope, DIBL coefficient, and the body effect coefficients are said to be the critical parameters. Zero bias threshold voltage is critical to leakage current but not to leakage savings. The parameters such as dimensions, gate oxide thickness, and carrier mobility's have only proportional effect on leakage current. In [2] Roy has proved that leakage current can be greatly reduced by transistor stack once the circuit is at idle mode. Long settling time cannot be claimed as drawback for the usage of transistor stack.

Settling time is proportional to the internal node capacitances since it determines how much charge must have to be discharged. So it is necessary to have a correct estimation of node capacitance which includes diffusion junction capacitances. Even if no leakage is said to be occurred the charges on the node capacitances will be discharged to the ground.

Several methods are deployed to exploit the transistor stacking effect. One way is to deploy leakage control transistors between the power supply rails and the remaining circuitry. Another method is to replace

some of the transistors with gate tied transistors. This leads to sufficient decrease in leakage current. The most attractive method is to use the existing transistor stack since it is able to overcome area penalties, performance degradation and altered switching capacitances.

IV. Existing Methods In Ivc

In [3] S. Bobba and I.N.Haji has estimated the maximum leakage power with the aid of graph algorithms. The main peculiarity of the algorithms is that they are pattern independent and so no simulation is required. Constrained graph are created with the structure and logic functionality of the components in the circuits. Algorithms on graph are used to find the maximum leakage power of the circuit.

Graph formulation: Leakage power dissipated by the circuit for an input assignment to the logic block is used as the weight on the vertex that corresponds to the input assignment of the logic block. Constraints are denoted by the edges. Edge between two vertices implies that logic assignment corresponds to the two vertices are incompatible.

Optimization of the constrained graph: The problem of finding the maximum leakage power has downgraded to finding the set of vertices in the constrained graph such that sum of the weights on the vertices is maximum, ie the problem has now reduced to find a maximum weight independent set in constrained graph and it makes the problem an NP-Complete. Solution to such a problem results in larger solution space.

For to find the maximum weight independent set they have used a faster linear time greedy algorithm and it produces a lower bound. The logic behind the algorithm is that it select a particular vertex in the graph using some gain functions. The selected vertex and the vertices adjacent to this vertex are deleted and the process is continued until all the vertices are deleted. The method is general and can be applied to dynamic and pass transistor logic. The algorithm is fast and require only small time.

Roy and his colleagues in [4] have mentioned the necessities for the development of accurate estimation tools for leakage power. They are of critical importance, since the accuracy of leakage power estimation relies on standby leakage current model. They have crafted an accurate standby leakage current model which is verified by HSPICE. For this particular model they have only considered the DIBL and body effect.

Accurate leakage current model: The model that they have created was a general one since the transistor stack was of arbitrary height. Steady state leakage was measured as a function of the no of transistors that are turned off. Analysis was only done for off transistors and on transistors is treated as short circuit. With no more further explanation of the mechanism they have pointed out that the leakage depends on Primary inputs.

Genetic algorithm for bound leakage: They have gone with the enumerative methods to find maximum and minimum leakage One of the advantage of using the random search was it was able to point out the average leakage power. The genetic algorithm they have used here stops at 50 generations and produces the minimal leakage power as well as the precise primary input combination. It gives as the maximum leakage power as well the worst case primary input combinations once the chromosomes are sorted by non-increasing fitness.

In [5] J.P.Halter and F.N. Najim have put forward a design technique for the reduction of leakage power. It was mainly based on the observation that logic gates are subjected to dissipate leakage current during steady state. For to find such a low leakage state they have developed an algorithm. These algorithms are able to determine input vectors by sampling the random vectors.

They have modified the logic design by means of minimal additional circuitry in standby mode so that the internal circuitry will be in a state of low leakage and circuit will comes back to the active state once it is reactivated. By random sampling they were able to put forward an algorithm that points to a vector which produces the minimum leakage value.

M. Johnson, D. Somasekhar, and K. Roy in [6] address the methods to estimate leakage at circuit level and also provided some heuristics and exact algorithm for random combinatorial circuits. These algorithms can be employed in power management applications or quiescent current. They have put forward a leakage model of transistor stack which can be used to evaluate the leakage of a cmos circuit for a choosy input signal. For small circuit the method evaluates all the possible inputs whereas for large circuit leakage for special circuit is analysed hierarchically.

Leakage observability measure: For to find the minimum and maximum leakage vector they have provided leakage cost measure called "leakage observability". The main principle behind the method is to evaluate the degree to which a particular input is observable in magnitude of leakage from the power supply. The heuristics and branch and bound algorithms useobservability measure to calculate maximum and minimum leakage current.

"Robust SAT-based search algorithm for leakage power reduction" presented by F. Aloul, S. Hassoun, K. Sakallah, and D. Blaauw, has changed the direction of research in leakage reduction by means of IVC. The paper in [7] uses an incremental SAT solver PBS which can be used to find maximum and minimum leakage

current associated with a particular circuit. In this method a SAT problem is created for the circuit which contains an objective function to be minimized or maximized. The problem holds the set of CNF clauses which paradigmatic the circuit behaviour and the constrain which specifies the extent of leakage. The estimate of desired leakage problem is represented in PB, in which Boolean decision on primary inputs will determine the leakage of the circuit. The method is set to have improved performance over random approach.

“Leakage current reduction in CMOS VLSI circuits by input vector control,” put forward by A. Abdollahi, F. Fallah, and M. Pedram, [8] have emphasised several methods to reduce leakage current of a circuit. The methods they have used don't alter the process technology and hence they are easy to use. In the method they have used a sleep signal so as to set all the values of internal signals to reduce the leakage current. This is possible since leakage is dependent on primary inputs. Then they have inserted nmos and pmos into certain gates to reduce the leakage current by the well-known stack effect. In both the techniques Boolean satisfiability is employed to formulate the problem and solved by a SAT solver.

For leakage minimization by input vector control method they have constructed a Boolean network which computes the total leakage of the circuit and is designated as LCN (leakage computing network). Boolean clause is used to calculate the leakage of the primary circuit and with a SAT solver an input vector for leakage minimization is obtained. From this the MLV is produced. Then the primary circuit is modified by the addition of multiplexers which will shift the MLV at idle mode.

Leakage reduction by adding control points: Circuits with larger logic the leakage current can be reduced if the internal nodes of the circuit are controlled. For this purpose multiplexer is inserted at the input of each gate. A SLEEP signal which select the precise input during active mode and also selects input values that produce low leakage in standby mode.

In paper [9] Afshin Abdollahi, Farzan Fallah, Massoud Pedram, states that leakage current is not only dependent on current state but also on the state history. The main postulate behind leakage power reduction technique is that leakage is a memory less function. In this article the authors have elucidated that leakage current is not only the depend on current state but also the previous state. What the reason they are pointing is output of logic states reach their steady state very fast, but in some cases it will take longer time. So they argue for to revise the leakage reduction technique.

Article [10] deals with the two methods of leakage power minimization in static cmos circuits by the aid of IVC. Leakage effects have been modelled by Pseudo Boolean functions. These are coupled to VG-ILP (optimal integer linear programming) and a heuristic mixed integer linear programming (MLP). They have constructed an ILP model called VG-ILP or virtual gates. Virtual gates are just the cells added for model formulation. ILP produces the minimum leakage vectors. Virtual gates simplify the ILP formulation and also reduce the run time.

VG-ILP model: This miniature creates a problem for producing input vectors with minimum leakage current with the aid of ILP formulation. For this purpose certain objective function should have to optimize and some constraints should have to be satisfied and has to be linear. The variable also must have to be linear.

MLP model: This pattern is specially designed for reducing run time. Primary stage deals with a model formulation. Once the results are produced it contains the binary form of the variable 'f', its logic value l (f) and arithmetic value a (f). MLP pattern is much faster than ILP.

Paper [11] presents a new approach for finding minimum leakage vectors (MLS). Vector applied in MLS is known as IVC and is very useful in reducing gate oxide and sub threshold leakage. These are based on implicit enumeration of integer valued decision diagram. Search space for minimum leakage vector increases exponentially with primary inputs. To reduce switching power dissipated MLS algorithm extended to compute bounded leakage sets (BLS). In IVC minimizing standby leakage current results in the power consumption due to switching which is proportional to input being driven in standby. If the no: of inputs being driven is reduced then switching can be reduced. From this a minimum cost cube can be constructed.

The paper presents algorithm for to perform accurate leakage analysis, INSPENUM: Implicitly enumerates circuit leakage w.r.t the inputs. For larger circuits MINCUTENUM: Performs enumeration in mincut space of the circuit hyper graph with optimality. The focus of the work is to reduce the switching cost of IVC and for that FINDBLS is used to compute the bounded leakage set (BLS). This particular method has improvement over Boolean SAT. They have reduced the the switching power by 60%, while standby leakage by 20%.

A comparison is made in the paper [12] mainly between input vector control, body bias control and power supply gating. They have identified the limits for potential leakage reduction, performance penalty, area and power overhead. The important observation they have made is IVC outperform body bias control (BBC) but they have the limitations.

“A Combined Gate Replacement and Input Vector Control Approach for Leakage Current Reduction” presented by Lin Yuan and Gang Qu in [13] have made the modification in such a way that they have replaced the internal gates which are subjected to the worst case leakage during active mode so that the circuit

functionality is kept as such. By gate replacement technique they were able to reduce the leakage by 40%. The overhead analysis makes it clear that control gates consume both leakage power and dynamic power. Here they have only considered the leakage power. Second is the sleep signal which consumes extra power.

V. Conclusion

The paper that we have discussed here is focused on the different standby leakage reduction techniques and what the existing techniques are. Each technique is said to have its own upper hand and also drawbacks. From the discussion that we have made so far clearly indicates that transistor stack with IVC technique is the sophisticated method for reducing leakage current. Transistor stacking is proven to be highly effective in lowering the sub threshold leakage in standby mode since it can be claimed as the major part of the total leakage power dissipation.[14],[15]. We believe that the discussion made here will be very helpful for the future circuit designers and VLSI architect the appropriate method for the reduction growing leakage current.

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