Low Power Circuits using Modified Gate Diffusion Input (GDI)

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Abstract: *Gate Diffusion Input (GDI) is a technique for designing low power circuits. This technique allows usage of less number of transistors as compared to CMOS logic. The basic GDI cell consists of only two transistors which are used to implement the basic logic functions. Because of less number of transistors, the switching is reduced and hence there will be a less power, delay and also reduced area. Complex functions can also be implemented using this technique. In this paper basic GDI cell is modified to get a "good" logic 0 and it is compared with the CMOS logic. The low power full adder is designed using GDI technique and is modified to get the strong logic zero. Using this modified GDI full adder, 4 bit Ripple Carry Adder and 4*4 Array Multiplier are designed and simulated. The simulation is done using CADENCE VIRTUOSO based on 45nm technology with the supply voltage of 1.2V.*
Keywords: *Full Adder, Ripple Carry Adder, Multiplier, Low Power, GDI.*

I.   Introduction

With the advent of new technology and techniques, complexity of the electronic circuits is increasing rapidly. This increase is in turn resulting in increase in power consumption. Hence, there is an earnest need and interest in designing circuits with less power consumption without disturbing the functionality of the circuits. This decrease in power will also enhance the performance of the circuit. There are mainly two sources of power dissipation. First is dynamic which is one of the main sources of power dissipation and is due to the switching activity of the node capacitance. This can be reduced by avoiding the unwanted switching activity in the circuit. Second is the static power dissipation. This is due to the leakage current when the transistor is not switching.

There is short circuit power dissipation that can be considered as a part of the dynamic power dissipation when there is direct path from supply to ground [1]. There are many techniques either to reduce the dynamic or the static power dissipation. The most common circuit design style or technique for designing any digital circuit is CMOS. But it dissipates most of the power during transistor switching activity. Hence, other techniques, such as using Pass Transistor Logic, Complementary Pass Transistor Logic, etc were explored for power reduction. The GDI technique proved to be more efficient compared to the others.

The Gate Diffusion Input (GDI) technique is one of the efficient low power techniques. A basic GDI cell consists of only two transistors. Using this technique any complex functions can be implemented with a less number of transistors as compared to CMOS logic. Because of the less number of transistors the switching node capacitance will be reduced that results in reduction of dynamic power.

Table 1. GDI Functions

N	P	G	D	Function
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT

Here we propose a power efficient Carry ripple adder and array multiplier based on gate diffusion input circuit design style. The GDI cell is modified to obtain the strong 0 and using this modified GDI circuit an adder and the multiplier are designed.

The main advantages of GDI techniques are less power, high speed, less area and more flexibility to the designer. The disadvantage of GDI is that of reduced swing, i.e., degraded output depending on the combination of the each input (explained in section II).

Since, GDI techniques are better suited for low power design, this paper attempts to design circuits based on GDI. First the basic gates such as AND, OR etc are designed and implemented. Using these basic gates, Full adder circuit is built. A 4-bit Ripple carry adder and a 4*4 multiplier is also designed and implemented. The designs and implementation results of each design are explained the following sections. These designs were implemented using Cadence Virtuoso based on 45nm Technology.

The paper is organised as follows: Section II gives a brief overview of a Basic GDI cell and its functioning. Section III describes the implementation of the basic gates such as AND, OR, XOR, half adder using GDI and Modified GDI. Section IV presents the GDI based full adder and a GDI based modified full adder. The implementation of a GDI based ripple carry adder and multiplier designs are given in section V. Section VI presents the results of comparison between GDI designs and CMOS implementations for the same designs. Finally Section VII concludes the paper.

II. GDI Basic Functions

The basic GDI cell consists of two transistor as shown in Fig 1. It has three inputs: G, P and N. The Drain terminals of the two transistors are taken as output. Source terminal of Pmos is acting as one input, and Source of Nmos is acting as another input. Bulk of Nmos and Pmos are connected to ground and supply respectively as shown in the Fig 1. Table 1 shows the implementation of few functions using GDI cell [4-5].
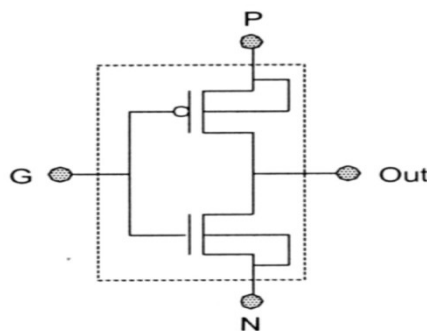

Fig.1 Basic GDI Cell

The main disadvantage of a GDI cell is the degraded output: The NMOS produces strong logic 0 or weak logic 1[3]. Similarly PMOS produces strong logic 1 or weak logic 0. From Fig 1, when G=0 Pmos will be turned on & hence P input passed to the output. Similarly when G=1, Nmos will be turned on and passes the N input to the output. When Pmos is turned on, if P input is at logic 0 that results in weak logic 0. Similarly when Nmos is turned on, if N input is at logic 1 then, it results weak logic 1. Hence, Pmos produces weak logic 0 and Nmos weak logic 1 respectively. Here the idea is to modify the GDI cell to produce the strong logic 0 which in turn can be considered as valid input to the next stage.

III. Implementation of AND, Half Adder using GDI and Modified GDI

Consider an example to design AND (Y= AB) gate using GDI cell. From Fig 1, G=A input, P=Gnd, N=B input. When A=0, input P is passed to output i.e grounded (Pmos Source), hence the output results in weak 0. When A=1, B input will be passed to output through Nmos. If B=1, then output will be degraded because Nmos passes poor logic 1. But if B=0 then that results in good 0, as Nmos passes good logic 0. The AND gate simulation of GDI cell and Modified GDI AND gate are shown in the Fig 2 and 3 respectively. It is shown that Modified GDI cell gives good logic 0 (Fig 3). The Modified GDI cell is designed for all the logic gates and also for the full adder design. The idea is that, when Pmos is turned on and if it passes logic 0 then it will be passed through Nmos so that it can produce good logic 0. For example considering AND gate, A=0, P input (gnded) is passed through Nmos rather than Pmos. If P input is logic 1 then it will be passed through Pmos to produce good swing. Similarly OR, XOR, MUX, and Half Adder circuit are modified to obtain proper output. Fig 4 and 5 show the GDI Half Adder and Modified GDI Half Adder simulation waveforms respectively.
The average power for AND, OR, MUX, Half Adder circuit using GDI cell and Modified GDI are shown in the Table 2.
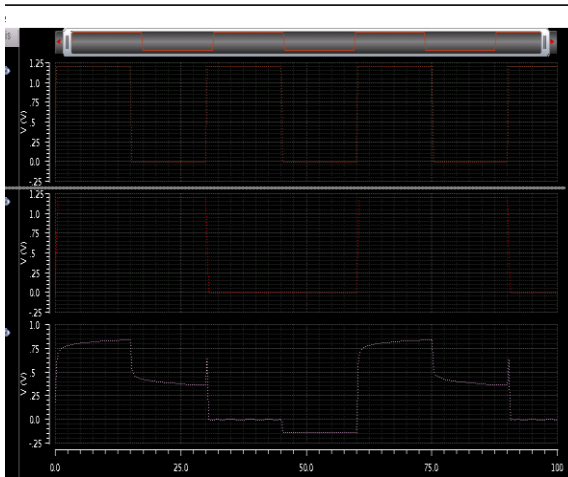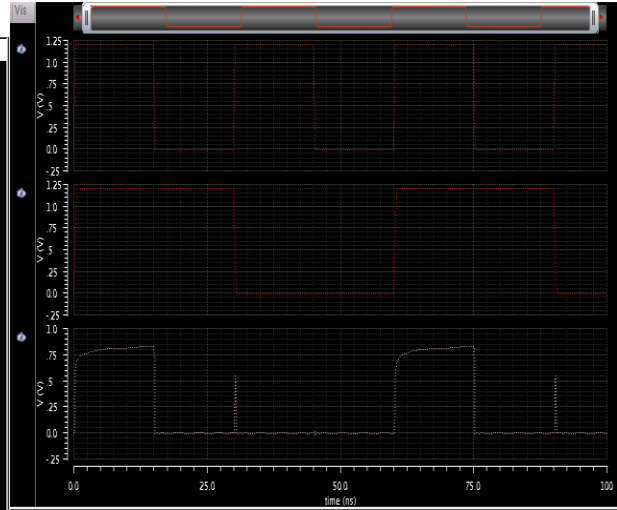
Fig 2: GDI AND Gate
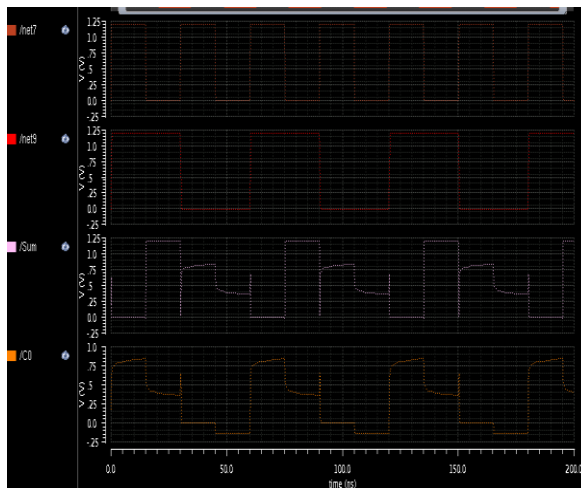

Fig 3: Modified GDI AND Gate

Fig 4: GDI Half Adder Circuit
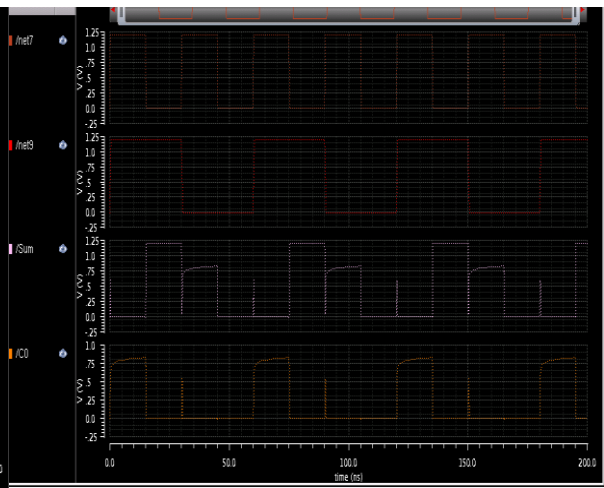
Fig 5: Modified GDI Half Adder Circuit

Table 2 . Average Power of GDI, Modified GDI

	GDI	Modified GDI (nw)	CMOS (nw)
AND	558.3x10-15	10.89	33.26
OR	10.66nw	10.89	14.87
XOR	175.3x10-12	21.57	54.64
MUX	337.9x10-12	3.41	51.77
HALF ADDER	7.6nw	33.16	82.69

IV.   Full Adder

The Full Adder Circuit is designed using 10T as shown the Fig 6. Full adder circuit consists of 2 inputs A and B, and one carry in as Cin. The 2 outputs are Sum and Cout. The truth table of 1-bit full adder is given in Table 3. The two outputs are obtained by the following expressions:

Sum = A xor B xor Cin

Cout = (A xor B) Cin + AB.

Table 3: Full Adder Truth Table

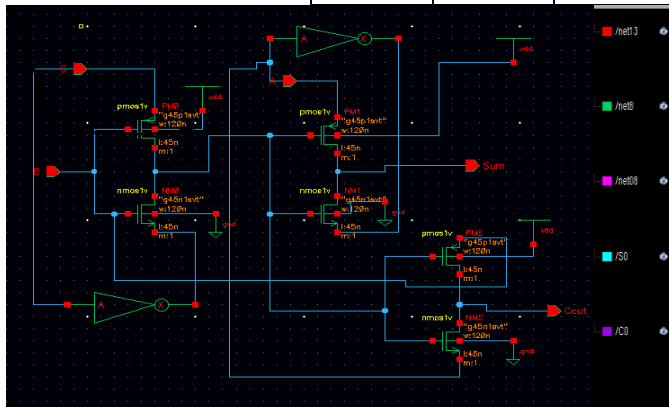| A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

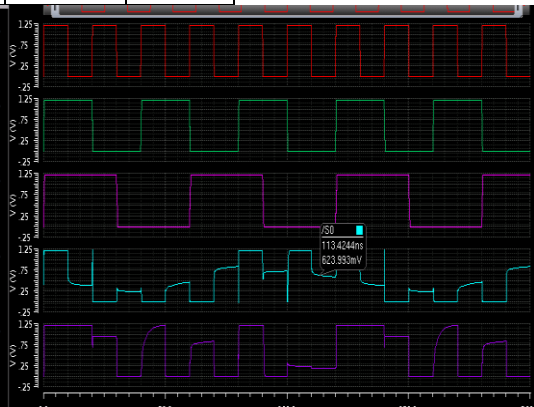Fig 6 . GDI (10T) Full Adder.   Fig 7 Simulated output of GDI Full Adder

The output Sum and Cout are implemented using 10T. The simulated output of the full adder design is shown in Fig 7.

Consider an example as shown: when inputs A,B,C are changing from 100 to 000 then Sum output should change from 1 to 0. When Sum = 0 for A, B, C=0,0,0 the output has a minimal voltage of 600mV as shown in Fig 7. This minimal voltage can be considered as logic 1 for next stage, which will result in an incorrect output. From the Fig 7, when A,B,C=100, Sum output gives good logic 1 through Pmos. When A goes to 0 then Sum output will not go to a full 0, before next input combination appears. Hence this will result incorrect output. The average power of this circuit is calculated and is shown in Fig 8.
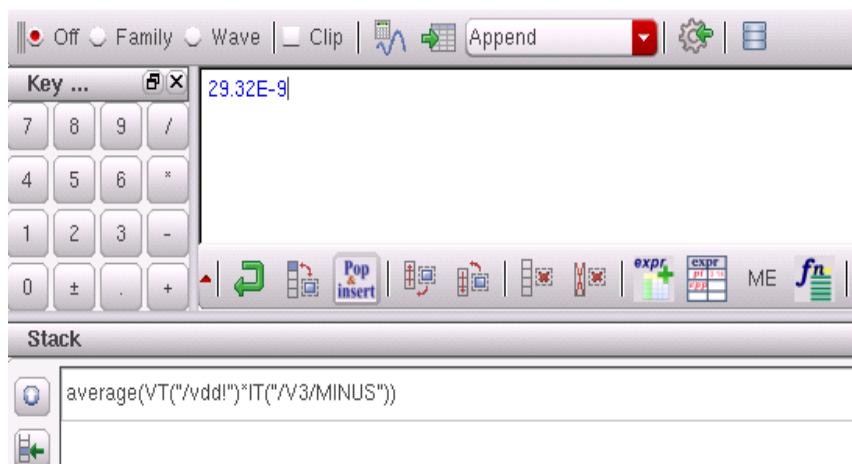
The Full Adder (10T) is modified to obtain the full swing of logic zero. The number of transistor increases by 7 for 10T full adder. Fig 9 shows the design for Modified Full Adder using 17T. The Simulated waveforms are shown in Fig 10. Here the low voltage is reduces to zero and that can be considered as correct result for the next stage as compared to the Fig 7. The average power of both GDI Full Adder and Modified GDI Full Adder is calculated.
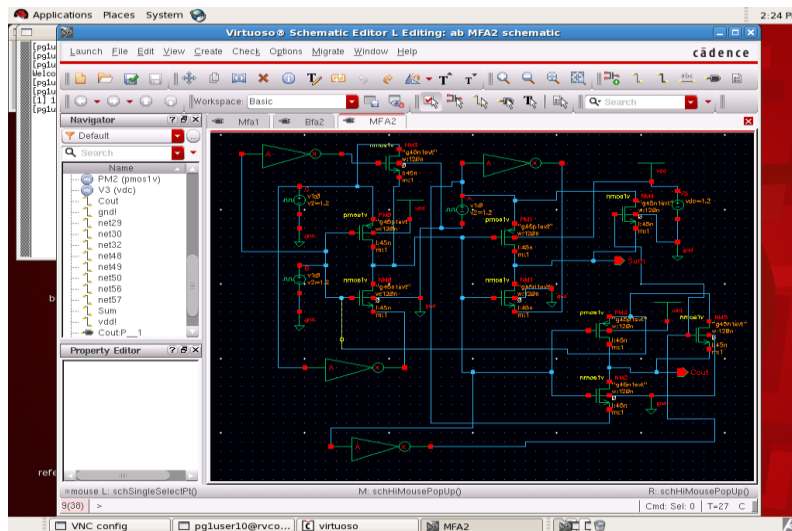
Fig 9 Modified GDI Full Adder

Fig 10 Simulated output of Modified GDI Full Adder

V.   Ripple Carry Adder & Array Multiplier

The adder, multiplier circuits are the basic building blocks of the arithmetic unit. Using the Low power full adder circuit, Ripple Carry Adder (RCA) or Parallel Adder is designed. The ripple carry adder is constructed by cascading full adders blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used. One of the drawbacks of this adder is that the delay increases linearly with the bit length. The worst case delay will be from Cin to Cout of most significant bits. The delay of ripple carry adder is linearly proportional to the number of bits. Each full adder stage has to wait for the previous stage carry, and it is propagated to the next stage. Due to this Ripple carry adder has increased delay. The advantages of this adder are simple design and lower power consumption. The 4 bit Ripple Carry Adder is designed in [7]. In the current paper the RCA circuit is implemented using both 10T and 17T full adder and compared with CMOS RCA. The block diagram of 4 bit RCA is shown in Fig 11. Here the first full adder circuit (from left) produces the carry C_1 for the next stage and it is considered as Cin for the next stage. Similarly carry generated from the current stage (Cout) becomes carry in for the next stage. The final carry output is taken from the forth full adder. Each four full adder is has two bit inputs from A_0 to A_3 and from B_0 to B_3. The sum outputs are taken from each full adder and the final carry out as a output.

The multiplier is a circuit that can be used in many applications like signal processing, processor, etc. There are various multiplier designs available. This paper addresses one specific multiplier called the Array Multiplier. An Array Multiplier multiplies each bit and adds the partial products as shown in Fig 12. It requires a

number of AND gates and Full adder to generate partial products. One advantage of the array multiplier is its regular structure. This regularity of the multiplier makes it is easy to do the layout and has a small design size. The design time of array multiplier is much less than that of a tree multiplier. Another advantage of array multiplier is its ease of design for a pipelined architecture. The main limitation is that they are very large. As the number of operand increases, the size increases.
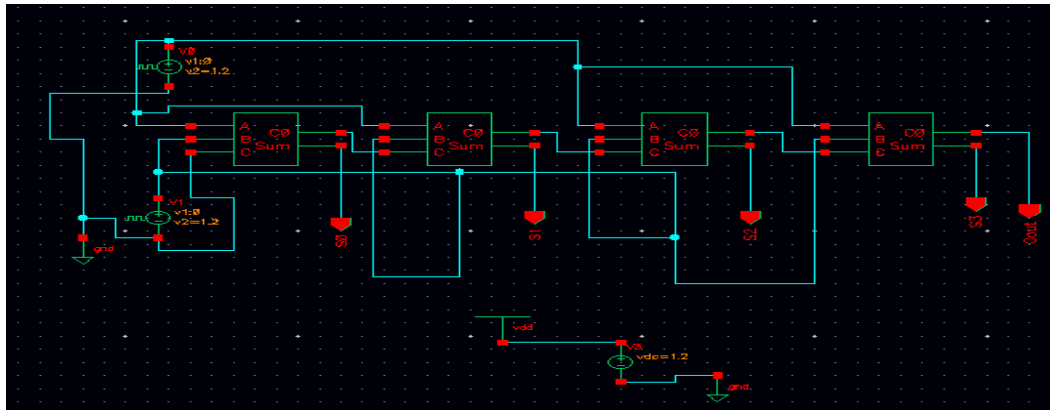

Fig 11   4 bit Ripple Carry Adder

The main block of the multiplier is full adder circuit as depicted in Fig. 12. The 4* 4 Array Multiplier is designed using GDI technique. The array multiplier is designed using the modified GDI technique to obtain the good low logic. The number of transistors are increased as compared to the standard GDI multiplier. This design is compared with the CMOS Array Multiplier.
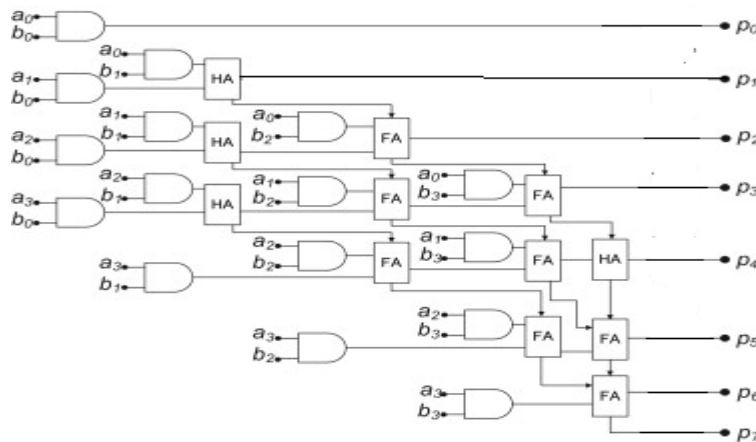

Fig 12. The block diagram of 4*4 array multiplier

VI.   Result

The three designs full adder, 4-bit RCA and array multiplier were designed and simulated using Cadence Virtuoso on 45nm Technology. All three designs were implemented using standard GDI, modified GDI (to obtain a good 0) and CMOS Technology. These designs were compared and the results for the same are presented in Table 3.

The average power is calculated for GDI circuits, Modified GDI circuits and CMOS circuit. From Table 3 it is shown that the modified GDI circuit gives less average power as compared with the CMOS circuit. The Modified GDI cell increases the number of transistors to improve the swing as compared to the GDI cell. But still the modified GDI circuit gives good average power as compared to the CMOS logic.

Table 3: Average Power consumption

	Average Power		
	Full Adder (nw)	4bit RCA	4*4 Multiplier (uw)
10T (GDI)	29.32	274.9 nW	1.62
17T (Modified GDI)	82.24	428.3 nW	2.55
CMOS	360	1.01uw	3.0

VII. Conclusions

The GDI is an efficient low power design technique. Complex functions can be implemented using this technique using less number of transistors. The disadvantage of the GDI technique is that, it is not possible to obtain a strong 0 and strong 1 at the output under certain combinations of inputs and previous state. An improvement was mentioned in this paper to overcome the disadvantage of GDI cell. The GDI cell is modified to obtain the proper low logic. The number of transistors increased but still the count remained less than that in the CMOS logic.

Three circuits – full adder, 4-bit RCA and multiplier, were designed and implemented using GDI, modified GDI and CMOS technology. All three designs and technologies were compared and results presented. It was shown that the modified GDI though consumes more power than standard GDI technique, it is still can be considered as low power when compared to CMOS logic.

The practicality and applicability of the modified GDI technique needs to be explored for complex circuits such as Dadda Multiplier, Carry Skip Adder etc.

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