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Layout Designing for Different Full Adder Topologies at 0.18μm Technology Node

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***Abstract*:** *In this paper VLSI layout designing and optimization techniques for different full adder topologies like Complementary MOSFET full adder (CMOS),Transmission gate full adder(TGA),Complementary Pass transistor Logic full adder(CPL) and Domino Full Adder has been discussed. Power consumption and propagation delay are the major issue for low voltage level circuit application designing in recent years. Full adders are the very important circuit element for calculating the basic four mathematical operations (addition, subtraction, multiplication and division) functions in Integrated circuits. In VLSI systems such as microprocessors and application specific DSP architecture are using different full adders for calculating mathematical operations. In this paper one bit full adders topologies has been used for analysis. The layout designing of the basic logic gates and different full adders is done using L-Edit v14.11 Tanner EDA tool using 0.18μm technology node. The results shows that parameters like Power consumption and total propagation delay, for a particular aspect ratio the Transmission Gate Full adder consume less power and having less propagation delay.*

***Keywords*:** *CMOS full Adder, CPL full adder, layout designing, Domino Logic Full adder, L-Edit v14.11 Tanner EDA tool, Transmission Gate Full adder.*

I. Introduction

Layout designing is the representation of an integrated circuit(IC) in terms of planar geometric shapes which correspond to the patterns of oxide or semiconductor layers and metal that makes up the components of the integrated circuits. To verify the safety of mechanical components and structures against collapse layout optimization technique is used. Layout optimization technique is applied to the problem of identifying the critical layout of slip-line discontinuities in a solid body. Layout can be characterized as the step in the design hierarchy where an electronic circuit is transferred to a silicon description [3]. The layout designer is responsible for creating the patterns on every layer such that the resulting stacked structure defines the electronic switching devices (transistors) and the wiring that connects the switching devices together. To do this, we must first examine what constitutes a transistor, and then learn the characteristics of the conducting and insulating layers. These results in a set of rules that help guide the complex task of defining every part of every transistor correctly and then providing the metal wiring. Layout is performed entirely on a computer using layout editor. Every layer on the chip is patterned so that the resulting layers stack into three-dimensional structures that constitute the electronic network. A common grid is used throughout the process, and the screen portrays the entire design, but the patterning information for each layer is stored in a separate database. It is the responsibility of the layout designer to insure that the patterns follow the geometrical guidelines established for the fabrication process. Violating the rules may result in a non-functional chip. The layout tools also provide the ability to translate a set of patterns into the equivalent electronic circuit for comparison. Depending on the application, this type of circuit design to be implemented, and this design technique used, different performance parameter become more important. In the previous study in past, the parameters like high speed, low cost and small area were the major issues of concern, but due to great demand of low power devices power Considerations are now gaining the attention of the community associated with VLSI design. In addition, reliability is strongly affected by power consumption. The High power dissipation is also associated with high temperature operation, which, in turn, may well tend to the failure mechanisms in the system. Two components determine the power consumption in a CMOS circuit:

1. Dynamic power consumption
2. Static power consumption

CMOS devices have very low static power dissipation, which is the result of leakage current. The dynamic and static power consumption occurs when all inputs are held at some valid logic level and the circuit is not in the charging states or in ON state. There are three major sources of power dissipation in digital CMOS

circuits, which are summarized in following equation:

$$P_{tot} = P_{(static)} + P_{(dynamic)} \quad (a)$$

The equation (a) represents the switching component of power, where f_{clk} is the clock frequency, C_L is the load capacitance.

$$P_{(dynamic)} = C_L * V^2_{DD} * f_{clk} \quad (b)$$

Where
Pd = transient power consumption
V_{DD} = supply voltage
The leakage current $I_{leakage}$ which can arise from substrate injection and sub-threshold effect is primarily determined by fabrication technology considerations. The switching power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage.

$$I_{leakage} = Is * e\ (qv/kT-1) \quad (c)$$

Where
Is = reverse saturation current v = diode voltage
k = Boltzmann's constant (1.38 *10−23J/K).

$$P_{(Static)} = V_{DD} * I_{SC} \quad (d)$$

Where
VDD = supply voltage
Isc= current into a device (sum of leakage currents)
The accurate analysis of propagation delay is quite difficult in digital electronics, a simple first order derivation [7] can be used to show the relation between power supply and delay time.

$$Td = CL * VDD/ (K*VDD-VTH)\alpha \quad (e)$$

Where
K = Transistor's aspect ratio (W/L)
VTH = Transistor threshold voltage
α = Velocity saturation index (varies between 1 and 2).

II. Research Already Done In the Field

With the help of some reference papers it is seen that previously the work done in this field is to make the efficient layout of full adder and the analysis of its performance. In modern VLSI circuit's logical operations plays an important role. Full Adder circuit plays a very important role in Digital Signal Processors (DSPs), Application Specific ICs (ASICs), Digital Processors and many other low power applications designing. Hence the implementation of full adders with low power and high performance is very essential requirement in digital electronics. Hence increasing the performance of 1-bit full adder shows a great impact on increasing the performance of the whole system. Designing low-power and high speed VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile and other battery power applications in cellular system. Different design styles have been proposed to implement 1-bit adder cells through VLSI technology. These adders are commonly aimed to reduce power consumption (Dynamic and Static), area and increase speed. In recent research we have found that Complementary Pass transistor Logic (CPL) is much more power-efficient than complementary CMOS. The comparative performance of 1-bit CMOS (Complementary MOSFET) full adder, Transmission gate full adder, CPL (Complementary Pass Transistor Logic) full adder and Domino logic full adder, designed using TANNER EDA, using 0.18micrometer technology with different CMOS logic design styles. To designing the Full adder layout its depend on the number of transistor used if the number of transistor is more the power ratio will increased to make power efficient layout is to required less number of transistor to make low power dissipation .

III. Proposed Methodology of the Research Work

Efficient layout optimization techniques for various full adders are proposed for CMOS Full Adder, Transmission Gate Full Adder (TGA), and Complementary Pass Transistor Logic Full Adder (CPL) and Comparison between the above in terms of aspect ratio that different parameters like Dynamic and Static Power consumption and total propagation delay. Layout designing is an iterative process which starts with the circuit

topology and the initial sizing of transistors. Using a layout editor tool according to the layout design rules mask layers are drawn. These are as follows:

- Process Design Rules
- Width Rule
- Space Rule
- Overlap Rule

This procedure may require several small iterations in order to accommodate all the design rules without changing the basic topology. After that, the layout is checked for errors using the Design Rule Check. Following the DRC, a circuit extraction procedure is performed on the finished layout to determine the actual transistor sizes and the parasitic capacitance at each node. The result of a detailed SPICE input file. The actual performance of the circuit design can be determined by performing a SPICE simulation, by using the extracted net list. If the simulated circuit performances do not match the desired specifications then the layout design must be modified and the whole process must be repeated. The layout modifications are based on the aspect ratio of the transistors, since the aspect ratio of the transistors determine the device trans- conductance and parasitic capacitance. The layout designing of the basic logic gates and different full adders is done using L-Edit v14.11 Tanner EDA tool using 0.18µm technology node.

IV. Layout Design Rules

A. Process Design Rules

Design rules are the rules that have to be respected when a given design is laid out. There are design rules for polygons and paths, transistors, and contacts. This processing group defines the design rules by trading off the cost-to-manufacture and yield, among other things, against the minimum feature size that is manufacturer by the equipment and processing steps [1]. Other factors that influence the definition of design rules could be the maturity of the manufacturing tools and process or the market requirements for an IC or foundry service. Overall, design rules are put in place to help layout designers understand and account for physical three-dimensional limitations and manufacturing tolerances within the layout tool environment.

B. Width Rule

The minimum width of a polygon is a critical dimension, which defines the limits of the manufacturing process. A violation in a minimum width rule potentially results in an open circuit in the offending layer. The manufacturing process will not reliably produce a continuous connection or wire below a specific value, and breaks in the path would result at the point at which the width rule was isolated.

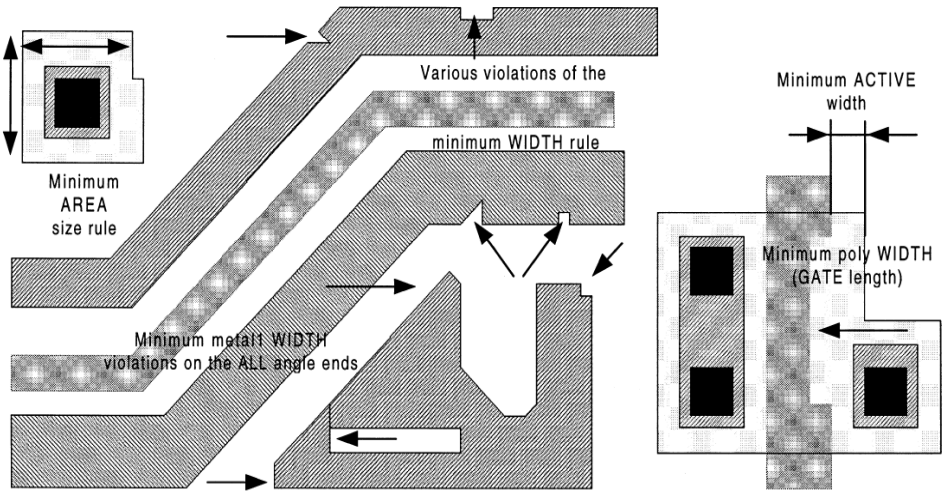

Fig. 1 Examples of the width rule [9]

C. Space Rule

Another critical dimension is the space rule, which is the minimum distance between two polygons. Generally, the space rule is applied to avoid an unwanted short circuit between the two polygons. Together with the width rule on a single layer, the space and width rules define a layer pitch. The pitch of a layer is important when considering interconnect and routing porosity. The routing area consumed by n metal lines is easily calculated by multiplying the number of lines by the layer pitch.

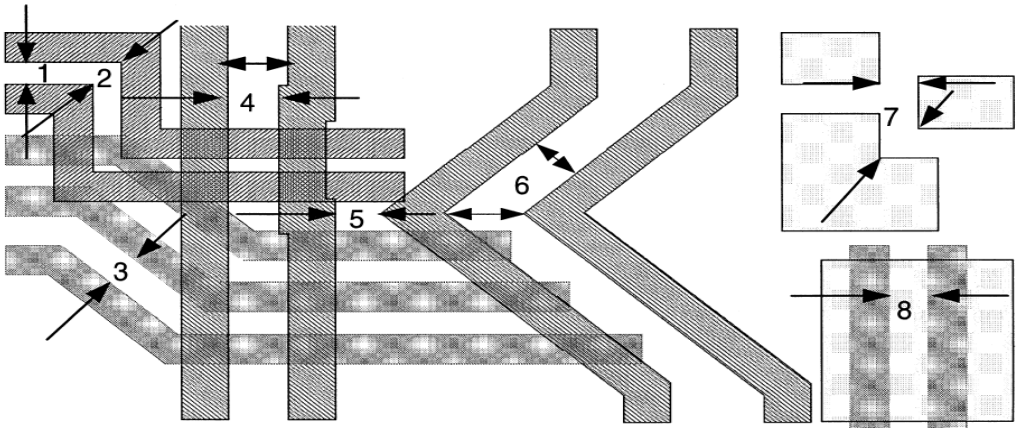

Fig. 2 Examples of the space rule [9]

D. Overlap Rule

As its name implies, the overlap rule is defined as the minimum overlap or surround of one polygon by another. The overlap of a metal layer over a via or contact is a prime example of this rule. This rule always involves polygons that exist on different layers, and this fact is the principal reason why this type of rule is required. Whenever structures are to be manufactured using polygons on two different layers, there is a significant chance that there will be a misalignment between the desired and actual relative placement of the two polygons. Misalignment between polygons can result in both undesired open and short circuit connections, depending on the layers involved. Fundamentally, overlap rules reduce the impact of a small misalignment between layers in the manufacturing process by ensuring that the desired connectivity is maintained. The overlap rule states that the two layers in question must not only overlap each other; one layer must surround the other by a certain value. This value is the value for the overlap rule. In the case of the contact, the upper and lower layers must completely overlap the contact and surround the contact hole by the overlap rule value [1]. If one of the layers does not sufficiently overlap and surround the contact hole, then the connection will not be reliable under all manufacturing conditions since the area that is available for the electrical connection is reduced. This results in a poor or weak connection.

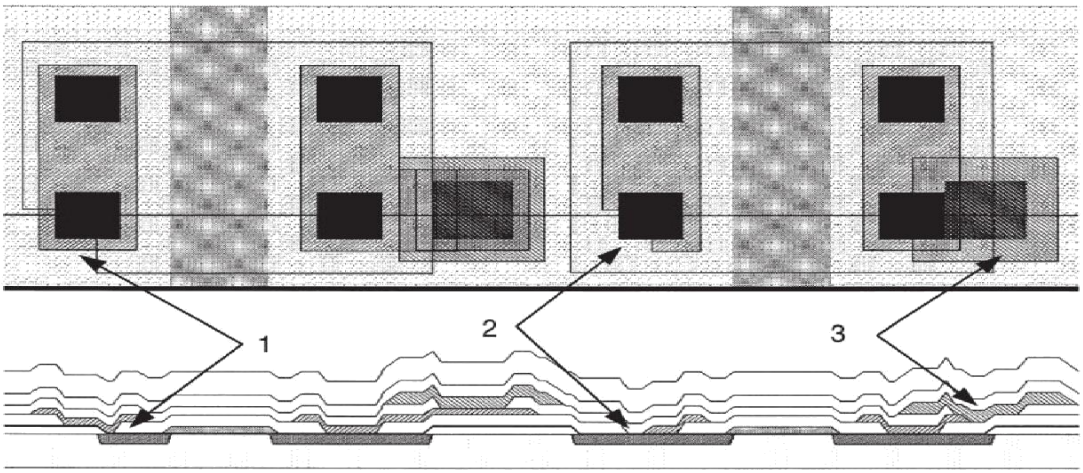

Fig. 3 Examples of the overlap rule [9]

V. Layout Design and Layout Optimization Techniques of Various Full Adder Topologies

A. CMOS Full Adder

The conventional CMOS full adder has 28 transistors and is based on the regular CMOS structure with conventional pull-up and pull-down transistors providing full-swing output and good driving capabilities. The layout of CMOS full adder circuit is shown in Fig. 4.1. And Fig. 4.2 shows the schematic diagram. A one-bit full adder has three one-bit inputs (A, B, and C) and two one-bit outputs
(Sum and carry). The relations between the inputs and the outputs are expressed as:

$$Sum = A \oplus B \oplus C \quad (1)$$

$$Carry = A * B + B * C + C * A \quad (2)$$

A complementary static CMOS circuit consists of an NMOS pull-down network connecting the ground to the output and a PMOS pull-up network connecting the power to the output. In this style all transistors (either PMOS or NMOS) are arranged in completely separate branches, each may consist of several sub-branches [4]. Mutually exclusiveness of pull-up and pull-down networks is of a great concern. The input capacitance of a static CMOS gate is large because each input is connected to the gate of at least a PMOS and a NMOS device. This is another reason for speed degradation of static CMOS gates. The CMOS design style is not area efficient for complex gates with large fan-ins hence care must be taken when a static logic style is selected to realize a logic function. Moreover, the layout of complementary CMOS circuit is straightforward and area-efficient due to the complementary transistor pairs and smaller number of interconnecting wires.

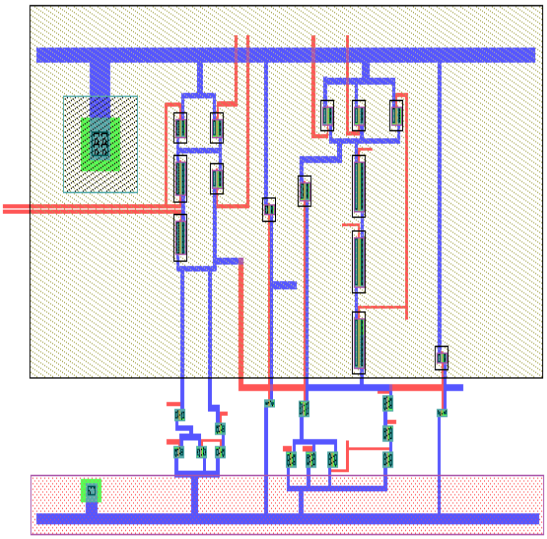

Fig. 4.1 Layout of CMOS Full Adder

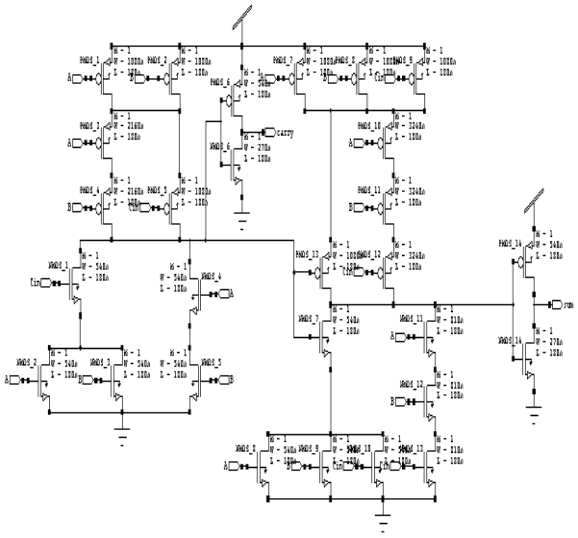

Fig 4.2 Schematic diagram of CMOS full Adder

B. Transmission Gate Full Adder (TGA)

The transmission gate CMOS full adder has 20 transistors and is based on transmission gates. The layout of transmission gate full adder is shown in Fig. 4.3. And Fig 4.4 shows its schematic diagram. Transmission gate full adder produces buffered outputs of proper polarity for both sum and carry. The circuit is simpler than the conventional full adder. It uses complimentary properties of NMOS and PMOS transistor. It is built by connecting a PMOS transistor and an NMOS transistor are in parallel, and Both the PMOS and NMOS field effect transistors will gives the path to the input logic "one(1)" or "zero(0)", respectively, when they are turned ON simultaneously. Thus, there is zero voltage drop problem whether the 1 or the 0 is passed through it. These adders are inherently low power consuming and are good for designing XOR or XNOR gates.

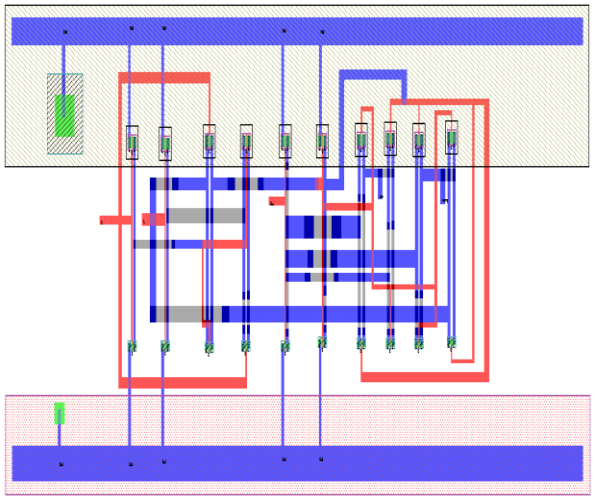

Fig. 4.3 Layout of Transmission Gate Full Adder

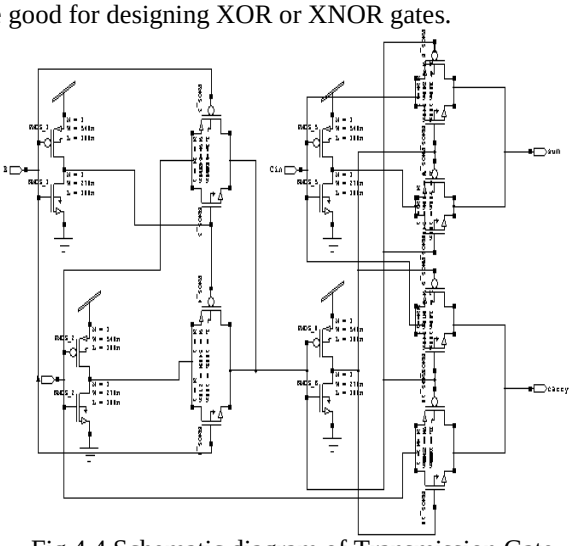

Fig 4.4 Schematic diagram of Transmission Gate Full Adder

C. Complementary Pass Transistor Logic Full Adder (CPL)

The complementary pass transistor logic full adder has 32 transistors and is based on the CPL logic. The layout of CPL logic full adder is shown in Fig. 4.6 and 4.7. And schematic diagrams are shown in the Fig 4.8 and Fig 4.9. In the circuit of CPL, two small pull-up PMOS transistors for swing restoration in the Sum output signal and the complementary Sum output signal, and another two small pull-up PMOS transistors for swing restoration in the Carry output signal and the complementary carry output signal [5]. CPL full adder gives high-speed, full-swing operation and very good driving capabilities due to the output static inverters and fast differential stage of cross coupled PMOS transistors.

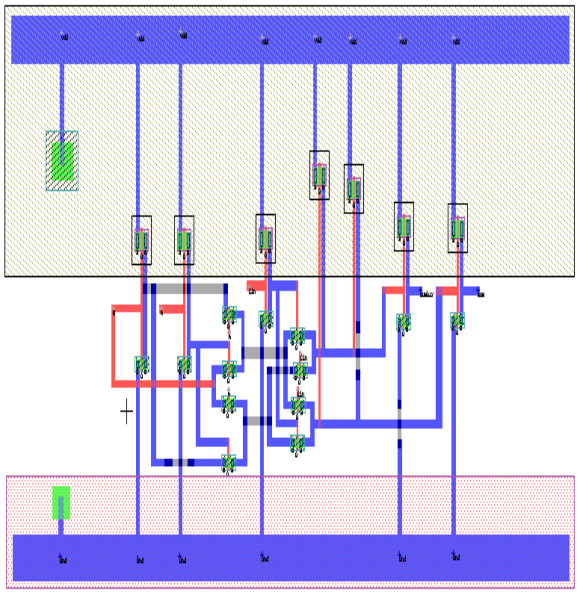

Fig. 4.6 Layout of CPL Sum

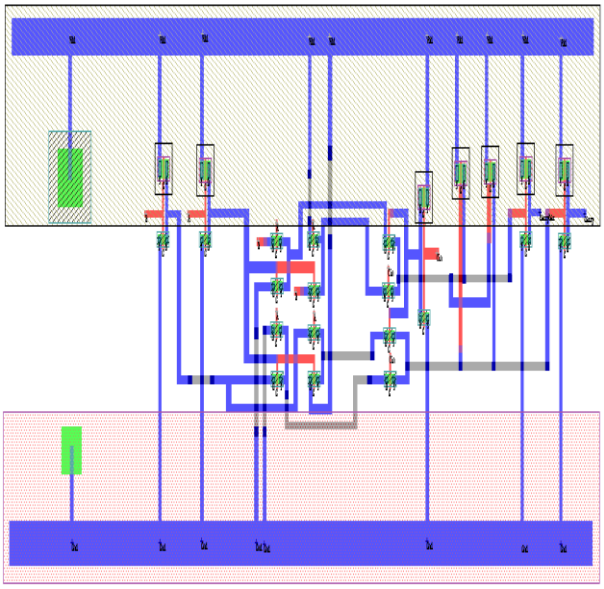

Fig. 4.7 Layout of CPL Carry

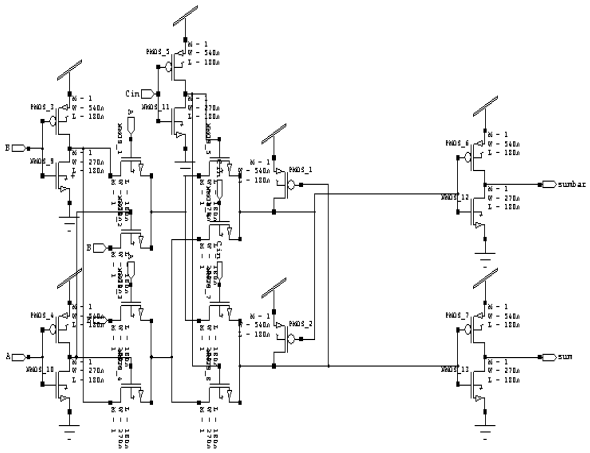

Fig 4.8 Schematic diagram of CPL full adder

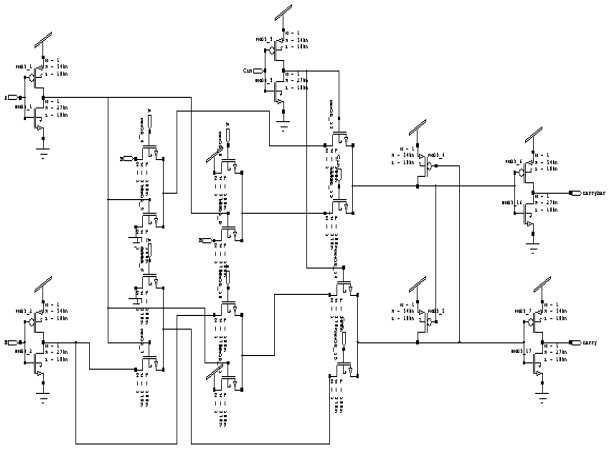

Fig 4.9 Schematic diagram of CPL full adder

D. Process for Layout Optimization Techniques

The Layout Versus Schematic check insures that the patterns accurately represent the desired circuit. The tool set is used to extract a circuit schematic from the layout drawings. This provides a listing of every electronic element and the wiring details; the parasitic resistance and capacitance of every line can also be determined. The extracted file is used to simulate the electronic behaviour of the silicon circuit [3]. This simple overview shows that physical design is dependent on every level of the design hierarchy. The shapes and sizes of the material layers created in the layout process determine how much of the final electrical characteristics of the fabricated chip. It is therefore considered to be a critical part of the design hierarchy. The layout must pass a series of checks in a process, known as verification, for its correctness. The two most common checks in the verification process are Design Rule Checking (DRC) and Layout Versus Schematic (LVS).

E. Design Rule Check (DRC)

Design Rule Check is the area of Electronic Design Automation that determines whether a particular chip layout satisfies a series of recommended parameters called Design Rules. Design Rule Check is a major step during Physical Verification of the design, which also involves Layout Versus Schematic. Design rules are a set of parameters provided by the semiconductor manufacturer that gives the designer to verifying the correctness of the mask set. Design rules are specific to a semiconductor manufacturing process [1]. The design rule verification step checks that all polygons and layers from the layout database meet all of the manufacturing process rules. A design rule set specifies a minimum size or spacing requirements between the layers of the same type or of different types of layers. This gives a safety margin for all various process variations, to ensure that the design will still have reasonable performance after the circuit is fabricated. The main objective of Design Rule Check is to achieve a high overall yield and reliability for the design. If the design rules are violated the design may not be functional. If the specific components that will interface or be adjacent to our design are available, we perform a DRC check with this interface cell included. If our cell is a general purpose design, then a more intricate and exhaustive check should be performed, perhaps including all possible interface cells as well as different orientations and combinations that may occur. These approaches really eliminate the possibility of errors as our design is integrated into the overall chip.

F. Layout versus Schematic (LVS)

The Layout Versus Schematic is the class of Electronic Design Automation verification software that determines whether a particular integrated circuit layout corresponds to the original schematic of circuit diagram of the design. LVS verification is checking that the design is connected correctly. The schematic is the reference circuit and the layout is checked against it. A successful Design Rule Check ensures that the layout fulfil to the rules required for faultless fabrication process. However, it does not have any guarantee if it really represents the circuit we desire to fabricate [1]. This is where an LVS check is used. LVS checking software identifies the drawn shapes of the layout that represent the circuit's electrical components, as well as the connections between those components. In principle, the following is verified:

- Electrical connectivity of all signals (input, output, and power signals) to their corresponding devices.
- Device sizes: transistor width and length, resistor sizes, capacitor sizes.
- Identification of signals and extra components that have not been included in the schematic layout design.

G. Layout Optimization Techniques

- First Stroke: The designing of basic transistor layout for maximum amount of current flow through the contacts.
- Second Stroke: For better manufacturing and for good performance compact the transistor layout.
- Third Stroke: Speed up the transistor for reducing the parasitic capacitance and resistance would increase the speed of the transistor.
- Fourth Stroke: to increasing the performance in analog design clean up the Substrate Disturbances.
- Fifth Stroke: Area, balancing Area, Speed and Noise to reducing the numbers of local N-well guard rings and P-diffusion guard rings.
- Sixth Stroke: Relief the Stress for reducing the Shallow Trench Isolation (STI).
- Seventh Stroke: Protect the Gate from the process of antenna effect.
- Eighth Stroke: Improve Yield for compact the layout.

VI. Results

Simulation analysis of various full adder topologies using 0.18µm technology node:

A. Simulation result of CMOS Full Adder

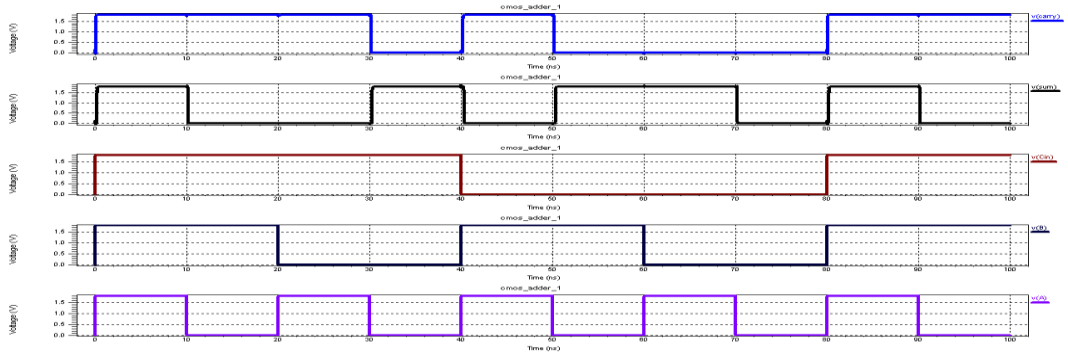

Fig. 5.1.Input and Output waveforms of CMOS Full Adder

B. Simulation result of Transmission Gate Full Adder (TGA)

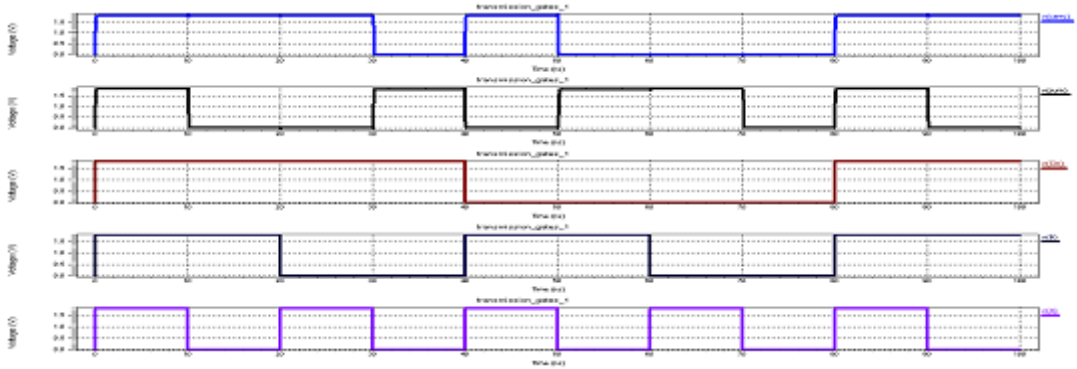

Fig 5.2 Input and Output waveforms of Transmission Gate Full Adder

C. Simulation result of Complementary Pass Transistor Logic Full Adder (CPL)

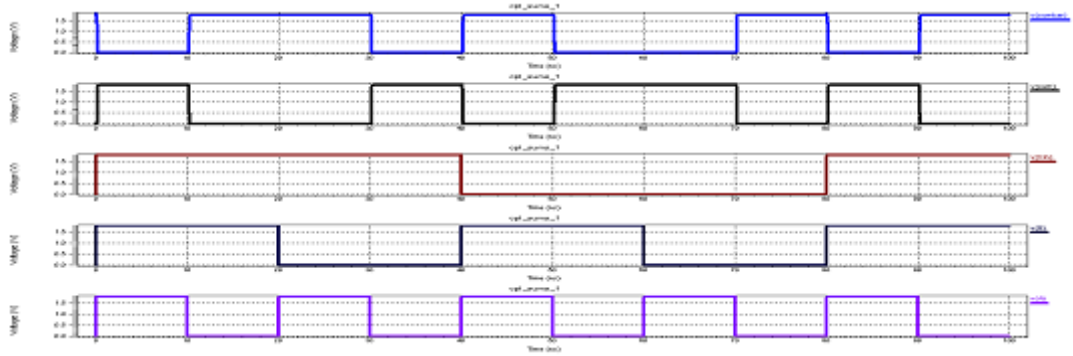

Fig.4.3.1. Input and Sum Output waveforms of CPL Full Adder

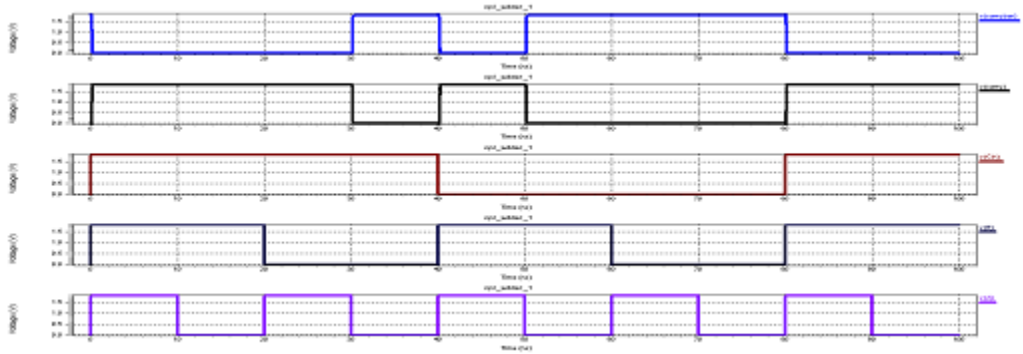

Fig. 4.3.2.Input and Carry Output waveforms of CPL Full Adder

Table A. Comparison of various parameters of different types of Adder

FULL ADDER TYPE	DYNAMIC POWER DISSIPATION (in watts)	STATIC POWER DISSIPATION (in watts)	PROPAGATION DELAY SUM (in sec)	PROPAGATION DELAY CARRY (in sec)
CMOS	7.98E-06	1.98E-10	1.74E-10	1.02E-08
TGA	2.07E-06	1.89E-10	5.90E-11	1.02E-08
CPL	4.14E-06	2.58E-10	1.76E-10	1.02E-08

VII. Conclusions

A main contribution of this paper is the designing of layout designing for Full adder topologies at 0. 18µm technology node by using efficient layout optimization techniques and mask layers are drawn using a layout editor tool according to the layout design rules. Therefore, the method give low Dynamic and Static Power consumption and total propagation delay. From the simulation results it is observed that Transmission Gate Full Adder is the most efficient adder since it has the minimum delay and power dissipation. As a result it is the fastest adder among CMOS, CPL and TGA.

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