IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 4, Issue 5, Ver. I (Sep-Oct. 2014), PP 54-59
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Delay-Power Performance of High Speed Radix 32 Booth Multiplier in 40nm Process Technology

[1]Er.Jatinder Pal Singh, [2]Prof.RupinderKaur, [3]Prof.Vishal Mehta
[1.] *Department of Electronics & Communication Engineering, UCOE, Punjabi University, Patiala, Punjab*
[2.] *Department of Electronics & Communication Engineering, UCOE, Punjabi University, Patiala, Punjab*
[3.] *Department of Electronics & Communication Engineering, Surya World, PTU, Jalandhar, Punjab*

Abstract: *Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation This thesis looks into the design and simulations of 32 bit booth multiplier with high speed carry select adder in 40 nm process technology and effect of temperature on power consumption. Process level simulation has been carried out on Xilinx suite 12.3.1 and Model -sim. For Investigation about Power, X Power Analyser is used which shows variation of power with respect to temperature.*

Keywords:*DSP, CSLA, RCA*

I. Introduction

Multipliersplay an important role in today's digital signal processing and variousother applications. Withadvances in technology, manyresearchers have tried and are trying to design multiplierswhichoffereither of the following design targets – high speed, low power consumption, regularity of layout and henceless area or evencombination of them in one multiplier thusmakingthemsuitable for varioushigh speed, low power and compact VLSI implementation. The common multiplication methodis "add and shift" algorithm. In parallelmultipliersnumber of partial products to beaddedis the main parameterthatdetermines the performance of the multiplier. To reduce the number of partial products to beadded, Modified Booth algorithmis one of the mostpopularalgorithms. To achieve speed improvements Wallace Treealgorithmcanbeused to reduce the number of sequentialadding stages. Further by combiningbothModified Booth algorithm and Wallace Tree technique wecanseeadvantage of bothalgorithmsin one multiplier. Howeverwithincreasingparallelism, the amount of shifts between the partial products and intermediatesums to beaddedwillincreasewhichmayresult in reduced speed, increase in silicon area due to irregularity of structure and alsoincreased power consumption due to increase in interconnectresultingfromcomplexrouting. On the other hand "serial-parallel"multipliers compromise speed to achievebetter performance for area and power consumption. [1][2]

Booth's Multipication Algorithm

Booth's Multiplication Algorithm Is A Multiplication Algorithm That Multiplies Two Signed Binary Numbers In Two's Complement Notation. The Algorithm Was Invented By Andrew Donald Booth In 1950 While Doing Research On Crystallography At Birkbeck College In Bloomsbury, London. Booth Used Desk Calculators That Were Faster At Shifting Than Adding And Created The Algorithm To Increase Their Speed .[4]

The Algorithm-

Booth's algorithm examines adjacent pairs of bits of the N-bit multiplier Y in signed two's complement representation, including an implicit bit below the least significant bit, $y_{-1} = 0$. For each bit y_i, for i running from 0 to N-1, the bits y_i and y_{i-1} are considered. Where these two bits are equal, the product accumulator P is left unchanged. Where $y_i = 0$ and $y_{i-1} = 1$, the multiplicand times 2^i is added to P; and where $y_i = 1$ and $y_{i-1} = 0$, the multiplicand times 2^i is subtracted from P. The final value of P is the signed product[5].

The multiplicand and product are not specified; typically, these are both also in two's complement representation, like the multiplier, but any number system that supports addition and subtraction will work as well. As stated here, the order of the steps is not determined. Typically, it proceeds from LSB to MSB, starting at i = 0; the multiplication by 2^i is then typically replaced by incremental shifting of the P accumulator to the

right between steps; low bits can be shifted out, and subsequent additions and subtractions can then be done just on the highest N bits of P.

To speed up the multiplication Booth encoding performs several steps of multiplication at once. Booth's algorithm takes advantage of the fact that an adder subtractor is nearly as fast and small as a simple adder. [6]

From the basics of Booth Multiplication it can be proved that the addition/subtraction operation can be skipped if the successive bits in the multiplicand are same. If 3 consecutive bits are same then addition/subtraction operation can be skipped. Thus in most of the cases the delay associated with Booth Multiplication are smaller than that with Array Multiplier. However the performance of Booth Multiplier for delay is input data dependant. In the worst case the delay with booth multiplier is on per with Array Multiplier .

The method of Booth recording reduces the numbers of adders and hence the delay required to produce the partial sums by examining three bits at a time. The high performance of booth multiplier comes with the drawback of power consumption. The reason is large number of adder cells required that consumes large power but lesser then other multipliers.

Problems In Designing High Radix Multiplier

1. Less operating power high performance multipliers have become a basic building block in computations especially in digital signal processing.. Multiplication process consumes most of the power.

2 .Low-power multipliers are required in modern DSP systems to reduce the power dissipation. To achieve high execution speed, parallel array multipliers are widely used. Most of the designs are targeted at a specific technology and require redesign for a new process technology.

Proposed Topology

To implement 32 Bit Efficient Booth Multiplier Using High Speed carry select adder in 40 nm Process Technology.

Carry Select Adder

CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and cin=1, then the final sum and carry are selected by the multiplexers (mux). The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.[7]

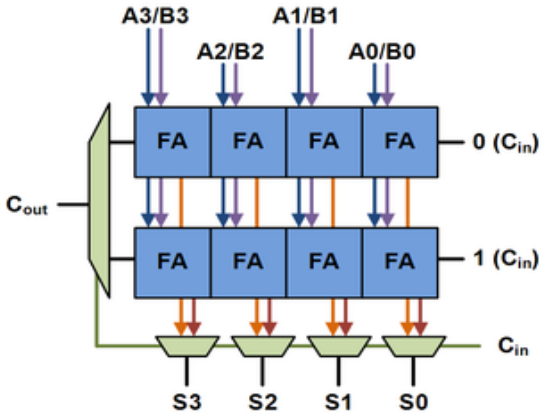

Figure.1 Concept of carry Select adder

Above is the basic building block of a carry-select adder, where the block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result.[8][9]

II. Result & Discussions

To implement 32 Bit multiplier coding have been done in VHDL. The processlevel simulation have been synthesizedusingXilinx 12.3.1i software. For the purpose of simulation Modelsim -6.3 isused.

Design Of Proposed Multiplier-

Figure 2 .design of carry select adder module in 32 bit multiplier

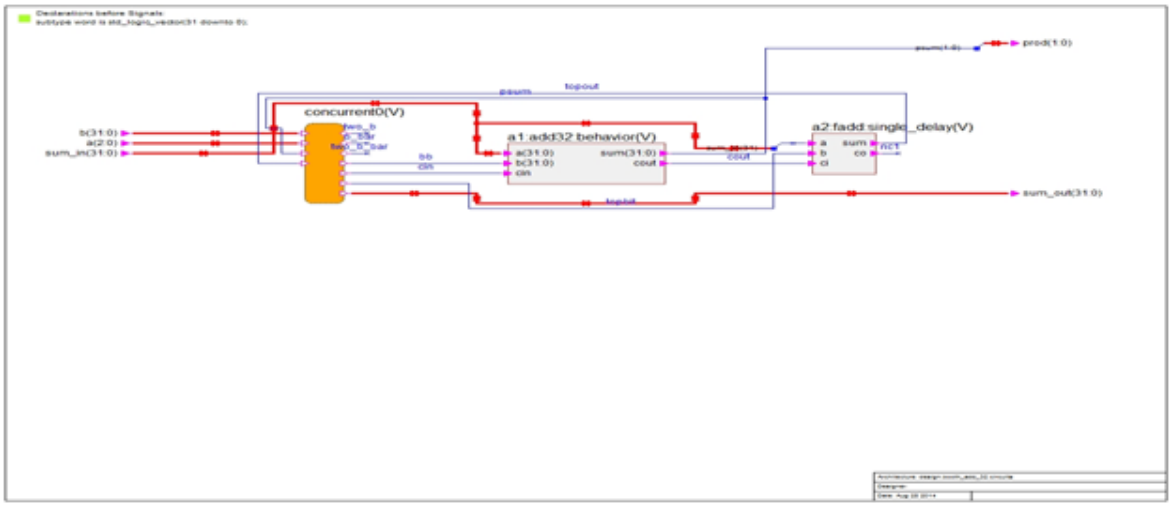

Figure3.design of carry select adder module in 32 bit multiplier

This Table shows comparison of Power consumptions and combinational path delay of 32 bit multiplier in 40 nm process technology at different temperature conditions.

COMPARISON OF POWER			
S.NO	TEMP(DEGREE CELSIUS)	POWER@90NMTECHNOLOGY(W)	POWER@40NMTECHNOLOGY(W)
1	53	0.162	1.008
2	50	0.158	0.984

3	45	0.152	0.948
4	40	0.147	0.931
5	35	0.142	0.881
6	30	0.137	0.851
7	25	0.133	0.822

CALCULATION OF COMBINATIONAL PATH DELAY			
1.	COMBINATIONAL PATH DELAY	90 NM TECH(VIRTEX4)	40 NM TECH(VIRTEX6)
		30.784 NS	27.674 NS

Table.1. Comparison of delay and power at different process technology

RTL VIEW

Thesediagram shows RTL view of design-

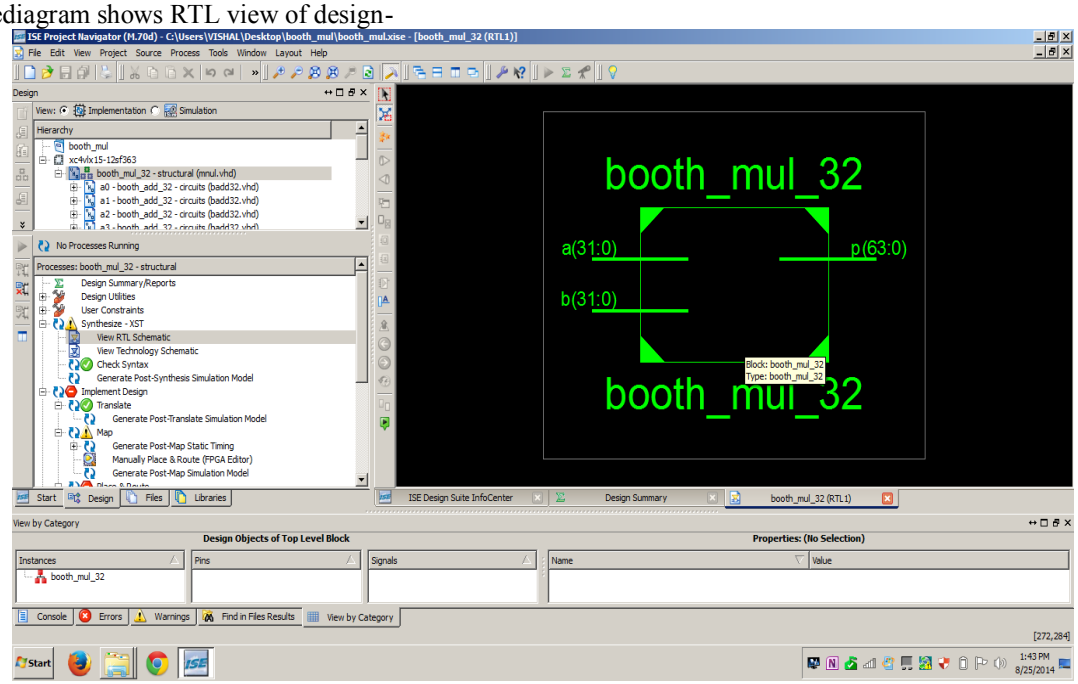

Figure.4.RTL view of proposed design

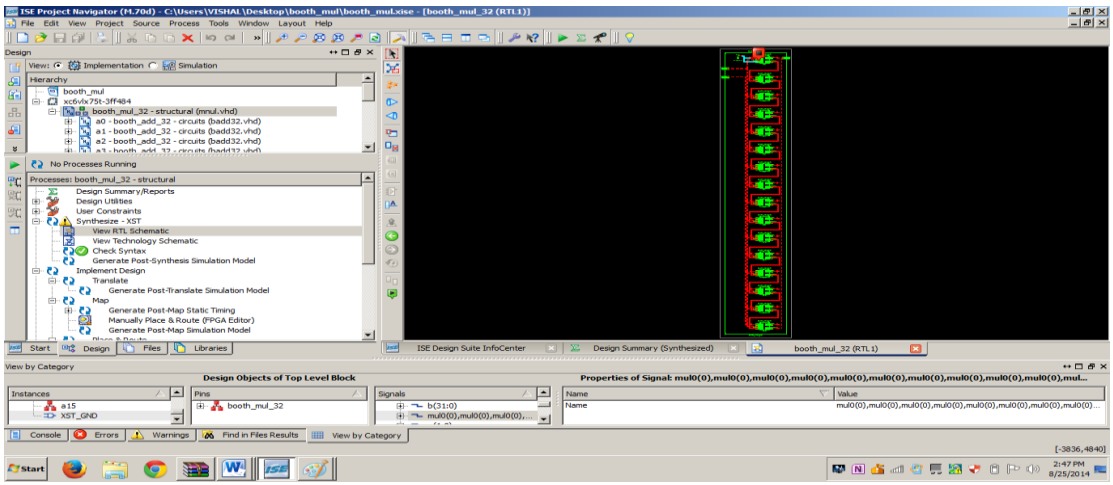

Figure.5.Expanded view of proposed design

Below are the graphs showing variations of power consomption and combinationalpathdelay in twotechnology.

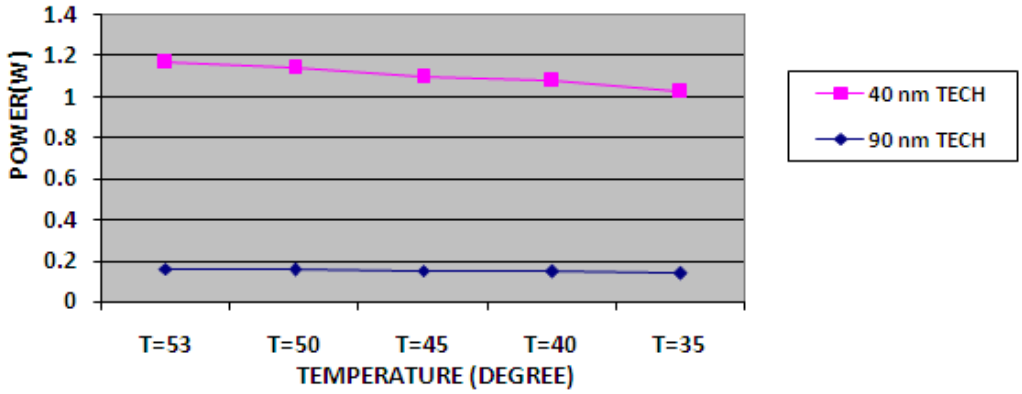

Figure.6. Comparison of power

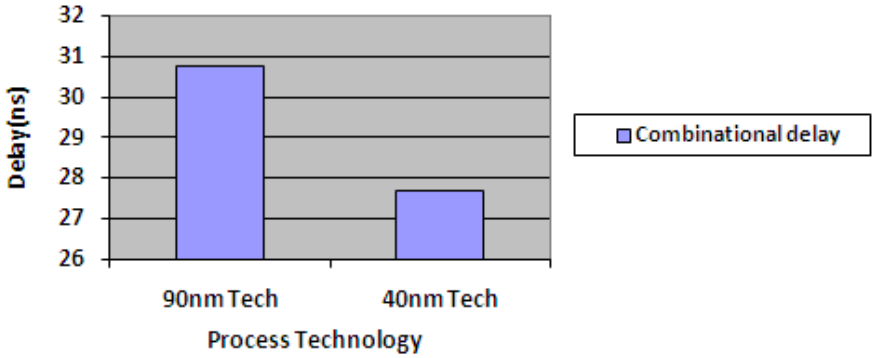

Figure.7. Comparison of delay

This figure shows simulation result of 32 bit multiplier.

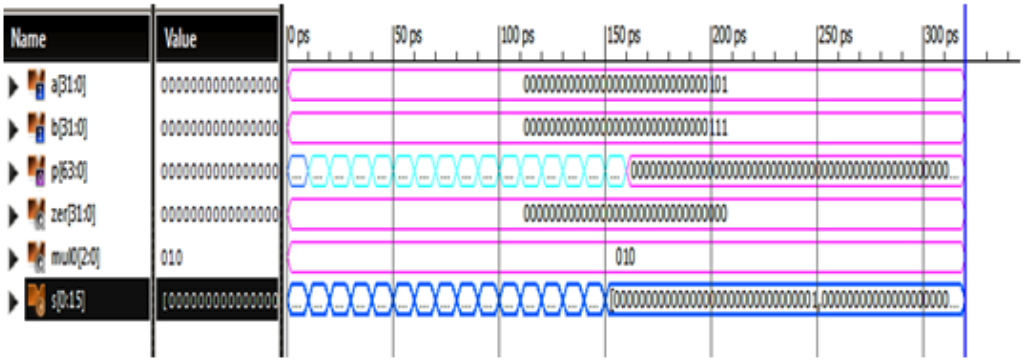

Figure.8.simulation result

III. Conclusion

Power-Efficient design of Booth Multiplier has been simulated by Xilinx suite and investigate the effect of temperature on Power Consumptionatdifferentambientconditions . It isclearlyshownthat as we change temperaturefrom 53 degree to 25 degree power in 40 nm as compared to 90 nm technology Power increases but combinationalpathdelayreduces to 27.674 ns from 30.784 ns whichisimprovementwith respect to solid state designing.

Refrences

[1]. Er. Neha Gupta, Dr. B K Sharma "EMPIRICAL REVIEW OF LOW POWER COLUMN BY PASS MULTIPLIER" International Journal of Computing and Corporate Research ISSN (Online): 2249-054X, Volume 4, Issue 3 May 2014, International Manuscript ID : 2249054XV4I3052014-19

[2]. RubiChoubey, Md. Arif "AREA OPTIMIZED AND LOW POWER USING MODIFIED BOOTH MULTIPLIER FOR UNSIGNED NUMBERS" International Journal of Emerging Science and Engineering (IJESE) ISSN: 2319–6378, Volume-2, Issue-6, April 2014

[3]. Amita P. Thakare, SaurabhAgrawal, VibhaTiwari "32 BIT CARRY SELECT ADDER WITH BEC-1 TECHNIQUE" Proceedings of Sixth IRAJ International Conference, 6th October 2013, Pune, India. ISBN: 978-93-82702-32-0

[4]. Naveen Kumar, Manu Bansal, AmandeepKaur "SPEED POWER AND AREA EFFICENT VLSI ARCHITECTURES OF MULTIPLIER AND ACCUMULATOR" International Journal of Scientific & Engineering Research Volume 4, Issue 1, January-2013 ISSN 2229-5518

[5]. Shweta S. Khobragade and Swapnili P. Karmore "LOW POWER VLSI DESIGN OF MODIFIED BOOTH MULTIPLIER" Int. J. on Recent Trends in Engineering and Technology, Vol. 9, No. 1, July 2013.

[6]. DhanyaGeethanjaliSasidharan ,AarathyIyer "COMPARISON OF MULTIPLIERS BASED ON MODIFIED BOOTH ALGORITHM" International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 3, Issue 1, January -February 2013, pp.1513-1516

[7]. N. Ravikumar, M.Vishwanath&B.DurgaMalleswara Reddy "AN AREA EFFICIENT 32-BIT CARRY-SELECT ADDER FOR LOW POWER APPLICATIONS" International Journal of Computer & Communication Technology (IJCCT), ISSN (ONLINE): 2231 - 0371, ISSN (PRINT): 0975 - 7449 ,Vol.-3 , Issue - 4 , 2012

[8]. I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng "AN AREA-EFFICIENT CARRY SELECT ADDER DESIGN BY SHARING THE COMMON BOOLEAN LOGIC TERM" Proceedings of the International Multi Conference of Engineers and Computer Scientists 2012 Vol II, IMECS 2012, March 14 - 16, 2012, Hong Kong

[9]. SumitVaidya and Deepak Dandekar "DELAY-POWER PERFORMANCECOMPARISON OF MULTIPLIERS IN VLSI CIRCUIT DESIGN" International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010