A Study on Programmable System on Chip

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Abstract: *PSOC (Programmable System-on-Chip) is a family of integrated circuits made by Cypress Semiconductor. These chips include a CPU and mixed-signal arrays of configurable integrated analog and digital peripherals. A PSoC integrated circuit is composed of a core, configurable analog and digital blocks, a software configured and programmable routing and interconnect.*
Keywords: *PSoC Designer, PSoC Creator, PSoC 3/5, microcontrollers, Capacitive Sensor, Thermistor, 24 External pins for output.*

I.   Introduction

After the invention of the transistor in 1948 there is a huge change in the number of the devices or we can say number of the electronic components on the circuit board. As the time passes there is a reduction in the manner of size of the components but the number of the components or we can say transistors are increasing as when the first integrated circuit came in 1957. That technology was called small scale integration. After this concept of the reduction in size of transistor and increment in numbers, today gives us ultra large scale integration technology where billions of the transistors place on the small circuit board and it consumes very less power.

In 1968 the first embedded system invented at MIT Draper Lab, Boston. The embedded system is the combination of the hardware components and the firmware (software). The embedded system is use for a particular application or we can say for a particular control operation. Similarly in 1968 the application specific integrated circuit (ASIC) invented by Mead Conway and in 1982 the first field programmable gate array (FPGA) invented through the Xilinx. After these technologies there is a more compatible technology comes into true when Mr. T.J. Rodgers invented the first programmable system on the chip (PSOC) by which the analog as well as digital components place on a single circuit board and the consumer uses the both analog and digital components and reprogram the microcontroller as the requirements of applications to both analog and digital type signals that is why it is also called mixed signal programming.

When we compare above technologies then we found the FPGA is less expensive than ASIC. When there is requirement of these both then FPGA designed in lab but ASIC designed outside the lab. Due to this reason FPGA is lower cost & lower performance technology and ASIC is higher cost & higher performance technology also ASIC is most versatile. Whereas PSOC and FPGA are quite versatile, also PSOC is less expensive than average FPGA and embedded system is the lowest cost technology. In embedded system we program on the software side only but PSOC has the advantage of programmability and we can program on the hardware side. PSOC not works with high frequency or RF signals.

Except this PSOC is an exponential disruptive technology because of the mixed signal capability. Mixed signal programmability is unique because it is universal and it is more difficult to implement before PSOC concept that is why it is a domain of Cypress. Mixed signal programmability is of a limited performance because of switching challenge. Mixed signal programmability is failed in ASIC.

II.   PSoC Family

At present there are three different families of PSOC devices i.e. 'PSoC 1' with CPU M8C, 'PSoC 3' with CPU 8051 and 'PSoC 5' with CPU ARM Cortex M3.

It also has three separate memory spaces: SRAM for data, Flash memory for instructions and fixed data and I/O Registers for controlling and accessing the configurable logic blocks and functions. PSoC Designer for PSoC 1 and PSoC Creator for PSoC 3 and PSoC 5 generate the start-up configuration code. Both integrate APIs that initialize the user selected components upon the user's needs in a Visual-Studio-like graphical user interface (GUI). PSoC 5 is the newest disruptive technology. Because PSocC 5 is ARM based hence it is most powerful and the design tools of PSoC 5 are compatible with PSoC 3.

2.1 PSoC 1

PSoC 1 is the original design and it has an 8 bit M8C core which perform 4 million instructions per second (MIPS). PSoC 1 is available since 2001. It is a simple device for LED lighting and motor control. It has high current FETs on board which are in the range of about1Ampere.

2.2 PSoC 3

PSoC 3 is a redesign kit of development tool chain. In this the analog blocks are also redesigned to better performance and handling. PSoC 3 has enhanced 8051 core which performs 33 MIPS. The PSoC 3 production parts are available since December 2010.

2.3 PSoC 5

PSoC 5 has the mostly same base architecture as PSoC 3. But it has 32 bit ARM Cortex M3 core powerful processor which performs 100 MIPS. The production of PSoC 5 starts since second quarter of 2011.

Above PSoC kits have good balance of processor, analog blocks and digital blocks. These have single chip solution for many designs. PSoC kits are also easily programmable in 'C' or assembly language and 'C' is the default language to PSoC kits. Development tools for PSoC are free and easily download from the PSoC official website. These are PSoC Creator and PSoC Programmer. Both are using the C – compiler in which Keil for PSoC3 and GCC for PSoC5. Here only a recompile needed in many cases.

The creator or designer have prebuilt components. In creator and designer these hardware components normally combined to make what you need for your application from a large library of prebuilt components. Each component consists of hardware specifications in graphical mode or VHDL mode. These components have schematic symbol for graphical editor, 'C' API, datasheet and custom configuration dialog.

III.   Platform Architecture

The PSoC devices mainly have four blocks which are processor block, analog subsystem block, digital subsystem block and interfacing block as shown in figure 1.
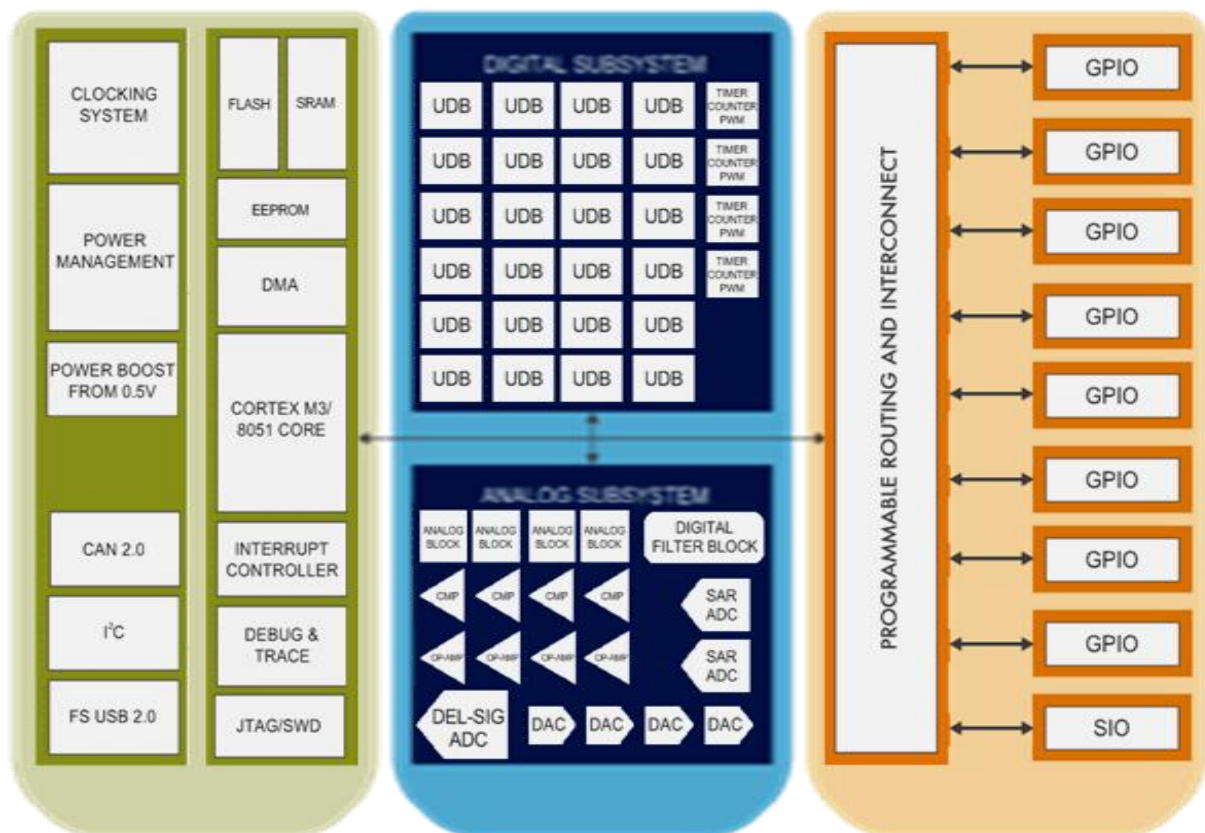
Fig. 1 PSoC 3/5 platform architecture

3.1 CPU Subsystem

ARM is industries leading embedded CPU Company. It provides broad support for middleware and applications. ARM Cortex M3 processor works upto 80 MHz with 100 MIPS. It has enhanced v7 ARM architecture. This processor is able to execute thumb2 instruction set of 16- and 32-bit instructions. It has 32-bit ALU, Hardware multiply and divide unit, single cycle 3-stage pipeline and Harvard architecture. Whereas 8051 processor works upto 67 MHz with 33 MIPS and it is a single cycle instruction execution machine.

3.2 High Performance Memory and DMA Engine

8051 have two types of data spaces. Internal Data space (IDATA) is of 256 bytes of SRAM where standard 8051 specific SFR registers are present. The access port data registers through SFRs. External Data space (XDATA) is of 16 MB. Where upto 8 KB of SRAM on lead devices, all PSoC peripheral and configuration registers, EEPROM, flash memory and external memory interface (EMIF) are easily connect to PSoC kit. ARM Cortex M3 processor has single 4 GB address space where registers from 8051 map easily fit into 0.5 GB peripheral region's bit band region for efficient bit operations.

PSoC kit also has 24-channel direct memory access (DMA). By which it access all digital and analog peripherals. DMA provides direct memory transfer or direct data transfer path between peripheral without copy into internal memory space. Due to this the time is reduce in transferring the data also DMA off loads the CPU operations and lowering the power consumption. CPU and DMA simultaneous access to independent SRAM blocks.

3.3 Clocking System

PSoC has many clock sources as internal main oscillator, external clock crystal input, external clock oscillator inputs, clock doubler output, internal low speed oscillator which is used in sleep mode when everything is in the sink mode also PSoC has, external 32 kHZ crystal input, dedicated 48 MHz USB clock, PLL output. Here we get 496 different frequencies using PLL.
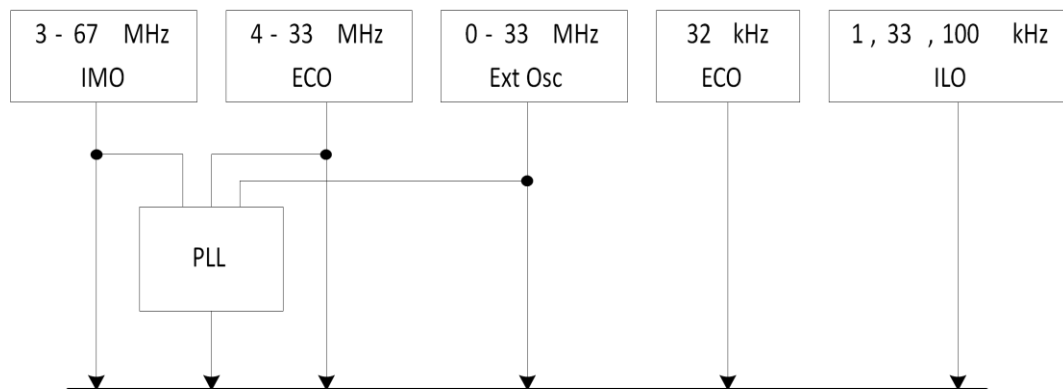
Fig. 2 Main clock sources

In addition PSoC has 16 bit clock dividers where 8 dividers are in digital domain and 4 in analog domain. Eight 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, as well as many others. If more than eight digital clock dividers are required then the Universal Digital Blocks (UDBs) and fixed function Timer/Counter/PWMs can also generate clocks. Four 16-bit clock dividers generate clocks for the analog system components that require clocking like ADCs and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise. In PSoC it is easy to configure clock options using graphical configuration tool as shown in figure 3.
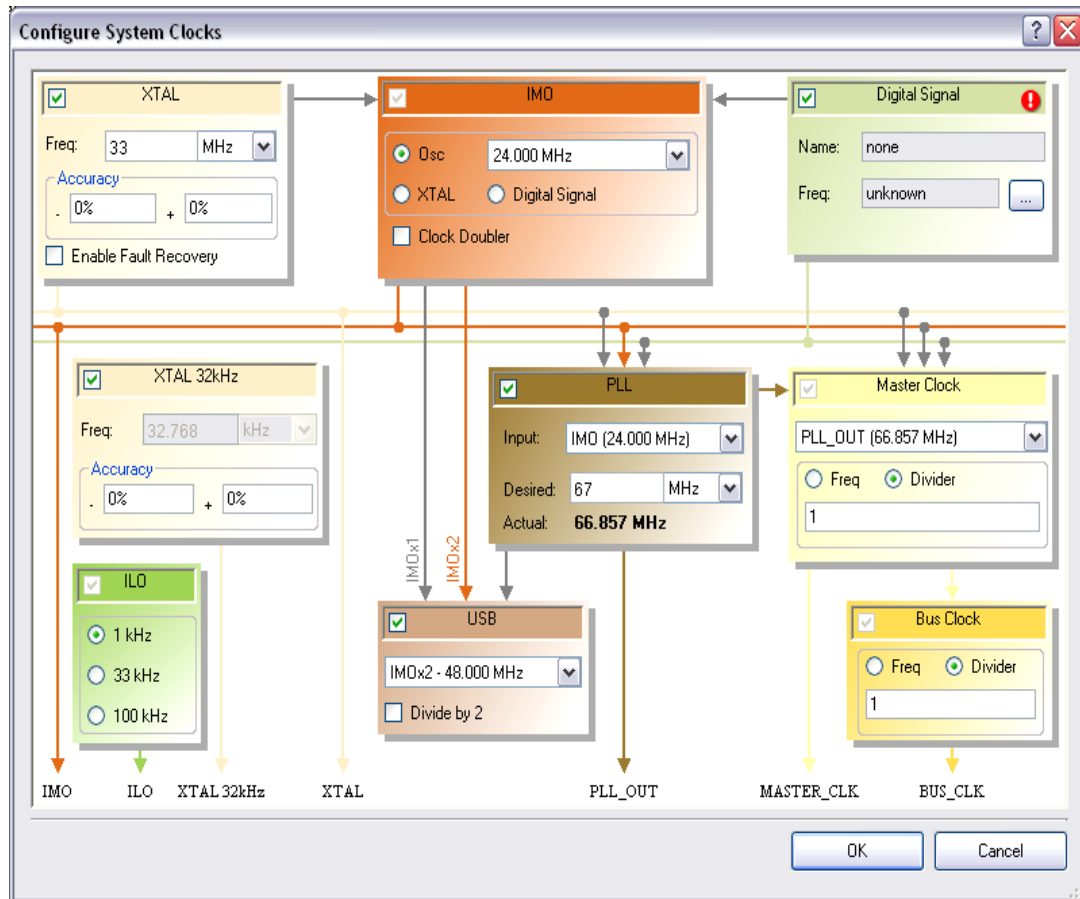
Fig. 3 System clocks configuration window

3.4 Power Management

PSoC has industries widest operating voltage from 0.5V to 5.5V with full analog/digital capabilities. We get high performance at 0.5V in PSoC 3 @ 67 MHz and in PSoC 5 @ 72 MHz we get voltage in between 0.5v to 2.7v and back up to 80MHz from 2.7v to 5.5v. There are 4 power modes as active, alternate active, sleep and hibernate.

3.5 Dedicated Communication Peripherals

PSoC has many types of dedicated peripherals as full speed USB device, full CAN 2.0b and I^2C master slave. Here USB device has 8 bidirectional data end points plus 1 control end point. For this no external crystal required also drivers are present in PSoC creator. CAN have 16 receiver buffers and 8 transmitter buffers for easily transmission or reception of the data. I^2C has transfer data rate up to 400 kbps and additional I^2C slaves may be implemented in UDB array. Also new peripherals will be added as family members are added to the platform like Ethernet, HS USB, and USB Host etc.

3.6 Universal Digital Blocks Array

UDB's provides hardware capability to implement components from a rich library of pre-built, documented and characterized components in PSoC creator. PSoC creator will synthesize, place and route components automatically. Here fine configuration granularity enables high silicon utilization. Digital signal interconnect (DSI) routing mesh allows any function in the UDBs to communicate with any other on-chip function or general purpose input output (GPIO) pin with 8- to 32-bit data buses.
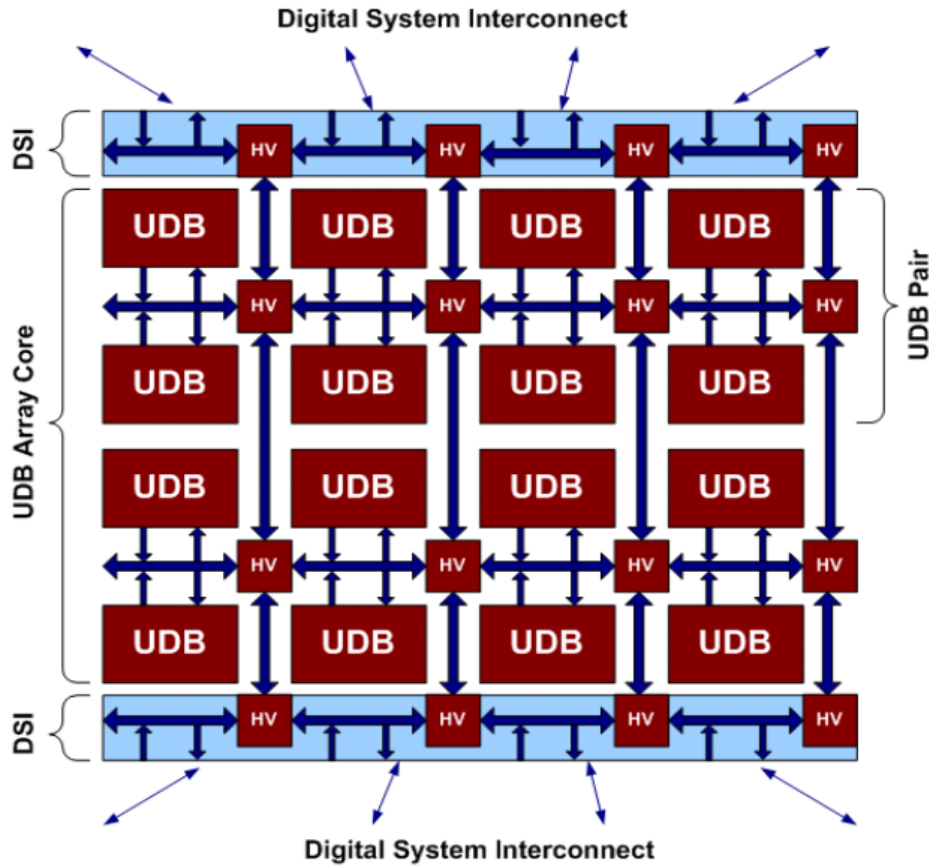
Fig. 4 UDB array architecture

As shown in figure 5 Each UDB block contains 2 PLD blocks where datapath is a programmable ALU. ALU has 8 bit single cycle with shift and mask operations. Also datapath have 2 accumulators, 2 data registers, 2 FIFO banks (4 bytes deep) and PLD usage can be decoupled from datapath which allows for more efficient resource mappings. PLD and datapath blocks can be chained for 16-32 bit operations.
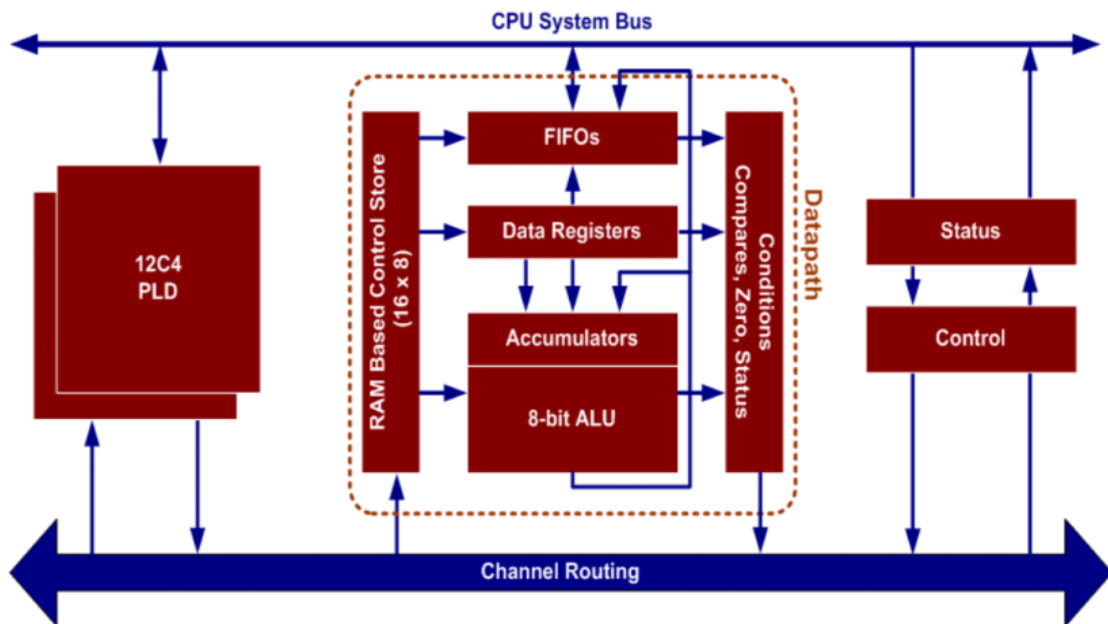

Fig. 5 Single UDB block diagram

3.7 Programmable Routing and Interconnect

PSoC has three types of input output system as general purpose input output (GPIO), serial input output (SIO) and universal serial bus input output (USBIO). Here any GPIO can be connected to any peripheral routing. Any bus or path is wakeup on analog, digital or I²C match. In PSoC programmable slew rate reduces power and noise by using 8 different configurable drive modes. PSoC provide programmable input threshold capability for SIO also auto and custom/lock-able routing is present in PSoC creator.

3.8 Optimized 16-bit Timer/Counter/PWM Blocks

PSoC provides nearly all of the features of a UDB based timer, counter, or PWM. For this PSoC creator provides easy access to these flexible blocks. Here each block may be configured as either a full featured 16-bit Timer, Counter, or PWM by using programmable options as clock, enable, reset, capture, kill from any pin or digital signal on chip also independent control of terminal count, interrupt, compare, reset, enable, capture, and kill synchronization. It can also configurable to measure pulse widths or periods.

3.9 Configurable Analog System

Some chips of PSoC present with lots or less analog systems. The PSoC3/5 architecture has a huge portfolio of analog IP. Exact configuration depends on the product family. PSoC provide flexible routing to all GPIO which are analog input/output, delta-sigma ADC up to 20-bit resolution

16-bit at 48 ksps or 12-bit at 192 ksps, ADC of 12-bit at 1 Msps, DACs of 8 − 10-bit resolution, low power comparators, Opamps of 25 mA, programmable analog blocks, configurable mixer, trans-impedance amplifier, sample and hold devices etc. In PSoC digital filter block implement HW IIR and FIR filters. Also CapSense Touch Sensing enabled on the board to provide easy access for functioning or controlling purpose.

CapSense support on all the GPIOs. In PSoC maximum of 61 sensors supported. For this sourcing, sinking is used by IDAC by which IDAC improves smaller errors on production testing and parasitic capacitance measurement range. An adjustable pre-charge clock is present in there. Here the two channel architecture reduces scan time, improved AC noise immunity and improved water tolerance using SIO as shield.
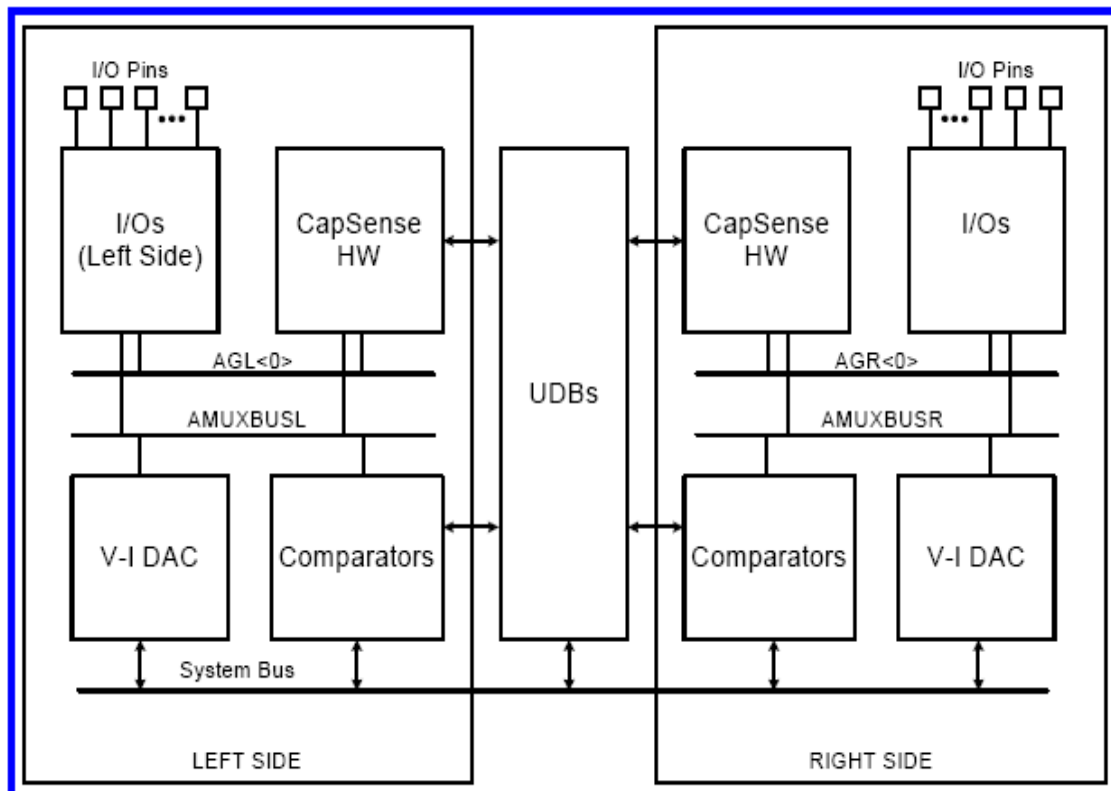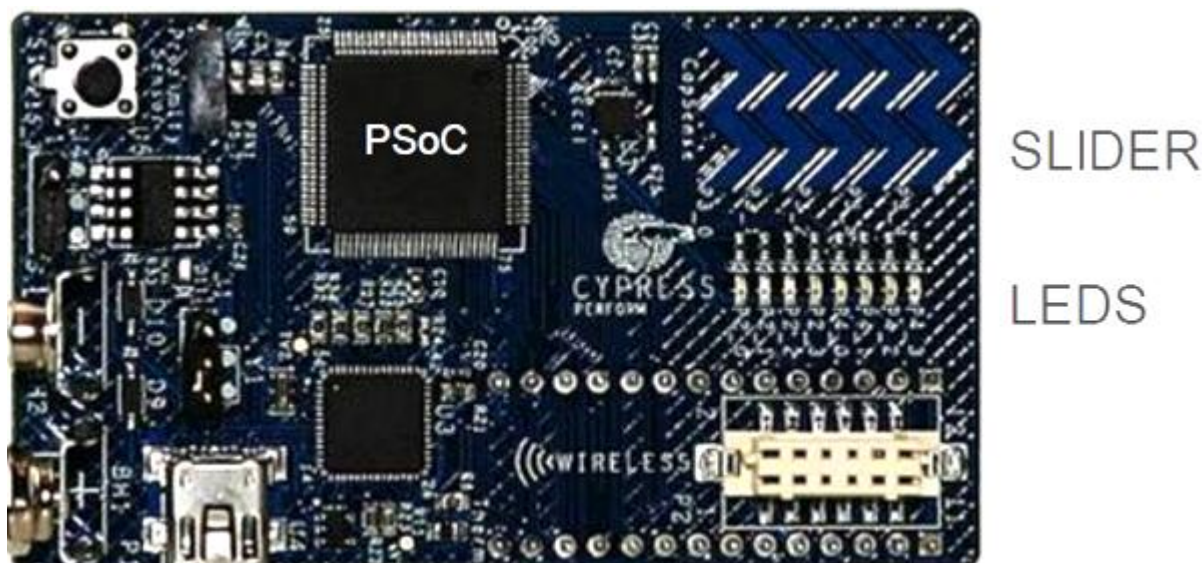

Fig. 6 Block diagram for capsense connection

Fig. 7 PSoC 3 kit

IV. Conclusion

By estimating the previous features of PSOC we found that it is a new disruptive technology which is able to works with analog devices or signals as well as with digital devices or signals or both on single kit. The programming to processor becomes easier due to graphical user interface feature. Also the capsense provide a extra feature in it because PSoC provides easily implementable robust and stylish solution for high-volume consumer markets like mobile phones, consumer electronics as implements buttons, sliders, track pads etc. After bulding the program in PSoC processor it works freely at the site of work for controlling or for detecting some input. PSoC can also control by CAN, Ethernet, WiMAX etc.

Acknowledgements

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