# Design of Low Power Carry Look-Ahead Adder Using Single Phase Clocked Quasi-Static Adiabatic Logic

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**Abstract:** *Efficiency of adiabatic circuits is determined by the adiabatic and non-adiabatic losses incurred by them during the charging and recovery operations. Lesser be the losses more energy efficient would be the circuit. In this paper, a new approach i.e., Complementary Energy Path Adiabatic Logic (CEPAL), is presented to minimize power dissipation in quasi static energy recovery logic (QSERL). It optimizes circuit, by avoiding non-adiabatic losses completely by replacing the diodes with MOSFETs. MOSFET gates are controlled by power clocks and this is implemented in Carry Look-Ahead Adder structure. Firstly, the performance attributes of CEPAL Carry Look-Ahead Adder are compared against the conventional static CMOS logic counterpart to identify its adiabatic power advantage. The analyses are carried out using the industry standard Tanner EDA design environment using 250nm technology libraries. The results prove that CEPAL adiabatic Carry Look-Ahead Adder results in 56.05% of power savings over static CMOS.*

**Keywords:** *Carry Look-Ahead Adder; CEPAL (Complementary Energy Path Adiabatic Logic); Low Power; Power Clock; Ripple carry adder; Static adiabatic logic; Very Large Scale Integration (VLSI)*

## I. Introduction

With the advancements in CMOS technology, chip capacity (transistor count) and clock frequencies have increased. As a result, the power dissipation in digital CMOS design has skyrocketed and now is a primary design constraint [1]. In earlier days, due to a high degree of process intricacy and the steep costs involved, low power circuit design was favored in applications where very low power dissipation was indispensable, but now it became the norm for all high-performance applications [2]. So, low power designs are highly valued in current VLSI systems.

This has inspired the designers to explore various design methodologies to reduce power dissipation in VLSI circuits. Adiabatic logic has been applied to low-power systems, and several adiabatic logic families have been proposed for low power applications [3]–[7]. Energy retrieval circuits based on the adiabatic logic have been proved to be a reliable method among non-conventional low power design approaches. The primary advantage of these circuits results from its intrinsic nature of developing a constant current from power-clock sources and making the Field Effect Transistor (FET) switches function with least voltage across the source and drain[8].

There are numerous types of static adiabatic logics, viz., Quasi Static Single-phase Energy Recovery Logic (QSSERL), Quasi Static Energy Recovery Logic (QSERL) and Complementary Energy Path Adiabatic Logic (CEPAL). These are intended to overcome the flaws of the irreversible adiabatic logics. These circuits use sinusoidal power-clocks to function and since the sinusoidal power-clock generation is flexible, it makes them apposite for energy recovery circuits [5, 9].

There are three types of losses in adiabatic circuits, i.e., non-adiabatic losses, adiabatic losses, and leakage losses. The last two losses are associated with fully adiabatic circuits, whereas non-adiabatic losses are related to quasi/semi-adiabatic circuits [10, 11]. Leakage losses are proportional to the clock period and are negligible in comparison to the other two and depend on current or voltage drawn from the source, load capacitance, charging path resistance, and transition time [12, 13]. Non-adiabatic losses can be eliminated using reversible logic. There are several remedies to reduce adiabatic losses. Some of them are by extending the charging time, constant current charging [14] for capacitance through a resistance in a given time. Another important mechanism for energy saving in adiabatic circuits is to recover the adiabatic losses which were stored in load capacitance during charging can be recovered again with a dissipation that depends inversely on charging time.

Section II briefly gives an introduction to CEPAL. The proposed structure of Carry Look-Ahead Adder and the details on how to implement it using CEPAL logic style is presented in Section III. Experimental results are given in Section IV, and this paper is concluded in Section V.

## II.     Complementary Energy Path Adiabatic Logic

A circuit of a single-stage Complementary Energy Path Adiabatic Logic circuit is shown in Figure 1 [15, 16]. CEPAL logic comprises an evaluation network and a power clock network. The power clock comprises of two P-type MOS transistors Pull-up P network and two N-type MOS transistors Pull down N networks. The evaluation network is a logic circuit composed of P- and N-type MOS transistors. The evaluation network, designed in accordance with the principle of a static complementary metal-oxide-semiconductor (CMOS) circuit, is used to perform evaluations based on the input signals and power clocks.

Each of the transistors involved in the power clock network acts as an active diode. The power clock input PC has its phase opposite to that of the complementary power clock input PCbar. These MOS transistors receive a power clock and an inverted complementary power clock, respectively. CEPAL achieves the evaluation in accordance with the power clock, the complementary power clock, and the inputs of the evaluation network.

Let us assume that the initial output $V_{out}$ is high, and the P network is on, while the N network is off, the output node will neither be following the power clock PC nor its complement $PC_{bar}$, when the next input does not warrant a change in the output node. Let us consider the alternate case, in which, the initial output $V_{out}$ is low and the P network is on, while the N network is off. Then, the output node $V_{out}$ follows either PC or its compliment $PC_{bar}$, whichever swings to high level. Once the output reaches high, it ramps down to low level following the power clock during its downward transition, thus making the node $V_{out}$ to become a floating node. However, this condition overcomes when the compliment of the power clock swings to high level. This eliminates the weak high node and also eliminates the hold state of the two phase power clock operated circuits.
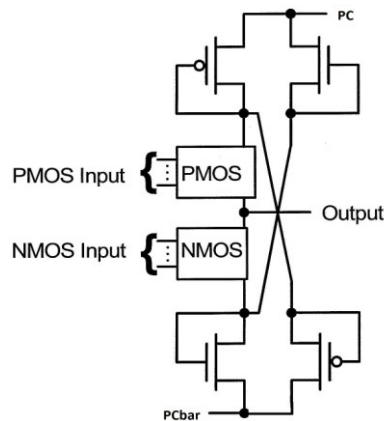


**Fig 1:** Complementary Energy Path Adiabatic Logic

## III.     Structure And Design Of Carry Look-Ahead Adder And Ripple Carry Adder

**3.1 Half adder**

The half adder adds two single binary bits A and B. It has two outputs, sum (S) and carry (C). The input variables of a half adder are called the augend and addend bits. The carry signal represents an overflow into the next digit of a multi-digit addition. The simplest half-adder design incorporates an XOR gate for S and an AND gate for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder. The structure of half adder is shown in the below figure.
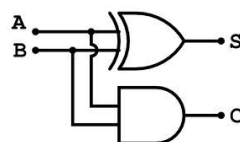


**Fig.2:** Logic Design of Half Adder

The number of transistors and the average power of the Half Adder using CMOS and CEPAL are shown in Table 1.
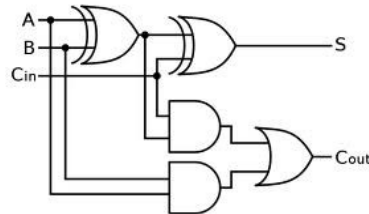
**Table 1:** Half Adder Transistor count & Power Comparison

| Logic | P-MOS | N-MOS | Total Transistors | Average Power (µW) |
|---|---|---|---|---|
| CMOS | 9 | 9 | 18 | 33.79 |
| CEPAL | 19 | 19 | 38 | 8.28 |

The CEPAL Half adder is 75.49% more power efficient as compared to its CMOS counterpart. Figure 4 shows the output waveforms of the CEPAL Half adder, where PC and PCbar are the two complementary power clocks. The plot p(VVoltageSource_4) shows the power dissipation of the power clock.

**3.2 Full adder**

A full adder adds binary bits and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and $C_{in}$; A and B are the operands, and $C_{in}$ is a bit carried in from the next less significant stage. The full-adder is usually a component in a cascade of adders. The circuit produces a two-bit output, that is, output carry and sum typically represented by the signals $C_{out}$ and S. The structure of half adder is as shown in the below figure.



**Fig.3:** Logic Design of Full Adder

The number of transistors and the average power of the Full Adder using CMOS and CEPAL are shown in Table 2.



**Fig.4:** Output waveforms of Half Adder

**Table 2:** Full Adder Transistor count & Power Comparison

| Logic | P-MOS | N-MOS | Total Transistors | Average Power (μW) |
|---|---|---|---|---|
| CMOS | 27 | 27 | 54 | 66.86 |
| CEPAL | 59 | 59 | 118 | 24.57 |

**Fig.5:** Output waveforms of Full Adder

The CEPAL Full Adder is found to be 63.25% power efficient as compared to the counterpart in CMOS technology. Figure 5 shows the output waveforms of the CEPAL Full Adder. Plot PC and PCbar show the power clock given. The plot p(VVoltageSource_4) shows the power consumption of the power clock.

**3.3 Ripple carry adder**

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a $C_{in}$, which is the $C_{out}$ of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that $C_{in} = 0$). The layout of a ripple-carry adder is simple, which allows for fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The structure of ripple carry adder is as shown in the below figure.
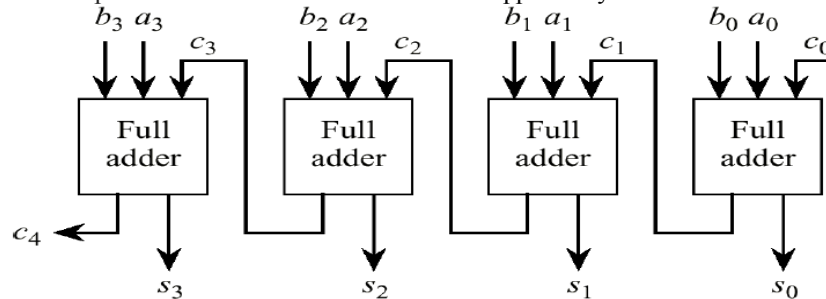


**Fig. 6:** Logic Design of Ripple Carry Adder

The number of transistors and the average power of the Ripple Carry Adder using CMOS and CEPAL are shown in Table 3.

**Table 3:** Ripple Carry Adder Transistor count & Power Comparison

| Logic | P-MOS | N-MOS | Total Transistors | Average Power (µW) |
|---|---|---|---|---|
| CMOS | 108 | 108 | 216 | 202.07 |
| CEPAL | 236 | 236 | 472 | 81.35 |

There is an increase in the number of transistors in the CEPAL technology; nevertheless, there is a significant decrease in power. The CEPAL Ripple carry adder is 59.74% more power efficient as compared to its CMOS counterpart. Figure 8 shows the output waveforms of the CEPAL Ripple carry adder, where PC and PCbar are the two complementary power clocks. The plot p(VVoltageSource_10) shows the power dissipation of the power clock.

**3.4 Carry Look-Ahead Adder**

A Carry Look-Ahead adder (CLA) is a type of adder used to improve speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits.
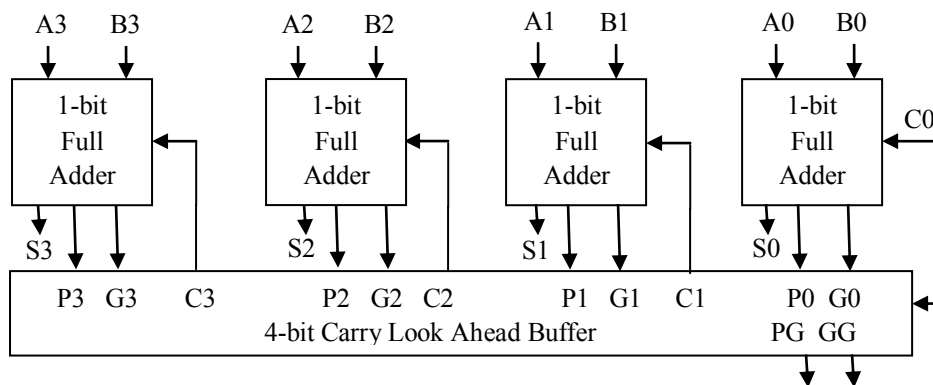


**Fig. 7:** Logic Design of Carry Look-Ahead Adder

The Carry Look-Ahead Adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits.
Consider a full adder circuit as shown in Figure 4.

$$P_i = A_i \oplus B_i \qquad (1)$$
$$G_i = A_i B_i \qquad (2)$$

Where, $G_i$ is carry generate and $P_i$ is carry propagate. The output sum and carry can be expressed as

$$S_i = P_i \oplus C_i \qquad (3)$$
$$C_{i+1} = G_i + P_i C_i \qquad (4)$$

$G_i$ produces on carry when both $A_i$ and $B_i$ are one, regardless of the input carry. $P_i$ is associated with the propagation of the carry from $C_i$ to $C_{i+1}$. Now the Boolean function for the carry output of each stage can be written as follows.

$$C_2 = G_1 + P_1 C_1 \qquad (5)$$
$$C_3 = G_2 + P_2 C_2 \qquad (6)$$
$$C_4 = G_3 + P_3 C_3 \qquad (7)$$

From the above Boolean function it can be seen that $C_4$ does not have to wait for $C_3$ and $C_2$ to propagate; in fact $C_4$ is propagated at the same time as $C_2$ and $C_3$. Using a look ahead carry generator we can easily construct a 4-bit parallel adder with a look ahead carry scheme which has been implemented using CMOS and CEPAL logic styles.
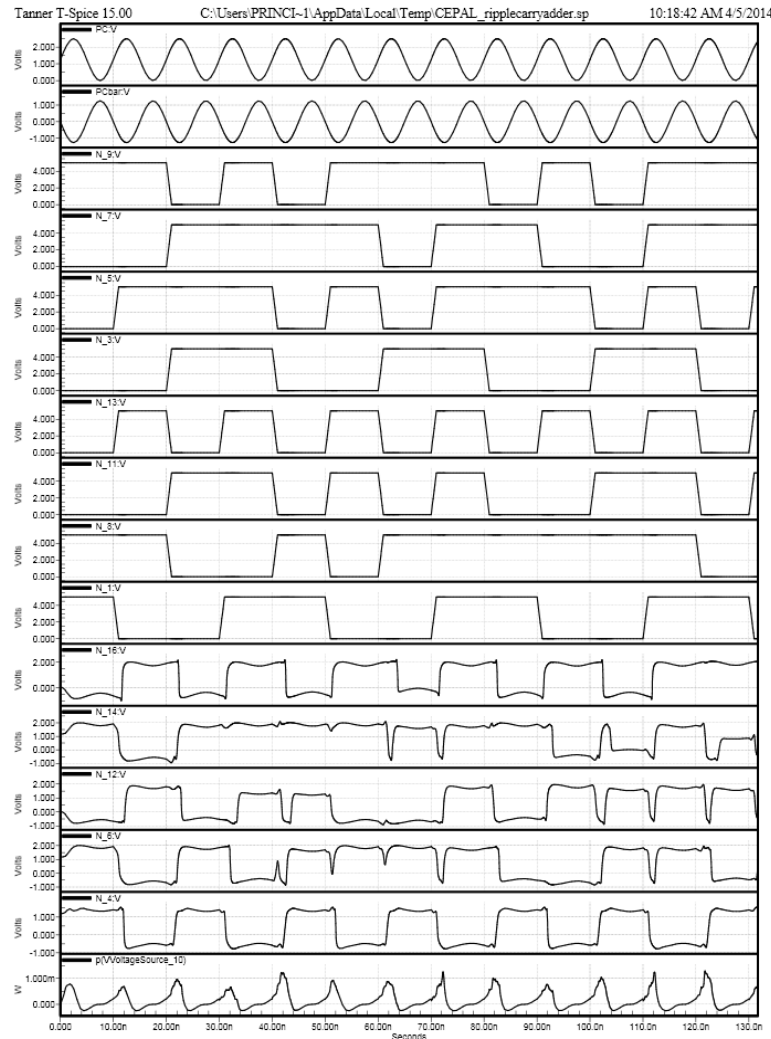
**Fig.8:** Output waveforms of Ripple Carry Adder

## IV.    Results

The CEPAL (Complementary Energy Path Adiabatic Logic) based Carry Look-Ahead Adder is implemented using 250nm technology of the Tanner EDA with a W/L = 0.35μm/0.25μm and at 2.5V operating voltage along with a power clock frequency of 100MHz. The simulation results of both CMOS and CEPAL based Carry Look-Ahead Adder are compared with the same logic implementation. The simulation environment was maintained the same to provide justified results.

Figure 9 shows the output waveforms of the CEPAL Carry look-ahead adder. The plot p(VVoltageSource_10) show the power consumption of the power clock. Plot PC and PCbar show the power clock given.

The number of transistors and the average power of the Carry Look-Ahead Adder using CMOS and CEPAL are shown in Table 4.

**Table 4:** Carry Look-Ahead Adder Transistor count & Power Comparison

| Logic | P-MOS | N-MOS | Total Transistors | Average Power (μW) |
|-------|-------|-------|-------------------|--------------------|
| CMOS  | 84    | 84    | 168               | 280.06             |
| CEPAL | 180   | 180   | 360               | 123.09             |

The CEPAL Carry look-ahead adder is found to be 56.05% power efficient as compared to its CMOS counterpart; this added advantage is a well worth tradeoff for the increased transistor count.
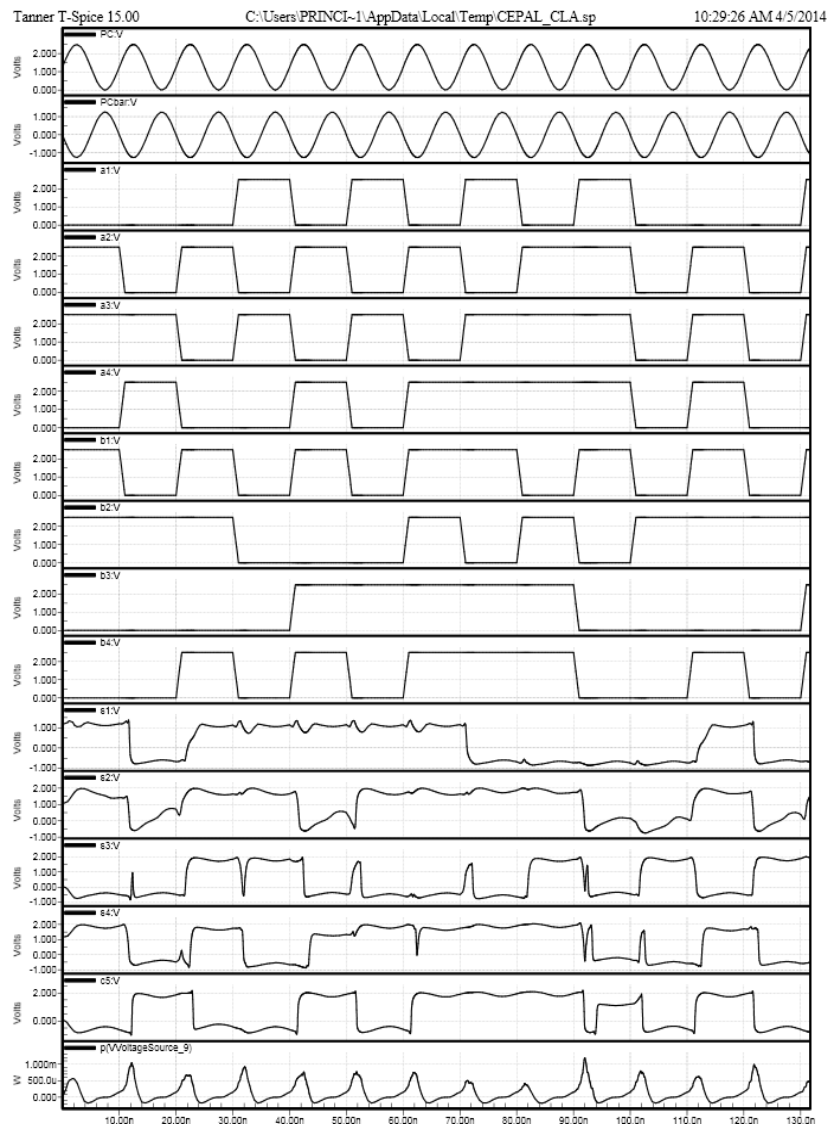
**Fig.9:** Output waveforms of Carry Look-Ahead Adder
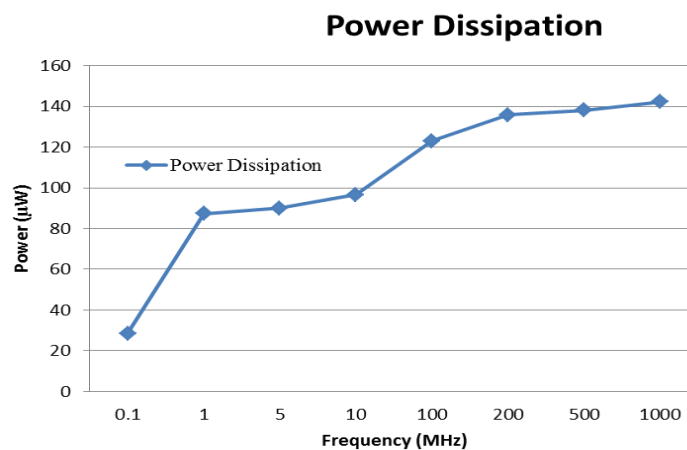


**Fig.10:** Power dissipation at various frequencies

The simulation results and the above graph clearly indicate that by applying CEPAL technology for Carry Look-Ahead Adder at various frequencies, the power dissipated by the Power Clock source has increased substantially with the increase in frequency of operation.

**CEPAL Vs CMOS Power Dissipation**
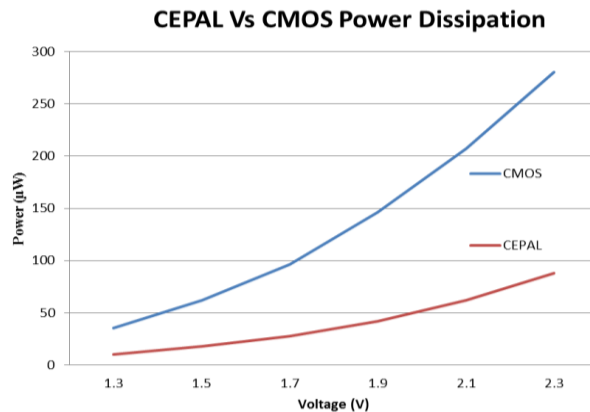


**Fig. 11:** Power dissipation at various supply voltage levels

Figure 11 shows the power dissipation comparison of Carry look-ahead adder for the two logic structures, namely CMOS and CEPAL, at different supply voltage levels. On incorporating CEPAL scheme, the power dissipation is evidently less than the Carry Look-Ahead Adder featuring CMOS at various supply voltages.

## V.    Conclusion

In this paper, we have presented the implementation of Carry Look-Ahead Adder circuit using single phase adiabatic logic family, namely, CEPAL (Complementary Energy Path Adiabatic Logic). The CEPAL uses increased number of transistors than the CMOS logic style due to the necessity of using the MOS diodes, in the charging/discharging process paths. These MOS diodes used in the CEPAL structure makes it identified as a static logic and the use of diodes helps in reducing the switching activity. The CEPAL structure, being a static type of logic, incurs the reduced switching activity.

Simulations indicate that the CEPAL realizes power advantage against the static CMOS to the tune of 56.05%. The results also prove that the CEPAL is suitable for optimal speed performance applications. When complex logic gates are operated at high frequencies, the output voltage fluctuation can be too large, which may result in erroneous circuit operations. Thus, the CEPAL scheme is found ideal for operation at the frequency range of 10MHz to 100MHz.

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