IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 4, Issue 4, Ver. I (Jul-Aug. 2014), PP 53-58
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Performance Analysis of Low Power Bypassing-Based Multiplier

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Abstract: *In the recent year growth of the portable electronics is forcing the designers to optimize the existing design for better performance. Multiplication is the most commonly used arithmetic operation in various applications like, DSP processor, math processor and in various scientific applications. In this paper a low power bypassing -based multiplier design is present, in which reduction in power is to be achieved in changed partial products of column bypassing multiplier as compared to column bypassing multiplier by exchange NOR gates with AND gates in the conventional multiplier I.e. in the design of conventional multiplier rather than AND gate, NOR gate is employed victimization DeMorgan's theorem. Compare with 32×32 bits typical (parallel array) multiplier and column bypassing multiplier, this planned system consume less power.*

Keywords: *changed column bypassing multiplier, conventional multiplier.*

I. INTRODUCTION

Multiplication is a necessary operation in DSP application. For the multiplication of 2 unsigned n-bit numbers, the number $A=a_{n-1}\,a_{n-2}\ldots a_0$ and also the multiplier factor,$B=b_{n-1}\,b_{n-2}\ldots b_0$ the product, $P=P_{2n-1}\,P_{2n-2}\ldots,P_0$ is depicted as the following equation:

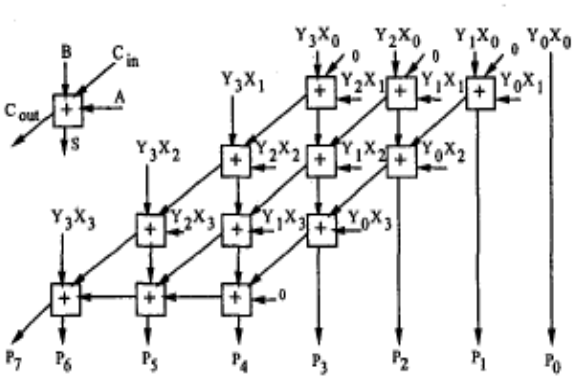
$$P=P_{2n-1}\,P_{2n-2}\ldots,P_0=\sum_{i=0}^{n-1}\sum_{j=0}^{n-1}(a_i\,b_j)\,2^{i+j}$$

To achieve the superior demand in DSP application, the structure of parallel array multiplier factor is wide used and also the typical implementation of such Associate in nursing array multiplier factor is Braun style. In n×n Braun multiplier[1],the multiplier factor array consists of (n-1) rows of carry-save adders(CSAs) and a (n-1) bit ripple carry adder within the last row, within which every row contains (n-1) Full adders(FAs). Multipliers square measure one among the foremost necessary arithmetic units in microprocessors and additionally a significant supply of power dissipation. Reducing the facility dissipation of multipliers is essential to satisfy the general power budged of varied digital circuits and system. Power consumed by multipliers is lowered at numerous levels of the planning hierarchy, from algorithmic rule to architectures to circuits, and devices.

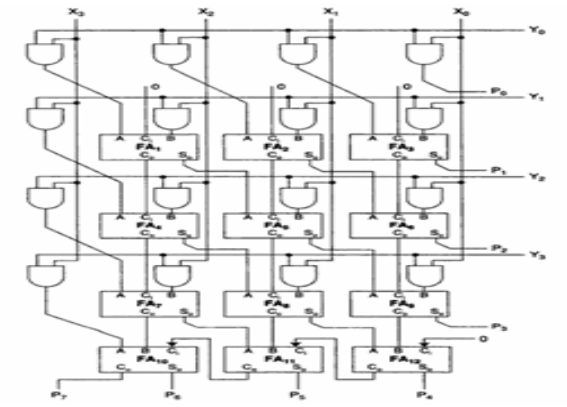
II.PRELIMINARIES

A. Parallel Array Multiplier(Braun Multiplier)

Multiplier factor circuit relies on add and shift algorithmic rule. Every partial product is generated by the multiplication of the number with one multiplier factor bit. The partial product square measure shifted in line with their bit orders so else. The addition may be performed with traditional carry propagated adder. N-1 adders square measure needed wherever N is that the multiplier factor length. The implementation of parallel array multiplier factor is additionally known as Braun design[5] as shown in figure1(b).



(a)



(b)

Figure 1: (a) multiplier array,**(b)** Braun design

B. Low Power Bypassing Based Multiplier

- **Column bypassing multiplier:**

For a low-power column-bypassing multiplier[3], the addition operations in the (i+1)th column can be bypassed if the bit, a_i in the multiplicand is 0, In the multiplier design shown in Fig(2), the modified FA is simpler than that in the row bypassing multiplier. Each modified FA in the CSA array is only attached by two tri-state buffers and one 2-to-1multiplexer. As the bit, a_i, in the multiplicand is 0, their inputs in the $(i+1)^{th}$ column will be disabled and the carry output in the column must be set to be 0 to produce the correct output. Hence, the protecting process can be done by adding an AND gate at the outputs of the last row of CSAs.

The column bypassing multiplier (CBM) only needs two tri-state gates and one multiplexer in a adder cell. When y_j is 0 then the corresponding diagonal cells are functioning unnecessarily. In all these cells the partial products $x_i \times y_j$ and the carry inputs are zero for i = 0,1,…,n-1 and this chain does not contribute to the formation of the product. Consequently, the sum output of the above cell can bypass this unimportant diagonal with the use of transmission gates. To achieve all of the above we can replace the Full Adder cell shown in ―Figure 2(a) with the cell in ―Figure 2(b) called the Full Adder Bypassing (FAB) cell. The transmission gates in the FAB cell lock the inputs of the full adder to prevent any transitions when y = 0, and a multiplexer propagates the sum input to the sum output. When y = 1, the sum output of the full adder is passed.

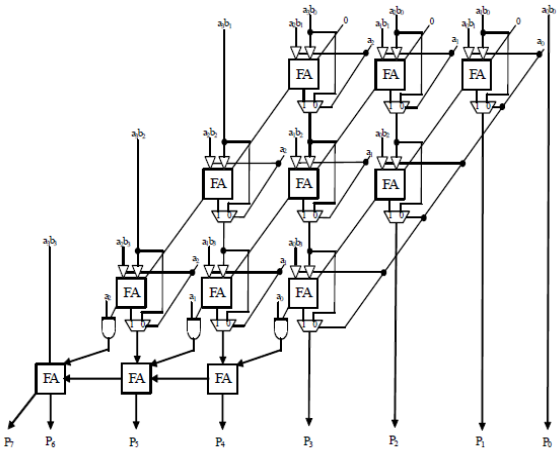


Figure 2: column bypassing multiplier

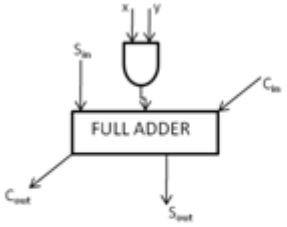


Fig2: (a)

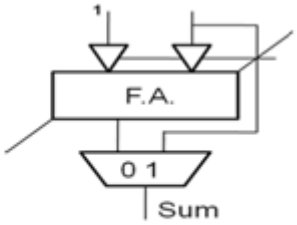


Fig2:(b)

- **Multiplier Design**

The column bypassing multiplier is shown in Fig (1). Note that we only need two tri-state gates and one multiplexer in a modified adder cell. If a_j=0, the FA will be disabled. We do not need a tri-state gate for the carry input (Ci-1, j), and the reason is given as follows. For a Braun multiplier, there are only two inputs for each FA in the first row (i.e. row 0). Therefore, when a_j=0, the two inputs of FA0, j are disabled, and thus its output carry bit will not be changed. In the bottom of the CSA array, we need to set the carry outputs to be 0. Otherwise, the corresponding FAs may not produce the correct outputs since their inputs are disabled. This is done by adding an AND gate at the outputs of the last-row CSA adders To understand the column bypassing technique, let's take an example of 4×4 multiplication as shown in Figure 2(c), which executes 1010*1111.

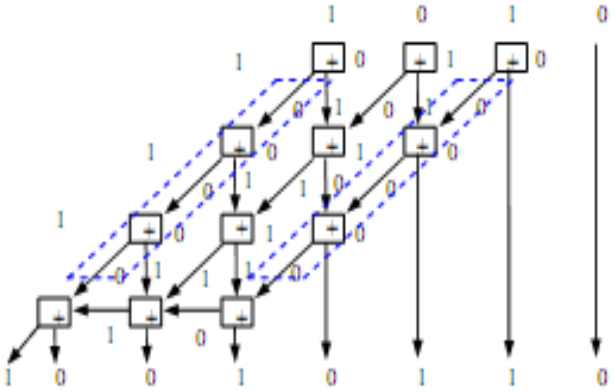


Fig 2(c): Multiplication in column bypassing

It can be verified that, for FAs in the first and third diagonals, two out of the three input bits are 0: the 'carry' bit from its upper right FA, and the partial product a_i b_j (note that a0=a2=0). As a result, the output carry bit of such an FA is 0, and the output sum bit is simply equal to the third bit, which is the 'sum' output of its upper FA.

III. THE PROPOSED DESIGN

- **Modified column bypassing multiplier:**

We propose a multiplier design in which partial products of column bypassing multiplier is modified. In the column bypassing multiplier, column can be disabled if the corresponding bit in the multiplicand is 0. There are two advantages to this approach. First, it eliminates the extra correcting circuit as shown in Fig. 2. Secondly, the modified FA is simpler than that used in the row-bypassing multiplier [2]. In the Proposed multiplier design instead of using AND gates we used NOR gates .The basic process of binary array multiplication involves the AND operation of multiplicand and multiplier bits and subsequent addition. NOR gates are used instead of AND in accordance with the De Morgan's Law: A.B = (A' + B')'

- **Hardware Modification:**

To design 4 x 4 bit multiplier we have a tendency to need sixteen AND gates, of that every AND gate consists of 6 transistor.a similar hardware will replaced by NOR gate that consists of solely four transistors .This reduction in hardware results into less power consumption.

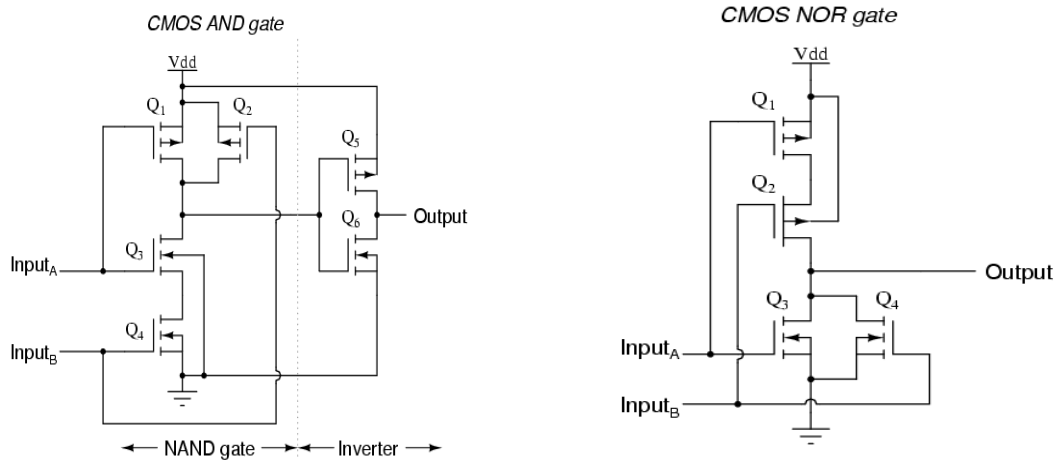


Figure 3: the circuit of CMOS AND gate and CMOS NOR gate.

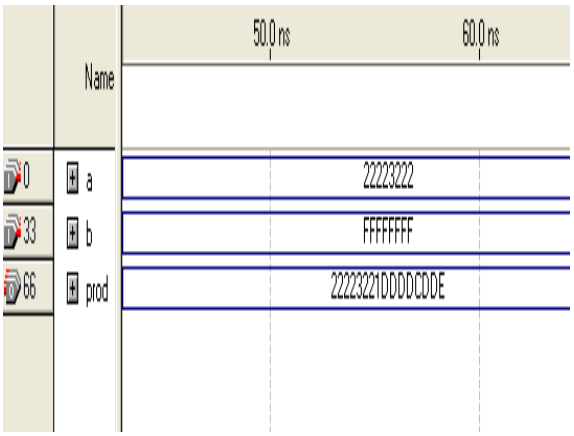
Thus, for a m* n multiplier factor, the projected technique introduces m + n further inverters beside dynamic m*n AND gates to m*n NOR gates, effectively saving (m*n − (m + n)) inverters or 2*(m* n − (m+n)) transistors. Figure (3) shows projected multiplier factor style with the replacement of AND gate with a NOR gate in partial product of column bypassing multiplier, ensuing into demand of less no. of transistor than the traditional style. The inputs are given in inverted form I.e. using NOT gate as shown in table I below:

Table I: Circuit Analysis of hardware modified for 32 bit multiplier

	No. of AND gates(n^2)	No of transistors	No of NOR and NOT gates(n^2)	No of transistors for	
				NOR gate	NOT gate
For 32-bit multiplication	32^2=1024	1024*6=6144	1024 & 64	1024*4=4096	64*2=128
Total transistor		6144		4096+128=4224	

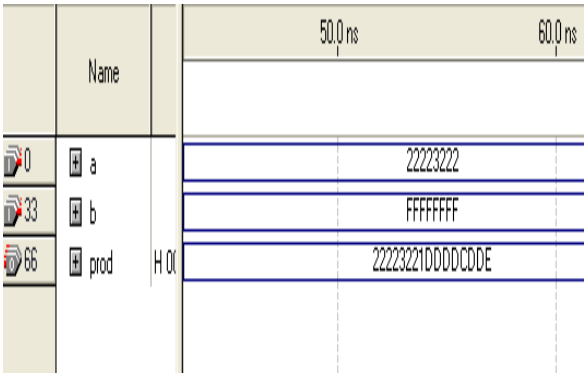
IV.RESULT

The performance analysis has been carried out on the proposed multiplier by performing simulations on Quartus II(8.1) and compared with the existing multipliers i.e Braun multiplier and column bypassing multiplier. Simulations are performed for 32×32 bit multiplier. Results shown in figure 4,5,6 are for particular inputs 22222222×FFFFFFFF.Similar result can also be obtain for other inputs. The power analysis and actual time is listed in Table II.



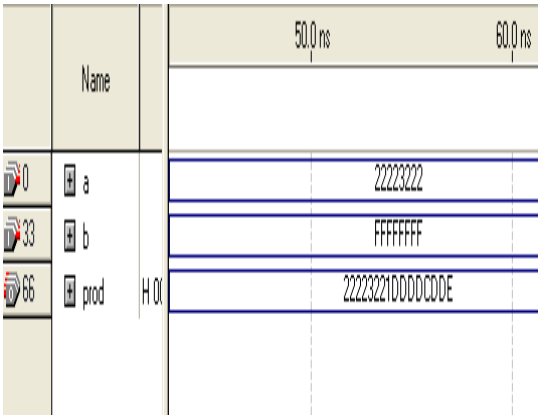
PowerPlay Power Analyzer Status	Successful - Mon May 12 20:56:18 2014
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	multiplier
Top-level Entity Name	multiplier
Family	Cyclone II
Device	EP2C5F256C6
Power Models	Final
Total Thermal Power Dissipation	124.65 mW
Core Dynamic Thermal Power Dissipation	10.88 mW
Core Static Thermal Power Dissipation	18.21 mW
I/O Thermal Power Dissipation	95.57 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

Figure 4: simulation and power analysis of 32× 32 bit Braun multiplier



PowerPlay Power Analyzer Status	Successful - Mon May 12 21:08:45 2014
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	multiplier
Top-level Entity Name	multiplier
Family	Cyclone II
Device	EP2C5F256C6
Power Models	Final
Total Thermal Power Dissipation	108.26 mW
Core Dynamic Thermal Power Dissipation	8.05 mW
Core Static Thermal Power Dissipation	18.17 mW
I/O Thermal Power Dissipation	82.03 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

Figure 5: Simulation result and power analysis of 32× 32 bit column bypassing multiplier



PowerPlay Power Analyzer Status	Successful - Mon May 12 21:23:06 2014
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	multiplier
Top-level Entity Name	multiplier
Family	Cyclone III
Device	EP3C5F256C6
Power Models	Final
Total Thermal Power Dissipation	93.52 mW
Core Dynamic Thermal Power Dissipation	4.86 mW
Core Static Thermal Power Dissipation	46.39 mW
I/O Thermal Power Dissipation	42.27 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

Figure 6: Simulation result and power analysis of 32× 32 bit modified column bypassing multiplier (Proposed design)

Comparison between Power and Actual time of three different multiplier

Table II: power comparison between Braun, column-bypassing and modified column-bypassing multiplier

Multipliers	Power	Actual Time
Braun multiplier	124.65mW	70.56nS
Column-bypassing multiplier	108.26mW	69.72nS
Modi-column-bypassing multiplier	93.52mW	62.52nS

IV. CONCLUSION

In this paper, a new approach for the design of partial product in column bypassing multiplier has been suggested. AND gates in the existing designs have been replaced with NOR gates. Where inputs are given in the inverted form. Results of simulation and power analysis show that the proposed (modified column bypassing) multiplier performs better than the existing system.

V.REFERENCES

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