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Design and Characterization of Third Generation Current Conveyor

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Abstract: *This paper presents a low power low voltage positive third generation current conveyor using four simple first generation current conveyors. It is designed and simulated in a standard 0.18um TSMC 1P, 6M CMOS process. This current conveyor design with the help of design architect and IC station (mentor graphics). Its DC, AC and transient analysis is carried out with ELDO tool. Its pre layout and post layout results are also given.*
Keywords: *Current mode circuit, third generation current conveyor*

I. Introduction

For LV, LP applications, current conveyors becoming very popular analogue building block now a days. Current conveyors are operated on the current mode approach [7, 8], which considers the information flowing on time varying currents. Current conveyors overcome many disadvantages of voltage mode op-amp.

1. When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increase the power consumption of voltage mode circuits [6].
2. In voltage mode designs the bandwidth is limited at high closed loop gains due to the constant gain-bandwidth product. Furthermore, the limited slew-rate of the operational amplifier affects the large signal, high frequency operation [6].
3. The MOS transistors are more suitable for processing currents rather than voltages [6].
4. MOS current-mirrors are more accurate and less sensitive to process variation than bipolar current-mirrors [5].

A current conveyor has current mode as well as voltage mode applications. Current conveyors are classified mainly in to three types. CC I(first generation current conveyor), CCII(second generation current conveyor),CCIII(third generation current conveyor). It shows below in the matrix form:

$$\begin{pmatrix} I_y \\ V_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & b & 0 \end{pmatrix} \begin{pmatrix} V_y \\ I_x \\ V_z \end{pmatrix}$$

If a = 1, Iy = Ix, which shows first generation current conveyor. If a = 0, Iy = 0, which shows second generation current conveyor. If a=-1, Iy = -Ix, which shows third generation current conveyor. b = ±1, which shows Iz = ±Ix, which shows either positive or negative current conveyor.

II. Third generation current conveyor

Third generation current conveyor (CCIII) was proposed by fabre in 1995.Its first CMOS implementation is done by A. Piovaccari. It is shown below in matrix form:

$$\begin{pmatrix} I_y \\ V_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} V_y \\ I_x \\ V_z \end{pmatrix}$$

CCIII works same as CCI except that the currents in ports X and Y flow in opposite directions. Here, Iz current follows current flowing in to the X terminal. It is a push-pull conveyor built from four simple first generation current conveyors [5]. Thus, the X and Y terminal impedances are maintained comparable low [5]. The third generation current conveyors (CCIIIs) can be considered as a current controlled current source with **a** unity gain [10]. Its schematic view is shown below.

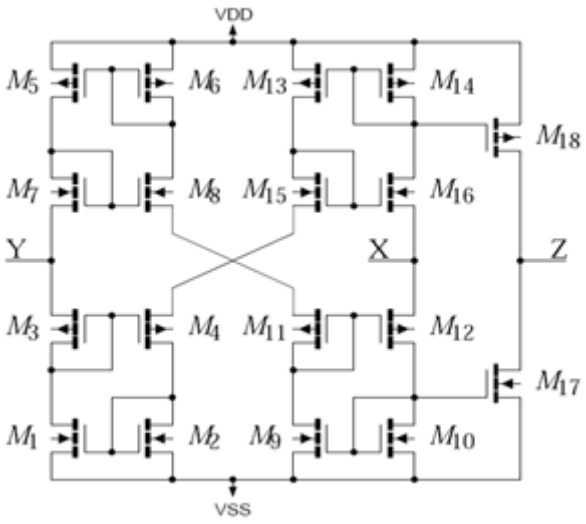

Fig. 1. Schematic of CCIII

This type of the current conveyor is useful to take out the current flowing through a floating branch of a circuit and can be utilized in realization of various multifunction filters, inductance simulation and all pass sections [10].The dimensions of the MOS transistors are given below in table1.

Table 1. Aspect ratio of transistors of Fig.1

Transistor	W(in µm)	L(in µm)
M3,M8	6.84	0.35
M2,M6	4.24	0.35
M4,M5	1.24	0.35
M7,M9	4.04	0.35
M11,M16	2.5	0.35
M10,M14	1.4	0.35
M12,M13	1.2	0.35
M15,M17,M19	1.44	0.35
M18	1.14	0.35

III. Simulation Results

The performances of presented CCIII are verified by Mentor Graphics simulation program using TSMC 0.18um CMOS technology. Here ±1.8V input supply is used for the operation of CCIII. For this circuit DC bias current value is set to 5µA.

The main DC and AC characteristics of the CCIII, such as plots of Vx versus Vy, plots of Iz+ and Iy versus Ix, frequency responses of Vx/Vy and Iz+/Ix are obtained.

The DC transfer characteristic of Vx versus Vy is shown in fig.2. Here input voltage is applied to Y terminal, output is taken from the X terminal with infinite load resistance connected to X terminal [10]. Z terminal is being grounded .Here linearity range is obtained from -1.14V to 1.14V.

Fig.3 shows DC transfer characteristics for Ix, Iy and Iz+ terminal. To obtained DC current waveforms, terminal X and terminal Z is being short circuited. Here maximum and minimum limits of the current Iz+ is obtained as: Iz+max = 0.93mA, Iz+min=-0.39mA.

Fig.4 shows the AC characteristics of voltages Vx and Vy.

f_{-3db} frequency of (Vx/Vy) is 1.24GHz. fig.5 shows current waveforms. For (Iz+/Ix), f_{-3db} frequency is 80.65Mhz.Fig.6 shows waveforms of trans impedance Rx, Rz as 26.98KΩ and 25.68KΩ respectively. Fig.7 shows transient analysis of voltages Vx, Vy.

Fig.8 shows layout of third generation current conveyor. This layout is simulated using IC station of mentor graphics. Results of post layout are depicted in Table 2.

Table 2 summarized performance characteristics of CCIII.

IV. Conclusion

CCIII is simulated and analyzed for pre layout and post layout design. It has good gain and high bandwidth. It uses low voltage and consumes low power. Here current gain will be improved by increasing trans impedance at X and Z terminals. Voltage gain will be improved by using modified topologies. By analyzing results, it is assured that current mode circuits give better performance in low voltage low power applications as compared with voltage mode circuits.

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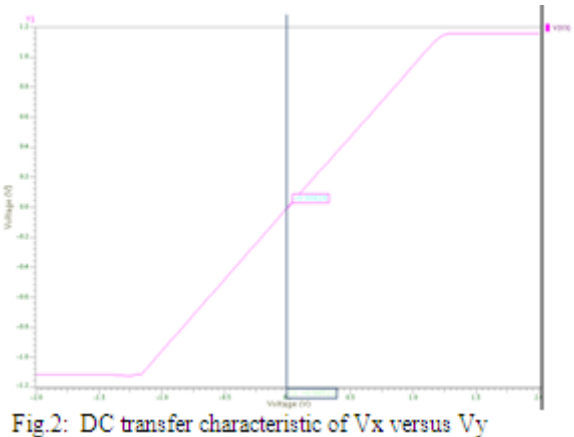

Fig.2: DC transfer characteristic of Vx versus Vy

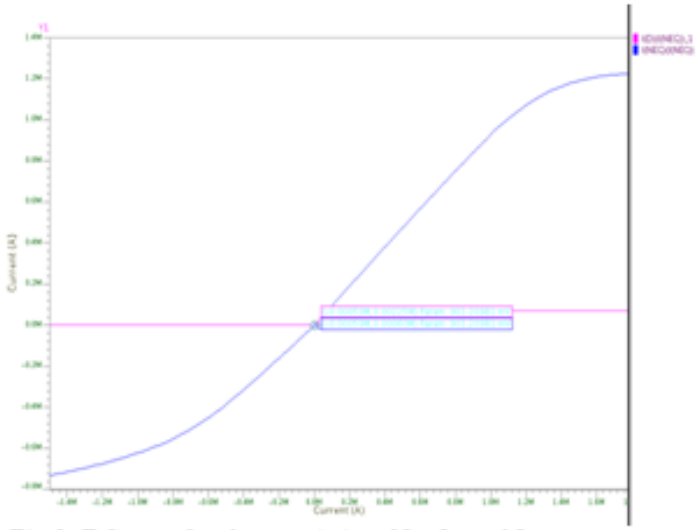

Fig.3: DC transfer characteristic of Iy, Ix and Iz+

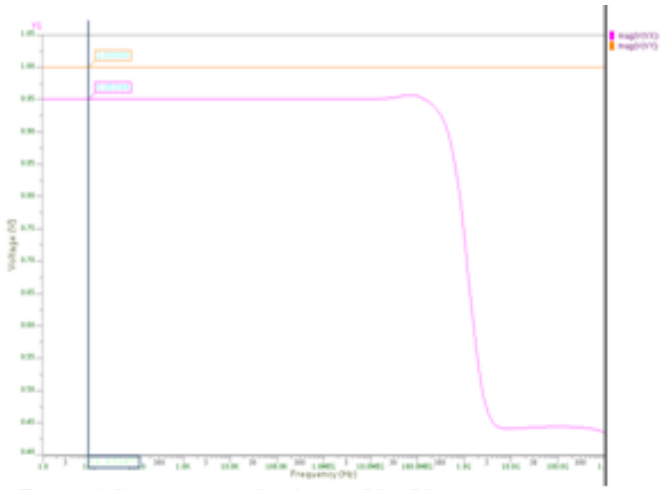

Fig.4: AC response of voltages Vx, Vy

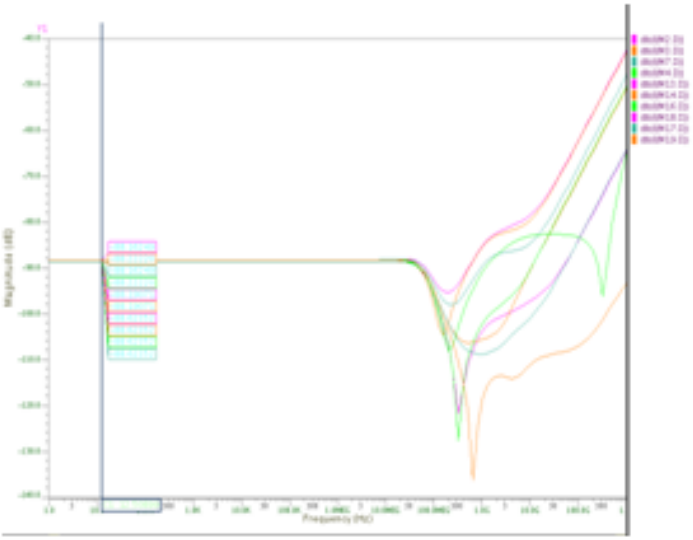

Fig.5: .AC response of currents Ix, Iy, Iz+

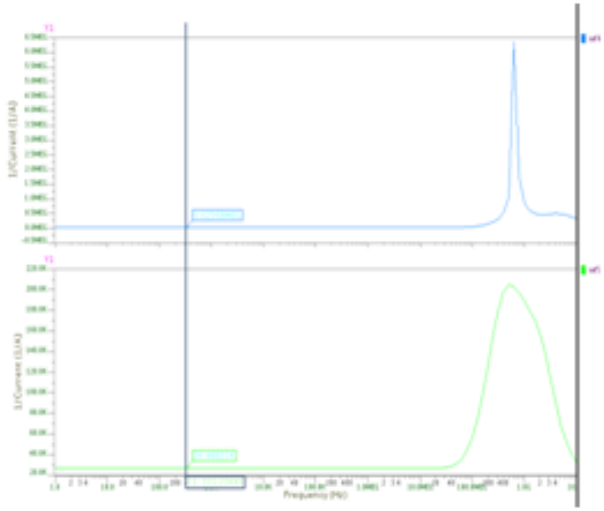

Fig.6: AC response of trans impedance Rx, Rz

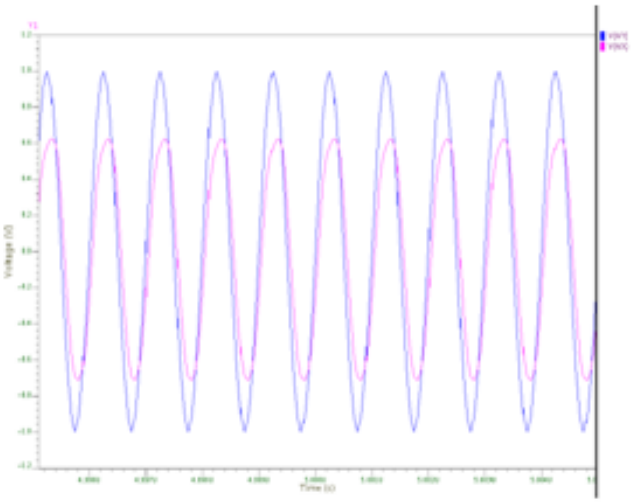

Fig.7: Transient analysis of voltages Vx, Vy

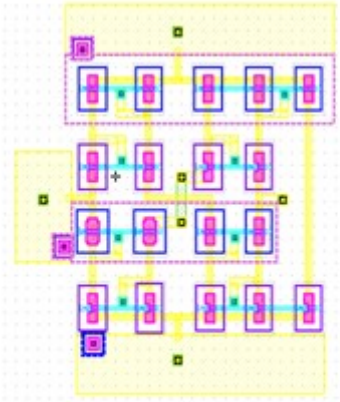

Fig.8: Layout of third generation current conveyor

Table 2: Performance Characteristic of Fig.1

Parameter	Pre layout results	Post layout results
CMOS technology	0.18µm	0.18µm
Voltage supply	±1.8V	±1.8V
DC bias current	5 µA	5 µA
Dynamic swing Vx-Vy	-1.14V to 1.14V.	-1.14V to 1.14V.
Dynamic swing Iz+-Ix	0.93mA to -0.39mA	0.93mA to -0.39mA
Vx/Vy accuracy (voltage gain)	0.95	0.95
Iz+/Ix accuracy	1.05	1.05
Ix/Iy accuracy	0.95	0.95
Vx/Vy f_{-3db}	1.24 GHz	1.22GHz
Iz+/Ix f_{-3db}	80.65MHz	77.81MHz
Trans impedance(Rx)	26.988KΩ	26.988KΩ
Trans impedance(Rz)	25.68KΩ	25.68KΩ
Power dissipation	256.64µwatt	256.67µwatt