Effect of phase of noise on the performance of 6T SRAM cell

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Abstract: *In this paper a detailed study of the effect of the phase of noise has been done on 6T SRAM cell. The 6T SRAM has been subjected to different combinations of noises at the storage nodes and the read ability and write ability of the SRAM cell is examined considering different noise voltage levels. It is found that the effect is different under different combinations of the phases of the noise voltages.*
Keywords: *SRAM, noise, phase, combination*

I. Introduction

The 6T SRAM cell is prone to noise during read operation, and during hold conditions. Several modifications to the circuit has been suggested in the literature**.** Naveen Verma *et.al* [1] introduced 8T bit-cell with buffered read which eliminates the read SNM limitation. The number of transistors increase for a given memory size. Jaydeep P. Kulkarni *et.al* [2] proposed yet another Schmitt Trigger SRAM cell, a modification of their earlier one which also incorporates a built-in feedback mechanism, achieving process variation tolerance, better read stability while absence of feedback and series connected NMOS in pull down path achieves better write-ability. The number of cells increase per memory cell.

Y. Wang *et.al* [3] proposed a 1.1 GHz 12 µA/Mb SRAM design in 65nm ultra–low power CMOS technology with integrated leakage reduction technique for mobile applications. They employ gate oxide thickness optimization and gate nitridation to reduce gate leakage. Well and pocket implants and source drain spacers are optimized simultaneously to reduce sub threshold leakage. Separate Vt threshold voltage control for N and P transistors in SRAM cells and peripheral circuit is employed to get minimum Vmin. The cell dimension is optimized to get high array efficiency of 78% and bit efficiency of 115Mb/cm^2 for 128kb sub array with improved static noise margin, write margin and read current at low-voltage design point. Transistor stacking and long channel transistors are used to save standby leakage in peripheral circuits. As reported it achieves 1.1 GHz frequency at a nominal voltage of 1.2V and 250MHZ at 0.7V which is claimed to be the highest reported frequency for the same class of standby power consumption for mobile applications.

Muhammad Khellah *et.al* [4] proposed process variations and supply-noise tolerant 45nm dense cache arrays with Diffusion-Notch-Free (DNF) 6T SRAM Cells and Dynamic Multi-Vcc Circuits. They have designed a programmable local word line voltage generator with built- in differential supply noise reduction circuits that help to set word line voltage optimally across global, within -die and die-to-die process variations, different cell VCC settings, and aging -induced degradations, and self-tracks word line and cell voltages over a wide frequency range. It also includes the programmable capacitive divider that can be used to provide adequate tracking at higher frequencies. The word line under drive (WLUD) provides ratioing between pass and pull down NMOS devices to improve read margin in Diffusion-Notch-Free min cells. They have allocated pull-up and pass PMOS devices with identical widths in the P cell to avoid diffusion notch. Partial writes along active rows are supported by implementing dynamic voltage collapse only along columns selected for write. Write assist technique mentioned in this paper minimizes generation, distribution & noise control overheads of additional supply rails in multi-Vcc static write improvement schemes. It was found by the authors that not only magnitude but also duration of dynamic collapse is programmable to flexibly track changes in the operating window across PVT variations & aging. Results in [4] show that 45nm CMOS min-cells with 200mV word line under drive (WLUD) improve read margin by ~3.5X at 1.1V. Write stability to be degraded overall cell margin below 1.1V. Dynamic Vcc collapse along with word line under drive restored overall cell stability down to 0.7V.

Baker Mohammad *et.al* [5] proposed a circuit to improve the noise margin of the 6T SRAM cell by reducing the effect of parametric variation of the cell in the low voltage operation mode. This design increases the SRAM Static Noise Margin (SNM) and write margin using a single voltage supply and with minimum impact to chip area, complexity, and timing. The technique put forward by the authors supports both on-chip corner identification to adapt the SRAM behavior to silicon, and software controllability to tradeoff yield, power, and performance. Delay elements are used to tune the value of the new voltage level, hence its granularity and level is limited by the delay element speed. But the speed of the memory access will be reduced to word line voltage reduction. However the authors have suggested that the timing impact can be reduced if the

control signal enables the reduced voltage swing control only on the fast corners. Here the SNM is most likely to affect the cell. Simulation results show that in the case study using 45nm data, the Vddmin is reduced from 1V to 0.8V which results in 36% of active power. Nalam.S *et.al* in reference [6] use asymmetric sizing for 5T SRAM to achieve higher read stability over 6T. However the effect of phase of the noise on SRAM cell has not been studied. Hence an attempt has been made so that the behavior of SRAM cells under noisy conditions can be understood in a better way.

II. Simulation model

The conventional 6T SRAM cell with sources of noise can be modeled as shown in the Fig. 1. It is assumed that equal amplitude of noise voltages appear at the storage nodes of the SRAM cell which are modeled by voltage sources connected to the input terminals of the inverters INV1 and INV2. T1 and T2 represent access transistors which are connected to bit lines BL and BLB. The polarities of the noise voltage sources are changed and the performance is observed under different noise levels. The HSPICE simulations are carried out using 65nm MOSFET model derived from [9]. The power supply voltage considered is equal to 1.1V. The SRAM cell considered has Static Noise Margin [7] of value 0.188V and write margin of 0.655V.

The amplitude of the noise voltage is varied gradually from 0 to 0.6V in steps of 0.1V. Three different simulations are carried out for each of the combination. i.e 1.Simulations to obtain the transient analysis during write, hold, read, hold times 2.Simulations to obtain static noise voltage margin using N curves[8] and 3. simulations to find the write margin. All these are done considering different noise voltage levels.
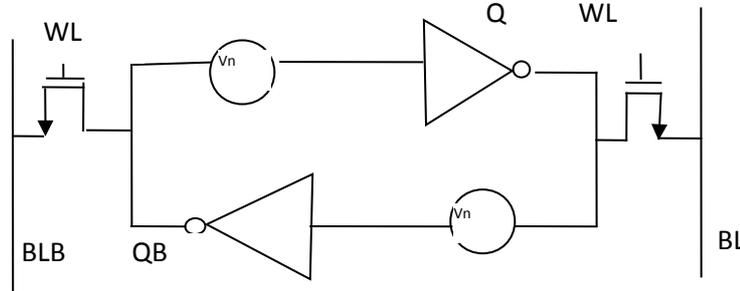
Figure 1a)   Model of 6T SRAM with noise sources shown as voltage sources
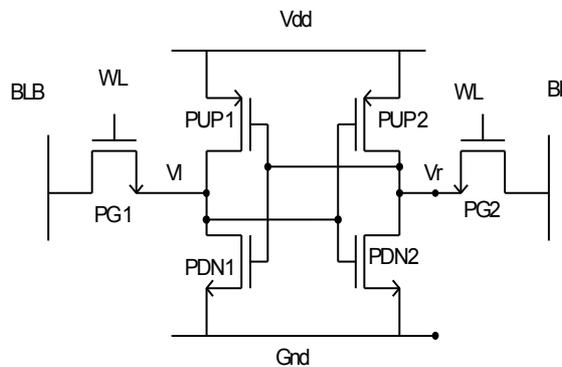
Figure 1b)   Circuit of 6T SRAM cell

III. PP Combination

It was found that in PP (positive terminals of the noise source are connected to the output nodes of the inverters) combination noise voltages help to maintain the existing status and hence the SRAM cell maintains the existing status as long as the noise voltage does not exceed the threshold voltage (0.5V) of the inverter. The waveforms of the operation of 6T SRAM cell is shown in the Fig. 2.The increase in the SVNM can be seen in the N-curves (Fig. 3). The write margin reduction with the increase in the noise voltage is seen in the Fig. 4.When the noise voltage exceeds the threshold voltage of the inverter *vinv* then the write operation by the noise is successful in both the inverters and they act as inverters with Vl =Vr.
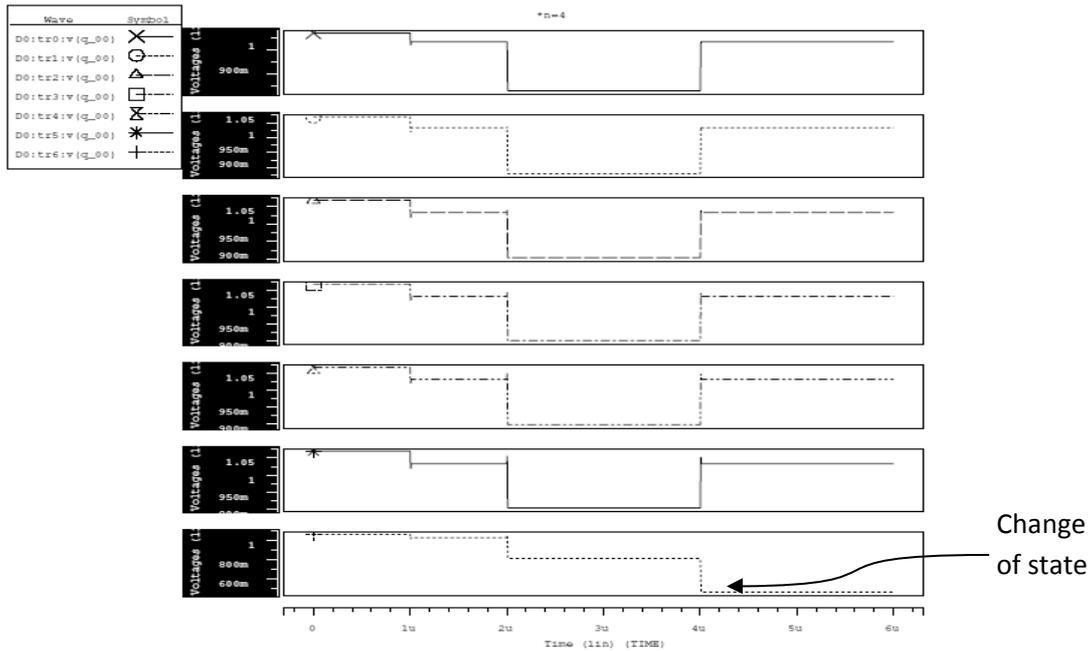
Figure 2 Waveforms of Q during write, hold, read and hold period. The level of Q is retained upto noise voltage <0.5V after read operation.
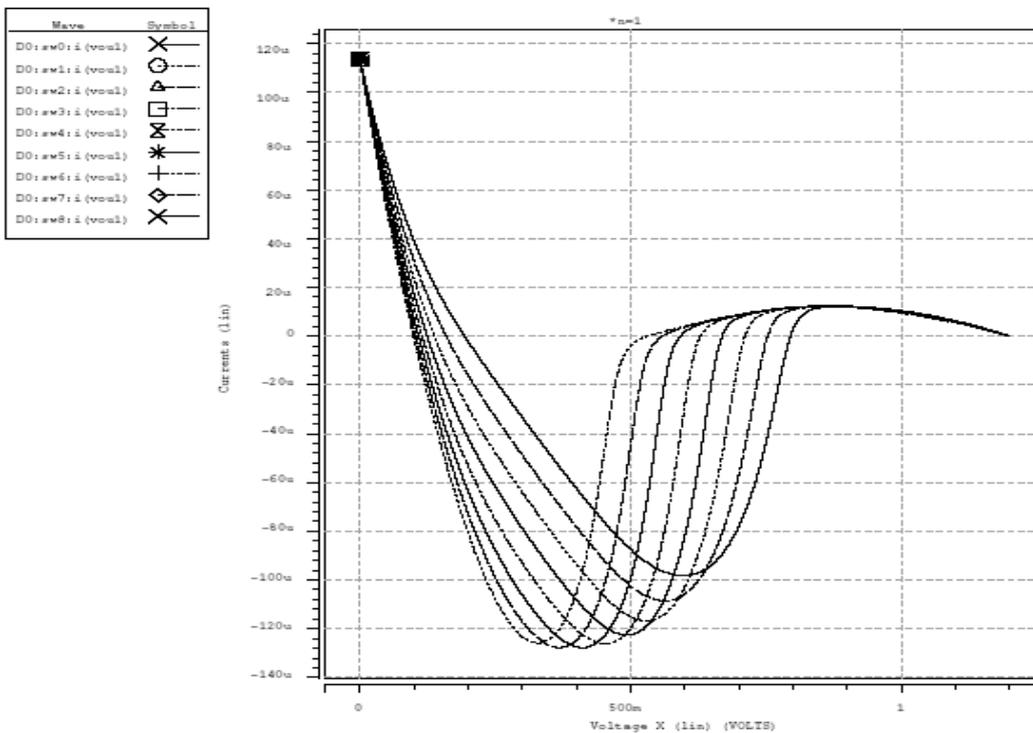
Figure 3 N-curves show the increase of Static noise voltage margin and decrease of write trip voltage as the noise voltages increases in PP combination
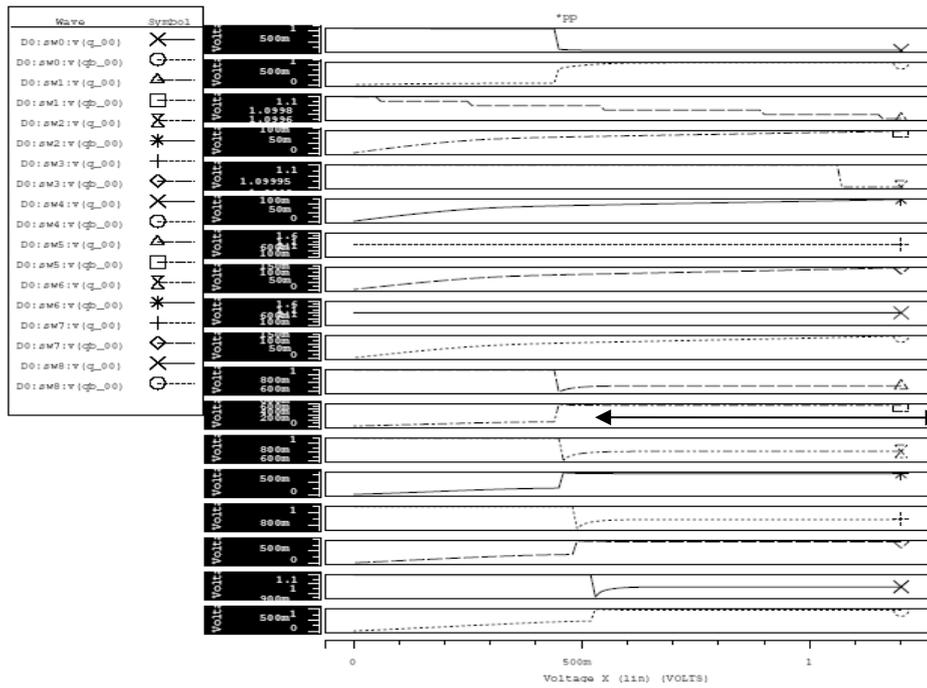
Figure 4 The write margin shown by double ended arrow decreases as the noise voltages increases in PP combination.

IV. NN Combination

In case of NN combination (the negative terminals of the noise sources are connected to the output terminals of the inverters respectively) the write ability increases with the application of noise. The noise voltages are tolerated up to the Static Voltage Noise Margin, the recovery fails and then successful write operation takes place. The waveforms of SRAM cell is shown in the Fig. 5. The corresponding N-curves are shown in the Fig. 6.The write margin marginally reduces with the increase in the noise voltage as seen in the Fig. 7
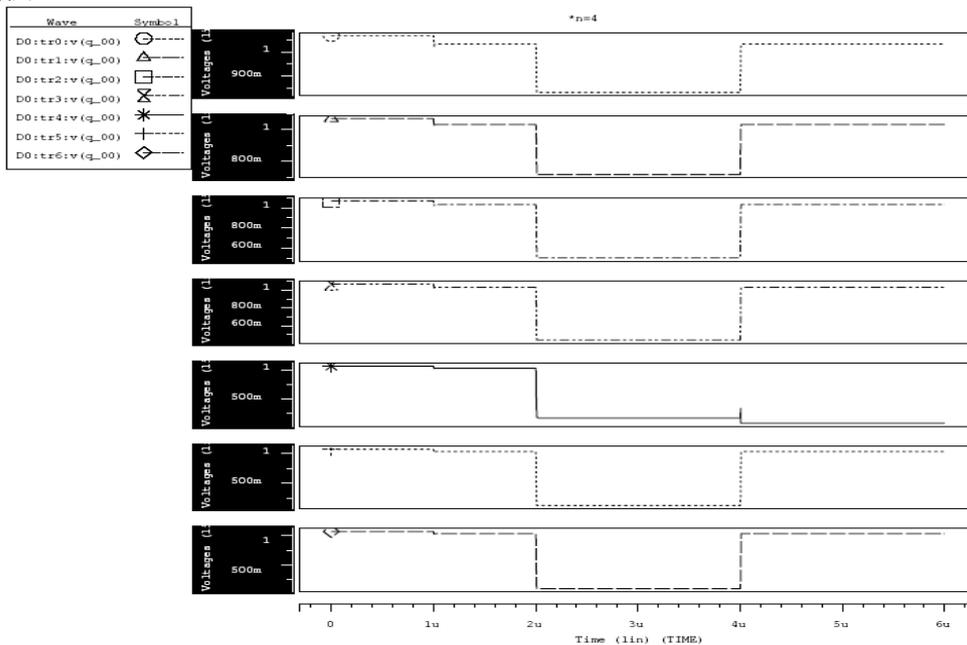
Figure 5 Waveforms of Q during write, hold, read and hold period.
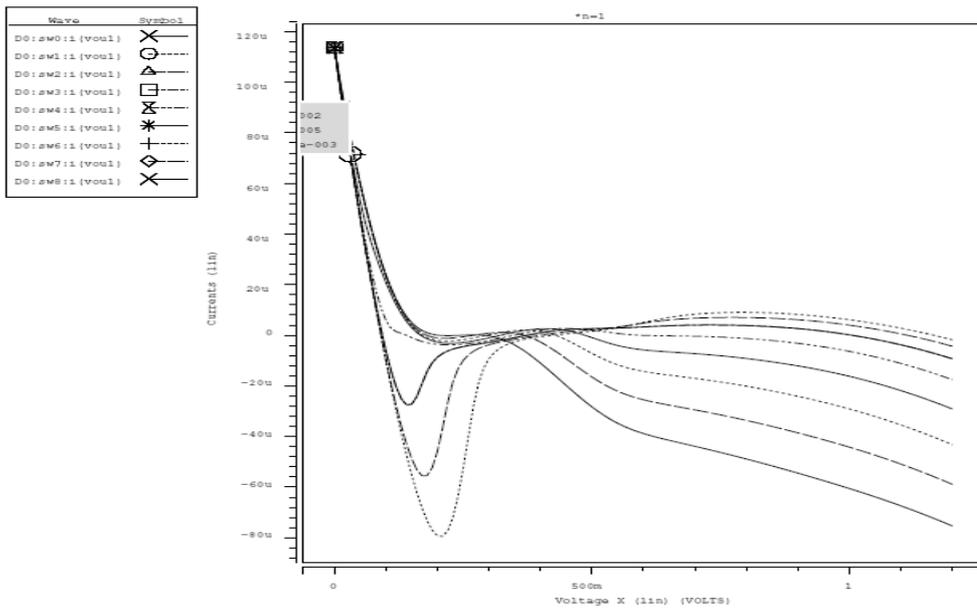
Figure 6 N-curves show the decrease of write margin as the noise voltages increases in NN combination
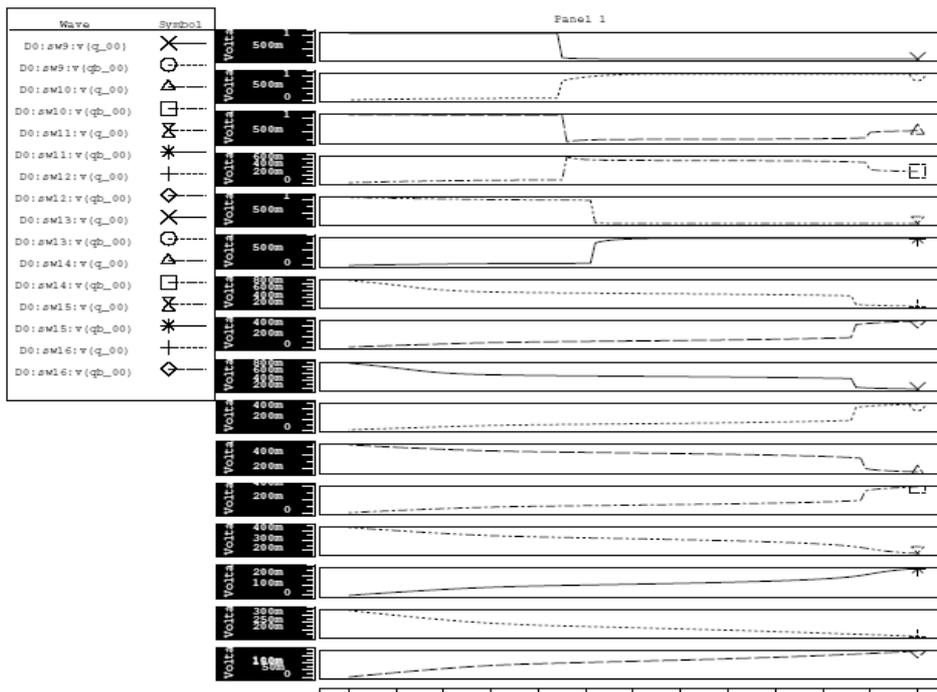
Figure 7 The write margin decreases as the noise voltages increases in NN

V.   PN Combination

In case   of   PN combination (the positive terminal of the noise source is connected to the output of the inverter (QB) and negative terminal of another noise source is connected to the output of the other inverter (Q) the polarities of the noise sources are in such a manner that the inverter operation is enabled and hence the SRAM cell tries to maintain its status even if the noise amplitudes are increased. The waveforms of SRAM are shown in the Fig. 8. N-curves (Fig. 9) show the decrease in write ability. The write margin decreases as the noise amplitudes are increased as seen in the Fig. 10 and writing becomes difficult.
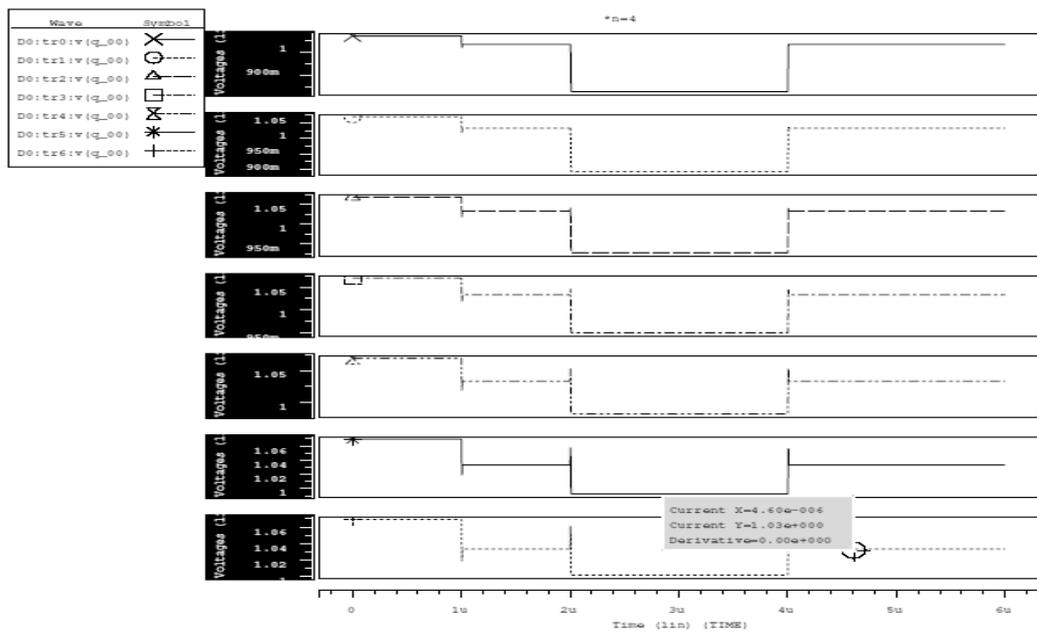
Figure 8 Waveforms of Q during write, hold, read and hold period of PN combination.
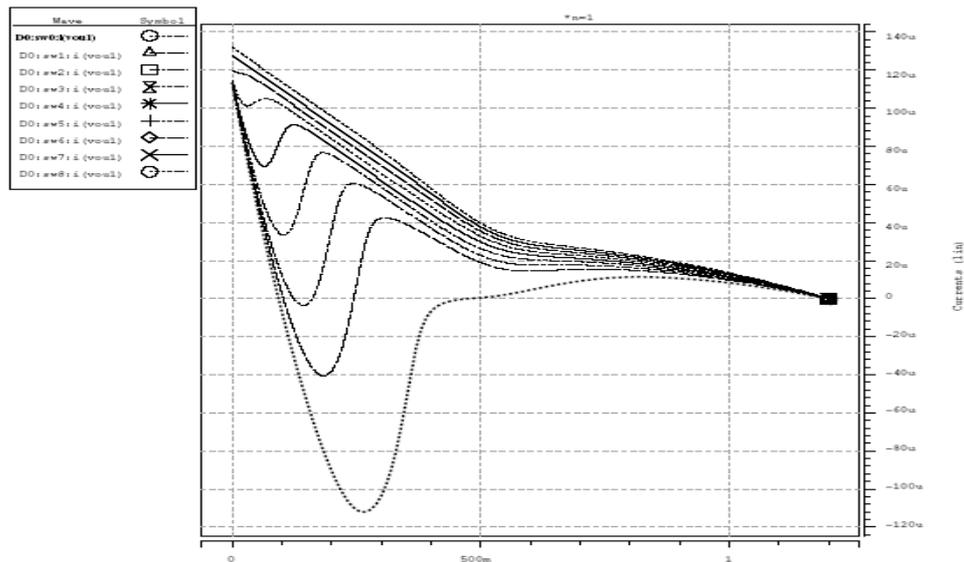
Figure 9 N-curves show the decrease of write ability as the noise voltages increases in PN combination.
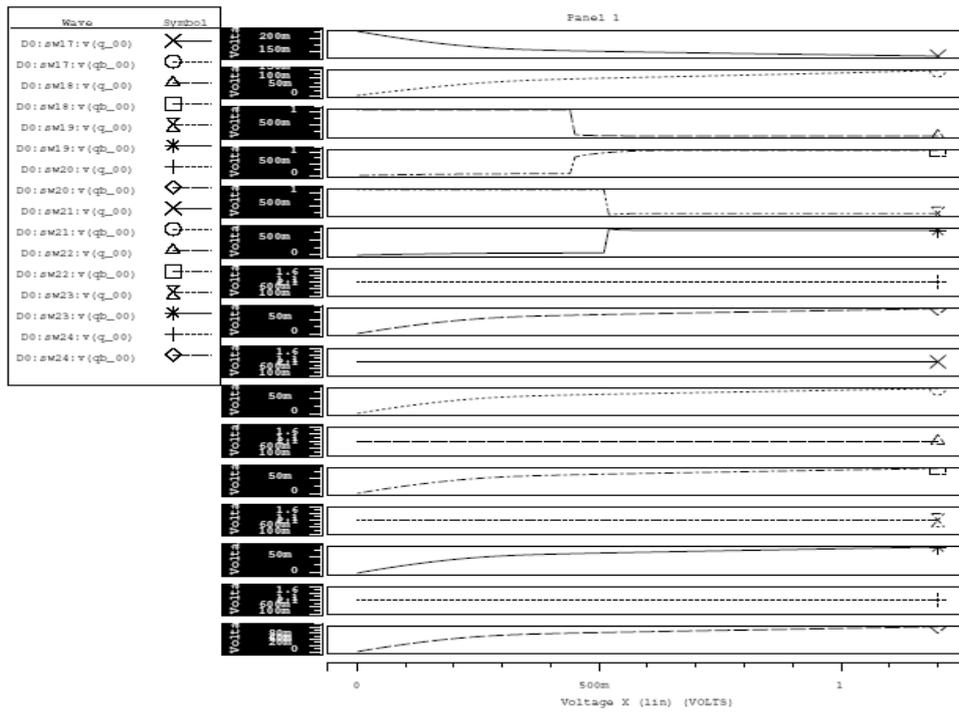
Figure 10 Write margin decreases as the noise voltages increases in PN combination.

VI. NP Combination

The polarities of the noise voltages (the negative terminal of the noise source is connected to the output terminal of the inverter (QB) and the positive terminal of the another noise source is connected to output (Q) are such that the stability is disturbed and the write ability increases and the noise voltage easily writes and the status is flipped for almost all noise voltage values. The waveforms of operation SRAM cell is shown in the Fig. 11. The level of Q is not recovered after read operation. N curves obtained for the same is shown in the Fig. 12. The write margin increases with the increase in the noise voltage as seen in the Fig. 13.
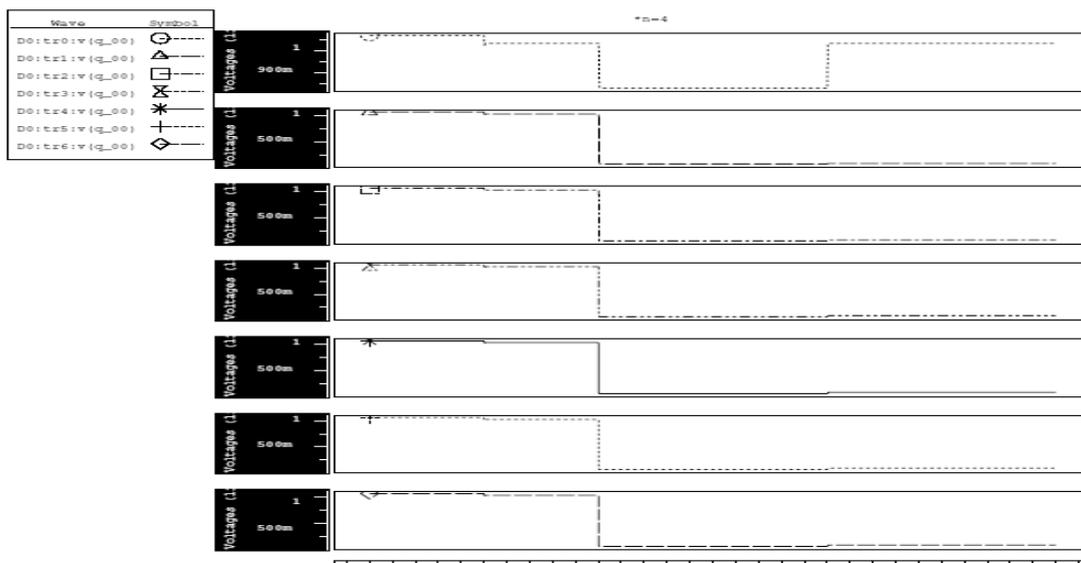
Figure 11 Waveforms of Q during write, hold, read and hold period.
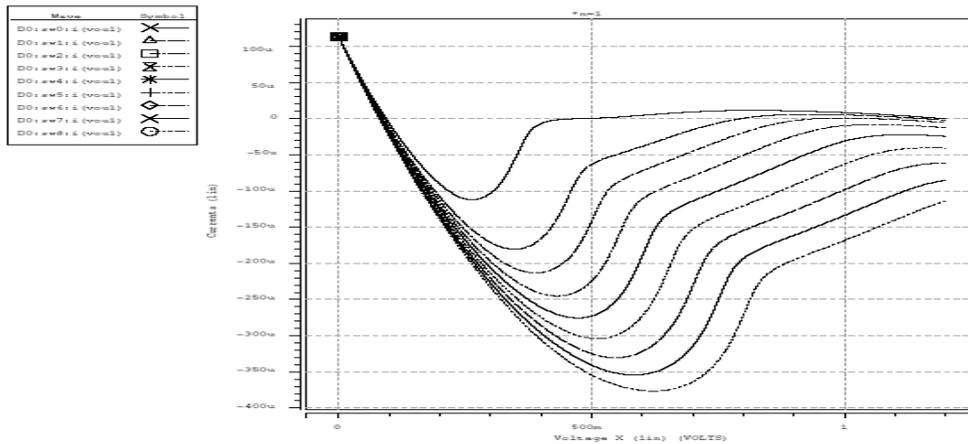
Figure 12 N-curves show the loss of stability as the noise voltages increases in NP combination
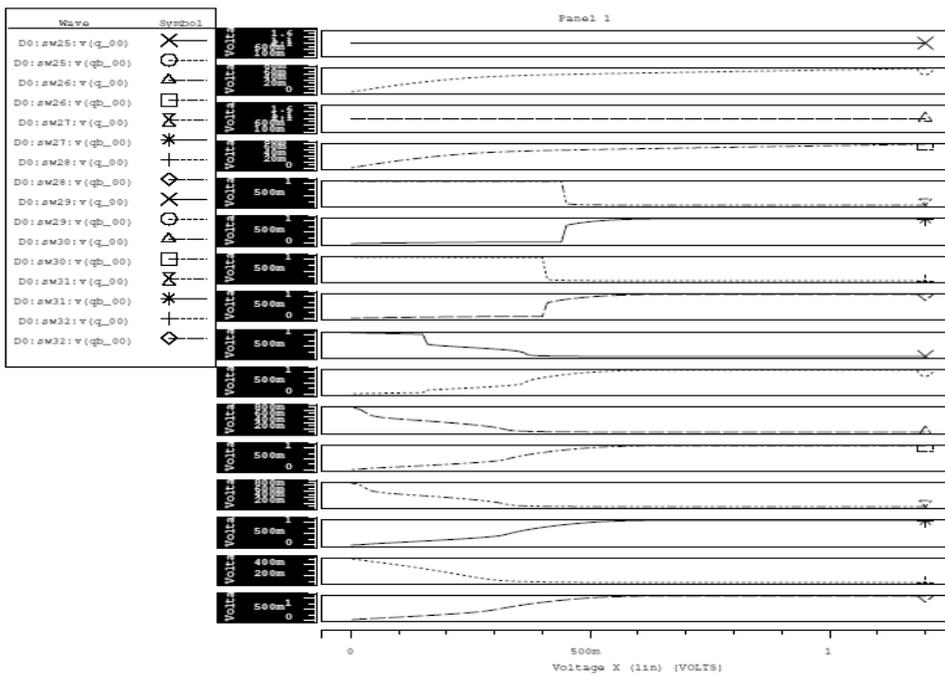
Figure 13 The write margin increases as the noise voltages increases in NP combination

VII.   Result Analysis

From these figures and discussions it may be understood that read stability and the write ability depend upon amplitude and polarity of the noise that affects the inputs of the inverters in the memory cell. During writing operation if the noise voltage enables to overpower the PMOS transistor of the inverter whose output is logic high, then writing is enabled and the status of the SRAM cell changes. Hence the polarities and the amplitude of the noise voltage affects the write operation and hence the write margin.

During read operation, if the cell has to change its state, then write operation should take place when both the bit lines are high. This happens when the noise voltage plus the voltage across the access transistors is

greater than the threshold voltage of the inverter. If the phase and amplitude of the noise voltage is such that the voltage across access transistors is reduced then the read stability is improved and vice versa. Of all the four combinations NP combination is the worst case for conventional SRAM cell.

VIII.   Conclusion

The effect of the phase of noise on 6T SRAM cell is considered during write, read and hold operations. The 6T SRAM cells has been subjected to different combinations of noises at the storage nodes and the read ability and write ability of the SRAM cell is examined considering different noise voltage levels. It is found that the effect is different under different combinations of the phase of the noise voltages. The effect is worst in NP combination   resulting in unstable operation.

Acknowledgements

References

Proceedings Papers:
[1].   Naveen Verma, Anantha P. Chandrakasan, A 65nm 8T Sub-Vt SRAM Employing Sense-Amplifier Redundancy: Proc. Of International Solid State Circuits Conference, 2007, 328-329
[2].   Jaydeep P. Kulkarni, Keejong Kim, Sang Phill Park and Kaushik Roy,Process Variation Tolerant SRAM Array for Ultra Low Voltage Aplications: Proc. Of   DAC2008, 2008, 108-113
[3].   Y. Wang, H. Ahn, U. Bhattacharya, T. Coan, F. Hamzaoglu, W. Hafez, C.-H. Jan, P. Kolar, S. Kulkarni, J. Lin, Y. Ng, I. Post, L. Wei, Y. Zhang, K. Zhang, M. Bohr, A 1.1GHz 12μA/Mb-Leakage SRAM Design in 65nm Ultra-Low-Power CMOS with Integrated Leakage Reduction for Mobile Applications: Proc. Of International Solid State Circuits Conference, 2007, 324
[4].   Muhammad Khellah, Nam Sung Kim, Yibin Ye, Dinesh Somasekhar, Tanay Karnik, Nitin Borkar,Fatih Hamzaoglu, Tom Coan, Yih Wang, Kevin Zhang, Clair Webb, Vivek De ,VT-Variations and Supply-Noise Tolerant 45nm Dense Cache Arrays with Diffusion-Notch-Free (DNF)   6T SRAM Cells and Dynamic Multi-Vcc Circuits: Proc. Of 2008 IEEE Symposium on VLSI Circuits, 2008, 48-49
[5].   Baker Mohammad, Martin Saint-Laurent, Paul Bassett, Jacob Abraham , Cache Design for Low Power and High Yield: Proc. Of ISQED'08, 2008,103-107,
[6].   Nalam.S and Calhoun, B.H ,Asymmetric Sizing in a 5T SRAM to Improve Read Stability over 6T: In Proc. IEEE 2009 Custom Integrated Circuits Conference,2009, 709-712
Journal Papers:
[7].   Seevinck, F.J. List and J. Lohstroh,Static-noise margin analysis of   MOS SRAM cells, Solid-State Circuits, IEEE Journal of, vol. 22,1987, 748-754
[8].   Evelyn Grossar, Michele Stucci, Karen Maex, and Wim Dehaene, Read Stability and rite–Ability Analysis of SRAM Cells for NanometerTechnologie ,IEEE J.Solid –State ircuits ,vol. 41,no.11, 2006,2577-2588.
URL :
[9].   http://ptm.asu.edu/