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Implementation of CDMA receiver using Recursive Digital Matched Filter

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Abstract: *Code Division Multiple Access (CDMA) is a multiple access technique widely used in cellular and military communication systems. In Direct Sequence Spread Spectrum (DSSS) communications, data samples are embedded inside Pseudo Noise code (PN code) prior to transmission. Synchronization of this unique code with the incoming data samples forms an important step in data recovery. Single Dwell Serial Search (SDSS) and Matched Filtering are some of types of the CDMA code synchronization techniques. This paper presents design and implementation of Recursive Digital Matched Filter (RDMF) for code synchronization in CDMA. From design summary, it is observed that with RDMF, lesser hardware is utilized compared to the conventional methods. And also, a modification in despreading steps is proposed for achieving reduced Bit Error Rate (BER) performance*

Keywords: *Synchronization, Digital matched filter, Component reuse.*

I. Introduction

DSSS communications uses PN spreading codes such as walsh codes to spread the data samples and then applies digital modulation technique such as Binary Phase Shift Keying (BPSK) to the spreaded data samples [1][2]. The most sensitive part of a DSSS system is the synchronization of the transmitter's PN sequence to that of the receiver. Synchronization in this paper represents the trigger of a timing mark. That is, during the synchronization process a signal indicates the position of PN code embedded in the data and initiates other steps in the recovery of transmitted data [3]. Synchronization in this paper denotes the use of a known preamble between the transmitter and the receiver which is to be synchronized by a matched filter [4] [5]. In literature, this is known as Data-Aided (DA) synchronization [6]. Several techniques like single dwell serial search, multiple dwell serial search, Matched Filter correlations are presented for obtaining synchronization. In this paper, the performance of Single Dwell Serial Search (SDSS) and Digital Matched Filter (DMF) is discussed comparatively. In SDSS technique, single chip multiplication is performed in a clock period. This technique has a demerit of longer time consumption for acquisition. To overcome this limitation DMF is used, where multiplication of entire PN sequence length is performed in single clock period but with increased resource consumption.

To decrease the number of resources utilized, a modified structure of DMF known as Recursive Digital Matched Filter (RDMF) is proposed and implemented in this work. This paper is organized in the following manner. Section II deals with Single Dwell Serial Search technique for synchronization. Section III is about synchronization using Matched Filtering. Section IV explains about Recursive structure of Matched filter in a detailed manner. Section V deals with the implementation of CDMA receiver and a proposal of modification in despreading steps for increased BER performance. Section VI gives results obtained and conclusions inferred from the results.

II. Single Dwell Serial Search technique

In SDSS system [7], the received signal is multiplied by a reference PN sequence over particular step size (single chip) and is accumulated subsequently after each step [8], the result of which is used to make a synchronization decision by comparison with a threshold. Such multiply and integrate type of correlation structure can be implemented through Multiply and Accumulate (MAC) operation in digital domain as shown in Fig.1.

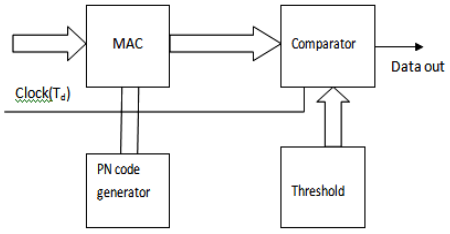

Fig.1. Block diagram for SDSS technique

SDSS systems poses a basic limitation on the search speed since the PN reference phase can be updated only at T_s second intervals (assuming the threshold test fails), where T_s is the time taken for the entire chip by chip multiplication of the PN sequence with the received data sequence. Thus the search rate R_S of the SDSS technique is

$$R_S = 1/T_s \qquad (1)$$

and $T_s = NT_c$, where N is the length of the PN Sequence and T_c is the chip period. To improve search rate synchronization is done using DMF, as discussed in next section.

III. Matched Filtering Technique

The search rate of a SDSS synchronization scheme can be increased by replacing the multiply-and-integrate operation with a correlator device such as matched filter (MF) [9] [10]. Conventional matched filter maximizes SNR at its output if the signal at its input is present embedded inside additive white Gaussian noise. For an input signal r(t) of duration T_s seconds, the impulse response h(t) of the matched filter is given by,

$h(t) = r(T_s\text{-}t)$ for $0<t<T_s$ (2)

The filter output is given by,

$$\begin{aligned} y(t) &= r(t) * h(t) \\ &= \int r(\tau - t)\, h(\tau) d\tau \\ &= \int r(\tau - t)\, r(T_s - \tau) d\tau \end{aligned}$$

$$y(t) = R(T_s - t) \qquad (3)$$

Thus filter output is the autocorrelation function of r(t).

Matched Filter can be implemented with technologies such as surface acoustic wave (SAW), charge coupled devices (CCD) convolvers [11] and discrete time correlators. Many commercial equipments use portable terminals with limited power supplies [12]. Thus, low power transmitters and receivers are required to be deployed in these devices. The receiver containing Matched Filter is considerably more complex and the work is on going to develop lower power devices. Matched Filter occupies a place between the input circuit and the digital data processing circuitry, so that the conversion from analog to digital can take place before the matched filter input or after its output. This leaves engineer with the freedom to implement matched filter in either analog or digital form.

In the analog case, the received PN signal is convolved with a finite segment of the PN waveform corresponding to, say, M chips and the continuous time output is tested against a threshold to determine whether synchronization has occurred. In this type, the input continuously slides past the PN waveform until the two are in synchronization. At this point the threshold would be exceeded and the local PN generator is enabled for despreading. The analog circuit implementation is more power efficient for shorter, faster matched filters, and, conversely, the digital circuit is more power efficient where the filters are longer and slower [13].

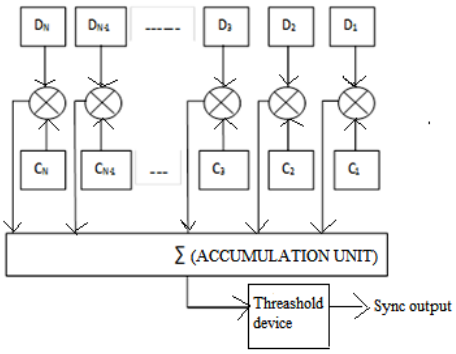

Fig.2. Digital Matched Filter

In the digital matched filter shown in Fig. 2, the contents of the shift register that holds the data samples and the PN code are correlated generating "+1" if the corresponding bits of them are equal and "-1" if they are not equal, and summing the resulting sets of "1's" and "-1's.". The correlation output is thus given by,

$$O(j) = C_N D_{N+j} + C_{N-1} D_{N-1+j} + \ldots\ldots\ldots + C_1 D_{1+j} \qquad (4)$$

where 'C_N' is PN sequence and 'D_N' is data sequence and 'j' is the number of shifts in data sequence done until the threshold is crossed. The search rate for this synchronization method is N times faster than that of the SDSS technique since threshold testing is done in each clock period. This results in apparent reduction in the time to search over the uncertainty region. Search rate for Matched Filtering case is given by,

$$R_{MF} = 1/T_c = N/T_s \qquad (5)$$

IV. Recursive DMF

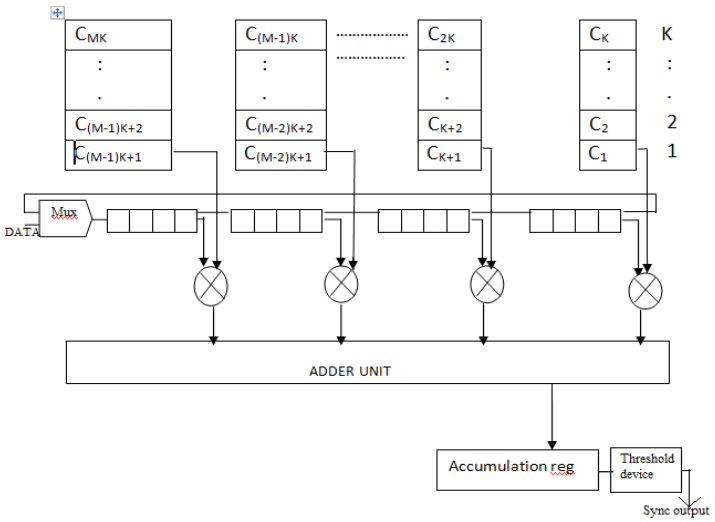

Fig. 3. Recursive DMF

In order to reduce the resources consumption, we inherited and modified the concept of segmented matched filter [14] [15] and designed the RDMF as shown in Fig.3. In RDMF, we do a part of correlation in one subcycle. We then reuse the same hardware to do the remaining correlation in the remaining subcycles. A complete correlation that is to be completed in one clock cycle by DMF, is done in K subcycles where K= N/L and L is the number of multipliers or adders used in the RDMF structure. The operation of the RDMF is given by the equation,

$$Y = \sum_{i=1}^{k} C_{(L-1)K+I} D_{(L-1)K+i} + C_{(L-2)K+I} D_{(L-2)K+i} + \ldots + C_i D_i \qquad (7)$$

where $C_1, C_2 \ldots, C_{LK}$ refers to the code and $D_1, D_2 \ldots, D_{LK}$ refers to the data sequence respectively.

The operation of the RDMF is explained as follows. Let N be the total number of code samples. Divide the entire code sequence into K segments (K= N/L), each segment of length L as shown in Fig. 3. Load the shift register with input samples. For first iteration, say i = 1, select the bottom code segment. Multiply this code segment and data samples of length L. Accumulate the result in a intermediate register. Shift the data in the input register. Increment i by 1, select the corresponding code segment (the one above the bottom code segment) and do multiplication and accumulation as done previously. Continue this multiplication and accumulation till i = K. Shift register is loaded with a new data sample once in every K subclock cycles. Output of the shift register is fed back into its input at the remaining cycles. The time period for each cycle is given as

$$T_{MF} = K\, T_K \qquad (6)$$

where T_K is the time taken for completion of one sub cycle and K is the number of subcycles.

V. Cdma receiver

The blocks for the typical DSSS CDMA receiver includes demodulation and despreading unit next to the synchronization unit as shown in fig. 4

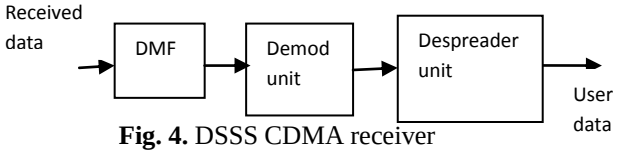

Fig. 4. DSSS CDMA receiver

After the frame is detected, the data samples next to the frame are collected in a register. It is then to be passed into the demodulation unit. Here BPSK demodulation is done through mapping of '-0.9' into '0' and '+0.9' into '1' (practical used values are 0.9 and -0.9). Then the resulting bits are passed into the despreading unit. First step in despreading is XOR-ing the demodulated sequence with the PN sequence, which is the one used for spreading operation in the transmitter side. This will result in continuous zeroes and ones with each of length equal to length of PN sequence and the total length equal to length of demodulated sequence. This is then reduced to the length of original data sequence through sequential mapping of one bit (first bit) out of N bits into a register, where N is the length of PN sequence. Fig. 5 shows the block diagram for the despreading done through mapping.

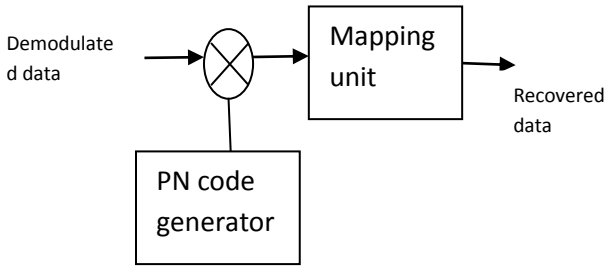

Fig. 5. Typical Despreading unit in DSSS CDMA receiver.

This type of despreading process will result in the exact recovery of data sequence sent at the transmitter provided that the received sequence is without any error. But recovering of channel affected sequence will result some bits in error in accordance with the SNR of the received signal. This is because if the mapped bit (one out of N bits) is noise affected (hence sign flipped), then its mapping will result in error. This widely happens particularly in the case of signals with low SNR values. For the improved performance, instead of mapping one out of N bits, mean operation is done on the resulted XORed sequence and its result is analyzed. If the result is above 0.5, '1' can be inferred and if it is below 0.5, '0' can be inferred. Fig. 6 illustrates the blocks in place for the despreading with averaging operation.

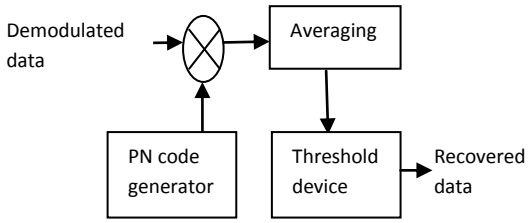

Fig. 6. Despreading unit with mean operation

VI. Results and Discussion

In this paper, code synchronization for CDMA application is implemented using SDSS, DMF and RDMF with following specifications as given in table 1.

Table 1. Implementation specification

Family	Sparten3e
Device	xc3s500e
Package	4fg320
Speed grade	-4

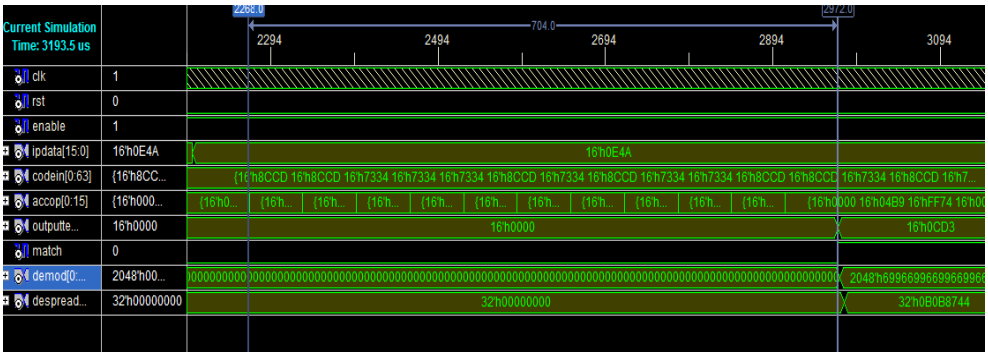

Fig.7. SimulationresultforSDSStechnique.

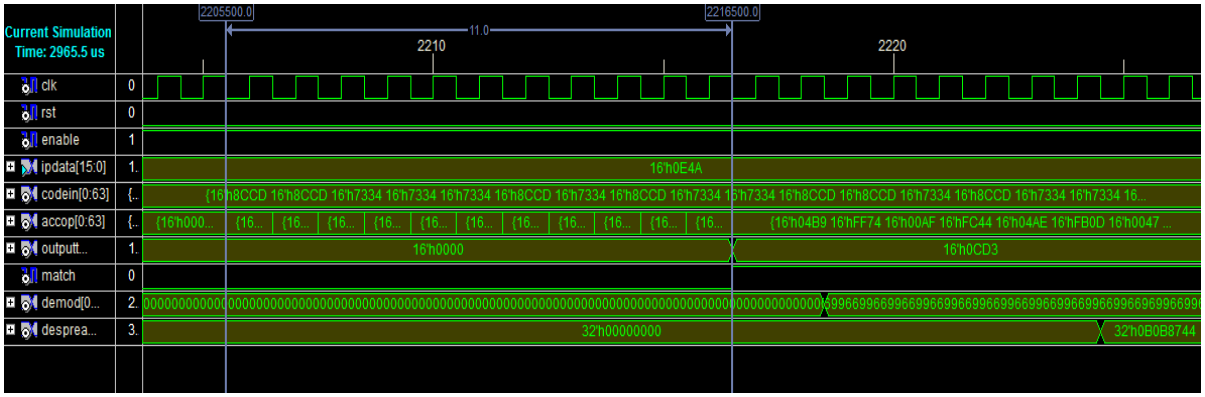

Fig.8. Simulation result for DMF technique.

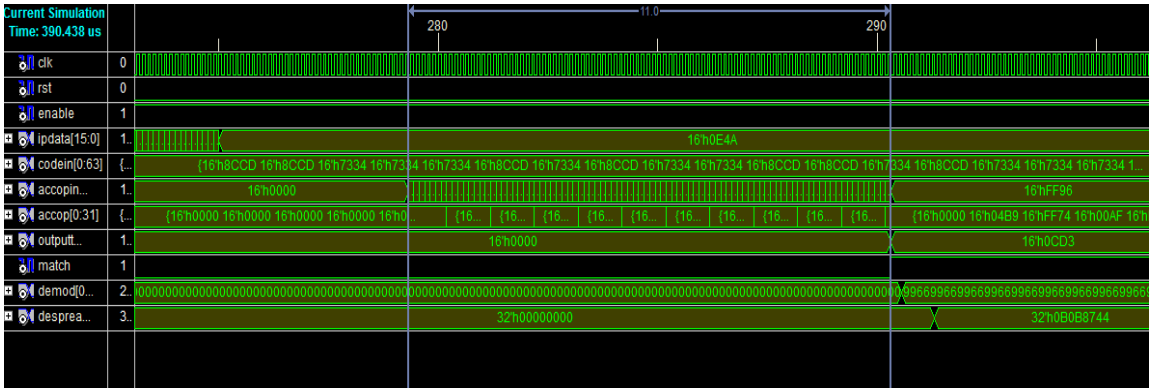

Fig.9. Simulation result for RDMF technique.

Fig.7 illustrates the simulation result of SDSS technique. Simulation results shows that the time taken for obtaining synchronization is about 704 microseconds. This can be infered using measure markers. Fig.8 and Fig.9 shows the simulation output for DMF and RDMF respectively. Time taken for obtaining synchronization using both Matched Filters is 11 microseconds. Thus time taken for synchronization using Matched filter is 'N' times lesser than that of the time taken by serial search technique, where 'N' is the length of the PN sequence (In these results, 'N' is chosen to be 64). From the results, it is to be noted that 'match' signal becomes one once the synchronization is obtained and it triggers the subsequent process of demodulation.

Table 2. BER values

	Despreading(Without averaging)		Despreading(With averaging)	
SNR	BER	No. of errors	BER	No. of errors
0	0.28125	18	0	0
5	0.140625	9	0	0
10	0.015625	1	0	0
20	0	0	0	0
30	0	0	0	0

Table 2 illustrates the comparison of BER performance between the despreading unit without averaging operation and despreading unit with averaging operation and proves that the despreading with averaging operation performs well in high SNR values as well as in very low SNR values.

Table 3. Resource utilization

Resource name	For digital design of SDSS	For DMF	For RDMF
Number of Multipliers	1	64	8
Number of 16 bit Adders	1	63	8

Table 3 illustrates the comparison of resource utilization based on the Hardware Description Language (HDL) design summary report. The number of multipliers and adders consumed by RDMF technique is N/K,

where K is the number of segments into which the code sequence is divided. Here, 'N' is 64 and 'K' is chosen to be 8 and hence the number of adders and multipliers (L=N/K) consumed is 8 each. This proves that RDMF can achieve acquisition with reduced number of hardware resources than DMF. From table 3, SDSS method utilizes only one multiplier and adder each, but it will take time for processing around 'N' times than that of DMF and RDMF.

For channel affected sequence, synchronization detection not occurs always at the correct position. For low SNR values, correlation output may not be large enough to cross the preset optimum threshold. At this juncture, acquisition point detection may become possible by analyzing the correlation output values for a sub-optimum threshold crossing. That is, if all possible correlation outputs doesn't cross the preset threshold, then they can be again compared with a second threshold which is lesser than the first one. This methodology of double threshold comparison results in notable reduction in the number of situations of missed frame detection or synchronization detection. Table 4 illustrates the number of failures in frame detection. It is experimentally observed that number of failures with double thresholding is 0 for SNR >= 5db.

Table 4. Number of frame detection failures

	No. of missed frames(for 100 iterations)	
SNR	Single threshold	Double threshold
0	14	3
5	9	0
10	5	0
20	0	0
30	0	0

VII. Conclusion

Synchronization techniques compared in this paper shows that the parallel synchronization techniques are suitable than the serial synchronization technique, which takes longer period of time to acquire the PN code. Also from the experimental results, it is shown that RDMF requires less number of resources as compared to the conventional DMF. This RDMF can be used for frame detection in OFDM (Orthogonal Frequency Division Multiplexing) applications. The methodology of double threshold comparison shows the improvement in BER performance in more noisy environments. And averaging operation has been added into the despreading module so as to achieve zero BER.

Acknowledgement

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References

[1]. Sanjay Kumar Jaiswal, Kumkum Maurya, Dheeraj Jain, Vijayendra Maurya, Design of DS-CDMA transceiver using BPSK modulation\Demodulation, World Applied Sciences Journal 16, Special issue on recent trends in VLSI design, Sep, 2012.
[2]. Andrea Goldsmith, Wireless communication, (2nd edition, Cambridge University press, 2005, 383–386)
[3]. Hong Gil Kim, Iickho Song, Sun Yong Kim, Jooshik Lee, PN code acquisition using nonparametric detectors in DS/CDMA systems, Signal processing, vol 80, issue 4, 2000.
[4]. Yi Wan and Zhongping Chen, A Novel Synchronization Method for DS CDMA Systems, IEEE International Wireless Communications and Mobile Computing Conference (IWCMC), 2012, 596-601.
[5]. STEL-2000A data sheet (Intel Corporation, Dec 15, 1999).
[6]. Sklar, Bernard, Digital Communications Fundamentals and Applications (2nd Edition, Prentice Hall, NJ, 2001).
[7]. Marwin K. Simon, Jim k. Omura, Spread spectrum communication Handbook (McGraw Hill, 2002, 765–767).
[8]. Scheim J, Optimal search resolution for single dwell serial-search code phase synchronization in DS-SpSp, 59th IEEE Vehicular Technology Conference, Vol. 3, 2004, 1406-1410.
[9]. Chengfeng Ruan, Jingyu Hua, Zhilong Zheng, Yuan Wu, Limin Meng, A Study Of Different Matched Filters In Digital Down Converter, IEEE International Conference on Systems and Informatics (ICSAI), 2012, 2059-2063.
[10]. Y.T. Su, Rapid Code Synchronization Algorithms Employing PN Matched Filters, IEEE Transactions on Comm., Vol. 36, No. 6, June 1988, 724-733.
[11]. L.B. Milstein, J. Gevargiz, P.K. Das, Rapid Synchronization for Direct Sequence Spread-Spectrum Communication Using Parallel SAW Convolvers, IEEE Transactions on Comm., Vol. 33, No. 7, July 1985 ,593-600.
[12]. Nuan Song, Mike Wolf, Martin Haardt, A b-bit Non-Coherent Receiver based on a Digital Code Matched Filter for Low Data Rate TH-PPM-UWB Systems in the Presence of MUI, IEEE International Conference on Communications, 2010.
[13]. Mark D. Hahm, Eby G. Friedman, Edward L. Titlebaum, A Comparison of Analog and Digital Circuit Implementations of Low Power Matched Filters for Use in Portable Wireless Communication Terminals, IEEE Transactions on circuits and systems-II, volume 44, June 1997, 498-506.
[14]. Zhang Zhang, Qingqing Yang, Lingkai Wang, Xiaofang Zhou, A Novel Hybrid Matched Filter Structure for IEEE 802.22 Standard, IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2010, 498-506.
[15]. Bruce Tang , David E. Dodds, Synchronization of weak indoor GPS signals with doppler using a segmented matched filter and accumulation, IEEE Canadian Conference on Electrical and Computer Engineering, 2007,1531-1534.