VLSI Architecture for MB-OFDM Transmitter

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Abstract: *(MB-OFDM) Multi-Band Orthogonal Frequency Division Multiplexing is a suitable solution for implementation of high speed data transmission in ultra wideband spectrum by dividing the spectrum into available multiple bands. In MB-OFDM system the most important part is base band of transmitter.   In this paper introduced the structure of MB-OFDM system transmitter and the design of transmitter baseband based on FPGA is described in detail. Quartus2 which allow the synthesis of Vhdl code on to Alter's FPGA chip or Xilinx's ISE suit for Xilinx's FPGA chip. The results show that all designed modules has achieved the expected purpose both in precision and resource.*

Keywords: *OFDM,UWB,Scrambler,encoder,puncturer,Interleaver,QPSK,IFFT*

I.   Introduction

In recent years, UWB communication systems have been getting attention from both the industry and the academia. In Feb 2002, the Federal Communications Commission (FCC) allocated 7,500 MHz of spectrum (from 3.1 GHz to 10.6 GHz) for use by UWB devices [1, 2]. This rules has helped to invent new standardization efforts, like IEEE 802.15.3a [3], that focus for developing high speed wireless communication systems for personal area network. A multi-band orthogonal frequency division multiplexing(MB-OFDM) ultra wideband (UWB) system being consider for physical layer of the new IEEE (WPAN) wireless personal area network standard, IEEE 802.15.3a [3]. 480Mb/s over 1 meter , 220 Mb/s over 4meters ,and 110 Mb/s over 10 meters, are the set standard goals at the high data transmission rates .(FPGA)Field programmable gate array technology is not only key technology in digital system, but also plays an important role in application specific integrated circuit (ASIC) design field because of its higher integration and design flexibility and the technical line for the implementation of MB-OFDM transmitter baseband module with Xilinx Virtex II series FPGA is introduced in this paper. It has been proved by the simulation results that the design of MB-OFDM transmitter baseband based on FPGA has good characterizes such as easy implementation ,simple structure, , high reliability and so on.

Table 1.Summery of PHY requirement

Parameter	Value
Bit rate (PHY Layer)	110Mbps,200Mbps,480Mbps
Range	10m,4m,2m
Power Consumption(PHY Layer)	100MW,250MW
Target bit error rate	10^{-5}
Co-located piconets	4

II.   Literature Survey

1] Xu Jinsong, Lu Xiaochun, Wu Haitao proposed implementation of MB-OFDM transmitter baseband based on FPGA,2008. They design all modules of MB-OFDM transmitter system using VHDL language, and simulate and verified it using model-sim and later on they synthesis the design using Xilinx Virtex II FPGA, they address the designs approach for all modules in details .

2] Anuj Batra proposed work on design of a multiband OFDM system for realistic UWB channel environments in September 2004.They design and analyze the MB-OFDM system [Tx and Rx] in more details against. the AWGN channel variation. They give methodology for finding the data rate against the variation in dist and AWGN channel. Also address the technology process variation [90nm , 130nm] for implementation and analyze for transmitted power and received power with variation in data rate .Give more elaborated parameter analysis for MB-OFDM communication system.

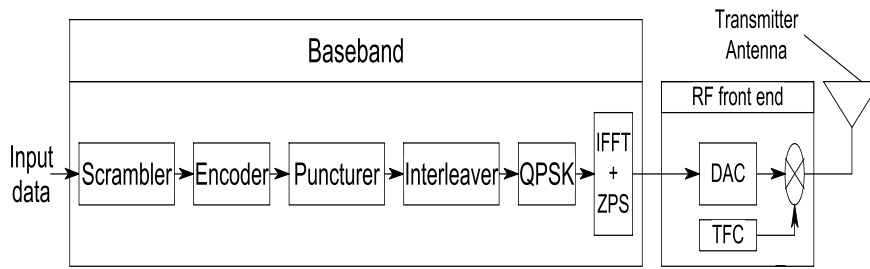### III.   MB-OFDM Transmitter Baseband Structure

Fig 1: MB-OFDM transmitter,

Fig.1 MB-OFDM system shows the transmitter. Input data is send to scrambler . it is used for security purpose. Then data fed to Encoder we can use Recursive type encoder or Non-Recursive type encoder. Non – Recursive type encoder is also called as feed-forward encoder, in this data goes to forward direction. data is feedback in Recursive encoder. constraint length is depend upon the number of flif-flop use and code rate is 1/3. Therefore Non-recursive encoder is more suitable. Then data is goes to Puncturer, it is increase the rate of given data. In Interleaver non-linear data stream is using hence we get less error. more error will get if we use linear pattern bit stream. QPSK is digital modulation technique. Zero-Padded suffix (ZPS) is appended to the modulated signal and then modulate these signal to various sub-band through RF front-end. Finally, the modulated signal is transmitted on various sub-band by antenna. The baseband is the core of a transmitter system.

3.1 Source of transmitter
We are designing FSM in active HDL for generation of input data obviously input data is in the form of binary number.
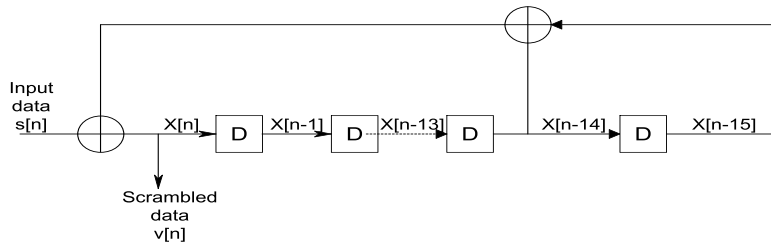
3.2 Scrambler

Fig 2.Block diagram of the scrambler

In telecommunication, a scrambler is a device that transposes or inverts signals or   otherwise encodes a messege at the transmitter to make the message unintelligible.
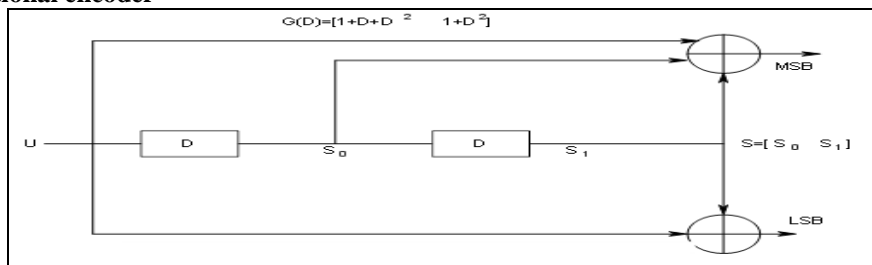
3.3 Convolutional encoder

Fig 3. Non-Recurcive encoder

In telecommunication, a convolutional code is a type of error-correcting code in which each m-bit information symbol (each m-bit string) to be encoded is transformed into an n-bit symbol, where m/n is the code rate ($n \geq m$) . length of the code.

3.4 Puncturer

Puncturing is the process of deleting some bits from the codeword according to a puncturing matrix. The puncturing matrix (P) consists of zeros and ones where the zero represents an omitted bit and the Puncturing can be applied to both block and convolutional (matlab representation of matrix) .
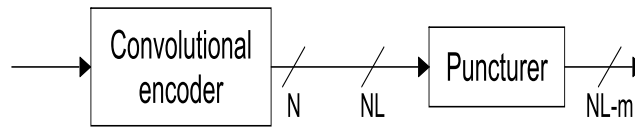

Fig 5. schematic of Puncturing

3.5 Interleaver

An interleaver is a device that rearranges the ordering of sequence of symbols in a deterministic manner. Interleaver is a device that mixes up the symbol from several code words so that the symbol from any given codeword give a random effect. When the Deinterleaver reconstruct the codeword by arranging the received sequence to it's original order , error burst introduced by the channel are broken up and spread across several codeword. Interleaver were used practically serially concatenated codes and in multipath coding channel to enhance the overall error correcting capability of the coding scheme. they were used differently for the first time in a parallel concatenated code and proved to reduced the number of code words with small distance in a code distance spectrum(i.e. generates less code words with minimum hamming distance).
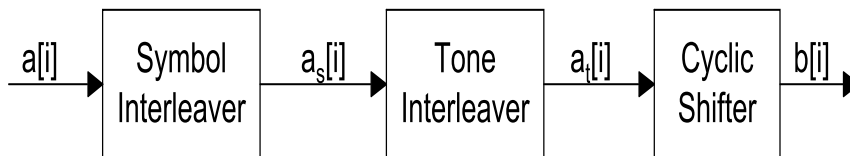

Fig 6. A block diagram of the various stages of the bit interleaver

3.6 QPSK

QPSK systems need only digital demux circuit .The coded and interleaved binary serial input data will divide into groups of two bits and converted into a complex number representing one of the four QPSK constellation points.
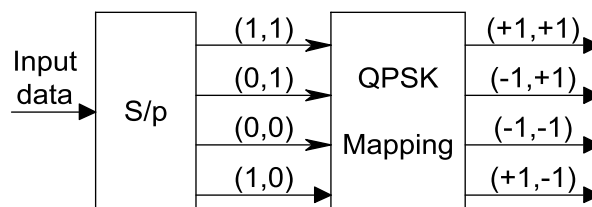

Fig 7. QPSK mapping

3.7 IFFT

IFFT is a core of the baseband of MB-OFDM transmitter. The bit streams will be modulated on various frequencies carrier by IFFT. In many applications high-speed performance is required. The speed enhancement is the key contribution of the main processing blocks in OFDM system .This proposed work will provide high speed data transmission in ultra wideband spectrum by dividing the spectrum available into multiple bands. Field programmable gate array (FPGA) technology is a key technology in digital system.

IV.   Frequency Planning And Synthesis Circuit

The frequency planning shown in Fig below was chosen for two specific reasons. First, it allows sufficient guard band on the lower side of band 1 and the upper side of band 3 to simplify the design of a pre-select filter, which is used to attenuate the out-of-band signals.
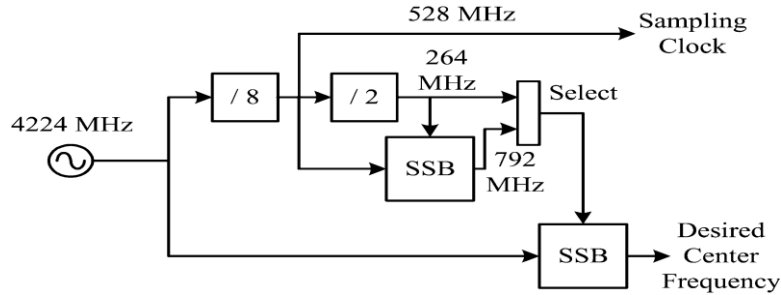
Fig 8. Example synthesizer architecture that can switch between frequencies within a few nanoseconds.

V. System Parameter

This system is capable of transmitting data at information data rates of 55, 80, 110, 160, 200, 320,and 480 Mb/s. This system employs an OFDM scheme with a total of 128 sub-carriers. from 128 sub-carriers, only122 tones carry energy. Of the 122 sub-carriers, 100 are devoted to data, 12 are assigned to pilot tones, and the remaining ten are guard tones. In addition, the 122 sub-carriers are modulate during quadrature phase-shift keying (QPSK). By limiting the constellation size to QPSK, we can reduce the internal precision of the digital logic, specifically the (IFFT) inverse fast Fourier transform and FFT, and limit the precision of the ADCs and DACs. This help to reduce the overall complexity of the system
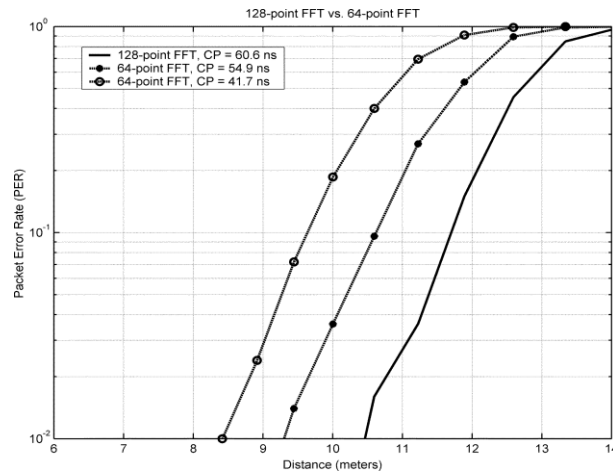

Fig 9: PER as a function of distance, and FFT size and   prefix length for a data rate of 110 Mb/s.

VI. Architectyre For A Multiband Ofdm System

In Fig10.shows one realization of a time–frequency code, where the first OFDM symbol is transmitted on sub-band 1, the third OFDM symbol is transmitted on sub-band 2, the fourth OFDM symbol is transmitted on sub-band 1, and so on. For the sake of simplicity, this example shows a multiband OFDM system employing only three sub-bands and using a time–frequency code of length 3. In practice, the time–frequency code can be quite different and much longer in length. The time–frequency codes are used not only to provide frequency diversity in the system, but also to provide multiple access. From Fig. 9,
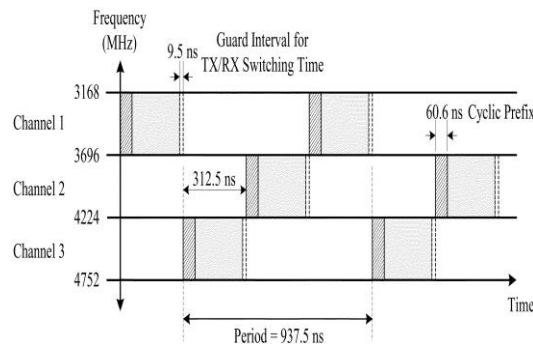

Fig 10: Example of time–frequency coding for the multiband OFDM system

The guard interval ensures that only a single RF transmit and RF RX chain are needed for all channel environments and all data rates and that there is sufficient time for the TX and RX to switch between the different center frequencies.

VII.   Optimul Operating Bandwidth

In Fig. 10, the received signal power as a function of the upper frequency is plotted for a distance of 10 m. From this figure, it can be seen that the received power increases by, at most,2.0 dB (3.0 dB) when the upper frequency is increased to 7.0GHz (10.5 GHz). results in the RX noise figure increasing by at least 1.0 dB (2.0 dB). however, this comes at the expense of higher complexity and higher power consumption in current CMOS technology.
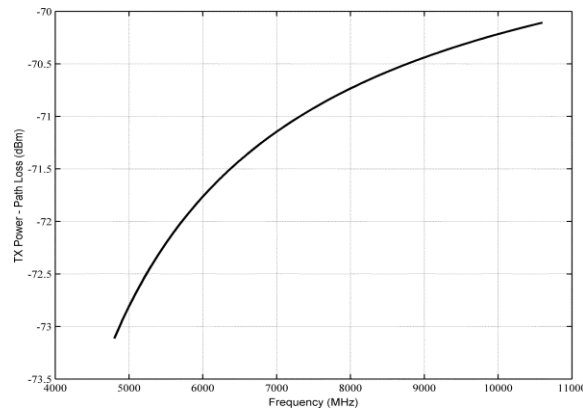

Fig 10.1.Received power as a function of upper frequency

Table 2. multiband OFDM system parameters

Info.data rate	110Mb/s	200Mb/s	480Mb/s
Constallation	QPSK	QPSK	QPSK
FFT size	128	128	128
Coding rate(K=7)	R=11/32	R=5/8	R=3/4
Frequency domain spreading	No	No	No
Time-domain spreading	yes	yes	No
Prefix Length	60.6ns	60.6ns	60.6ns
Guard Interval	9.5ns	9.5ns	9.5ns
Symbol Length	312.5ns	312.5ns	312.5ns
Channel Bit Rate	640Mbps	640Mbps	640Mbps

VIII.   Simulation

Using the design methods above, the simulation of each module for MB-OFDM transmitter baseband which has been validated with ALTERA FPGA is given.
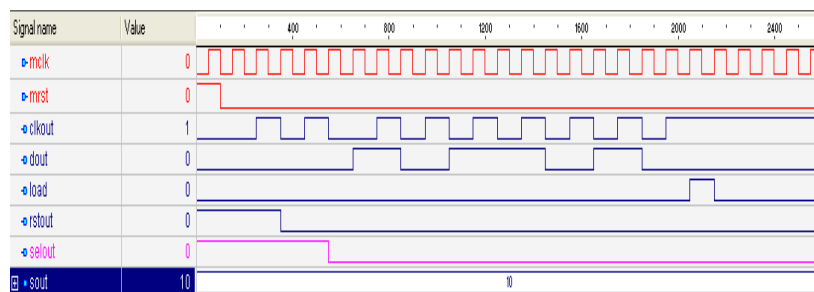

Fig.11 The simulation of the transmitter signal source generation.

This is the input source of system in this waveform we are giving 8bit data which is 01011010. When sellout is one that time seed value is given to the scrambler. when sellout is zero that time eight bit input data is send. Now in below fig. we are increasing the input source that means adding two 8 bit data.
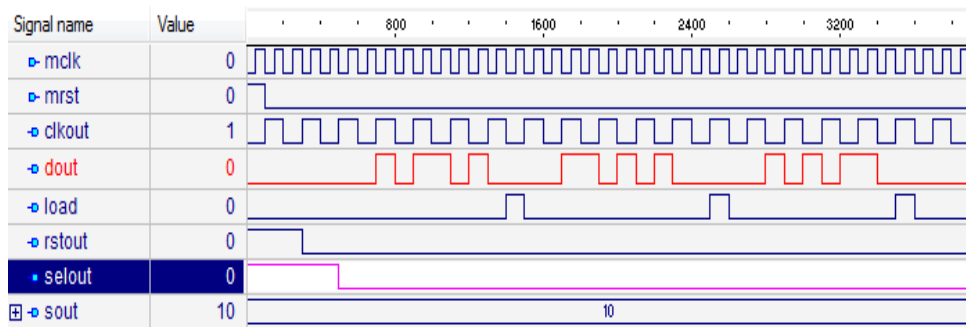
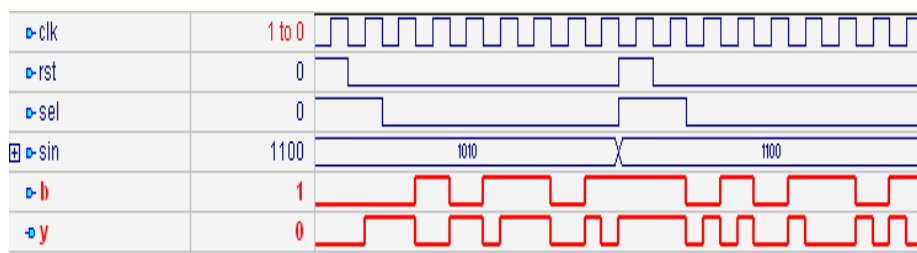Fig.11.1 The simulation of the transmitter signal source generation.

Fig. 12 Simulation of Srambler

Fig.12 shows the simulation of scrambler. The data out inFig.12 is the output of scrambler. Which is indicated by Y seen in Fig.12, the input data of scrambler is randomized by scrambler. The scrambler has been initialized with the same initialization vector, which is determined from the seed identifier contained in the PLCP header of the received frame [n].
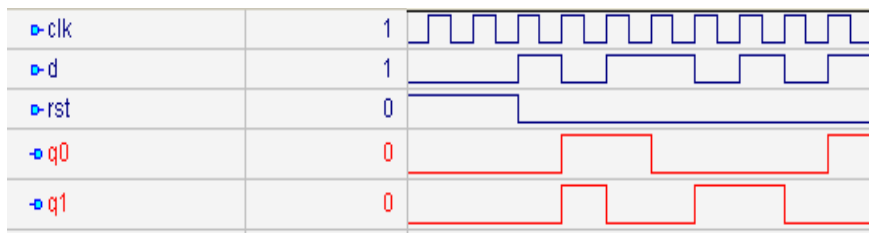
Fig.13 Simulation of Convolutional Encoder

Fig.13 shows convolutional Encoder. In that d is input data and q0,q1 shows output data. Code rate is ½ achieved by convolutional encoder.
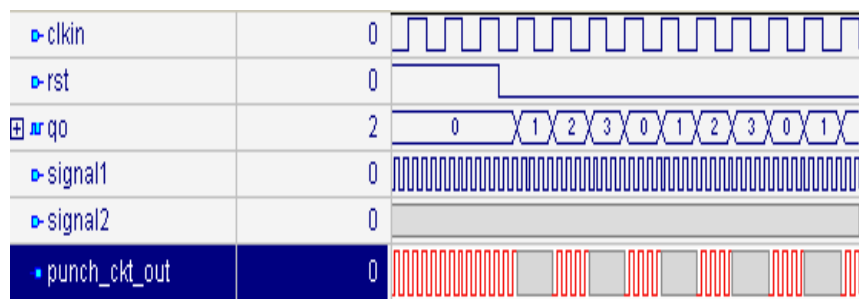
Fig.14. the simulation of Puncturing

Fig.14 shows the simulation of puncturing based on FPGA. After puncturing, the R=1/1 code rate is obtained from R=1/2 bit streams. The various code rates can be achieved by puncturing according to requirements.

The simulation of interleaver is expressed in Fig.15. Data in is the input of interleaver and dataout is the output of interleaver. The order of bit streams is psuedorandom when bit stream passes through interleaver.
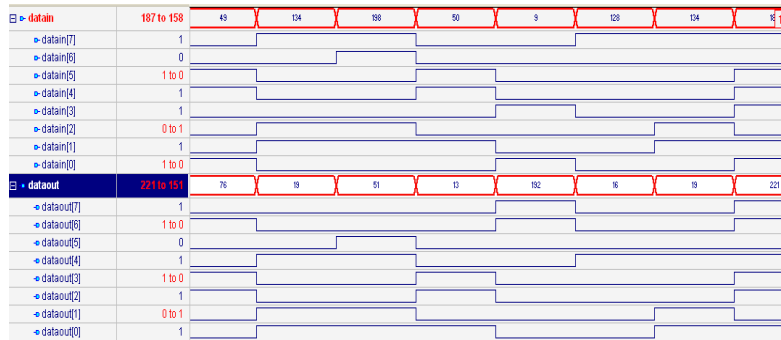

Fig. 15 Simulation of Interleaver.

Fig.16 shows the simulation of QPSK mapping . After QPSK mapping, the input bit streams takes two different roads. .According to QPSK mapping relation, input data is modulated to complex signal which can be seen from Fig.15.
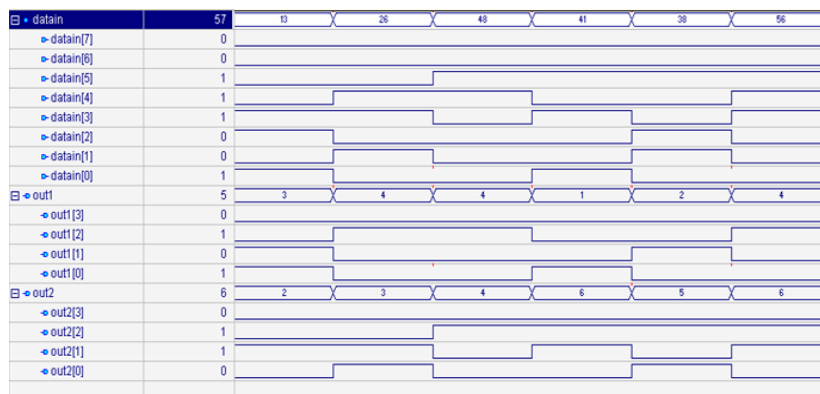

Fig.16 Simulation of QPSK

The IFFT simulation results are given in Fig.17. The input data is modulated on different sub-carrier by IFFT. It has seven clock signals input in this figure because time (TD) based on radix-2 128-point FFT is selected in this system. The output of IFFT shown in fig. below.
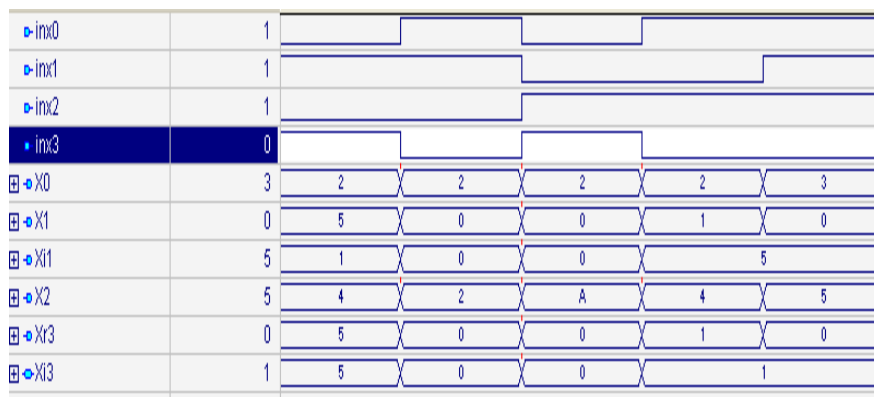

Fig.17 Simulation of IFFT

The simulation of transmitter baseband is shown in Fig.18 and the synthesized report of whole transmitter baseband is obtained in Fig.19. The real and imaginary parts of transmitter baseband output are described by "xk_re" and "xk_im" in Fig.17respectively. As shown in Fig.18, the occupied resources which uses FPGA to implement MB-OFDM transmitter.
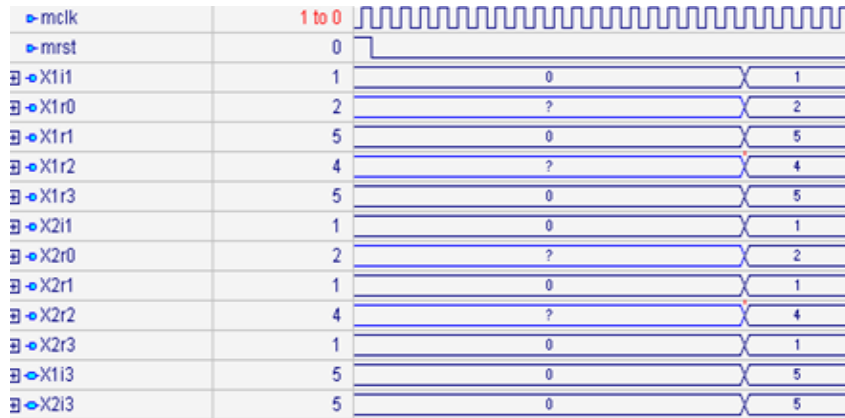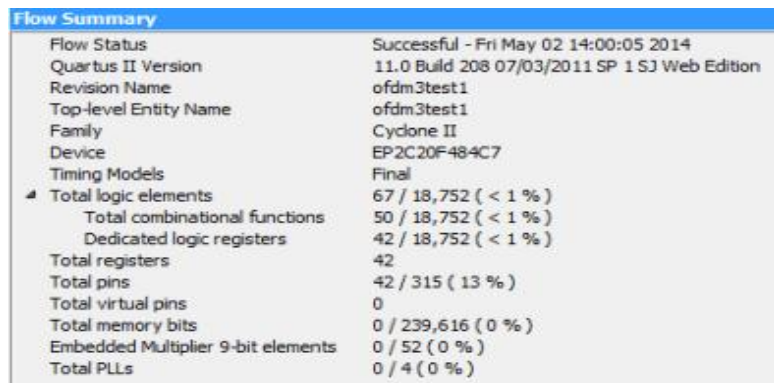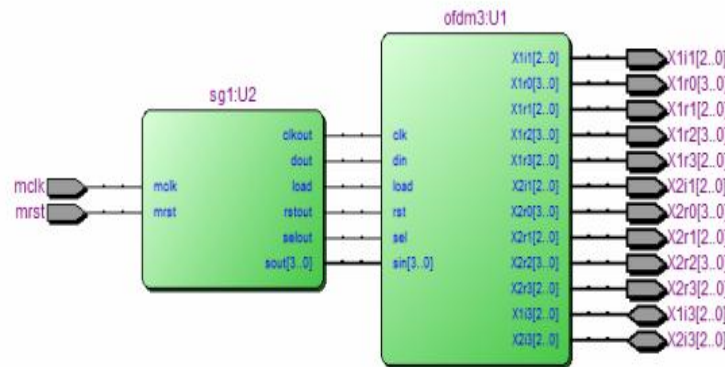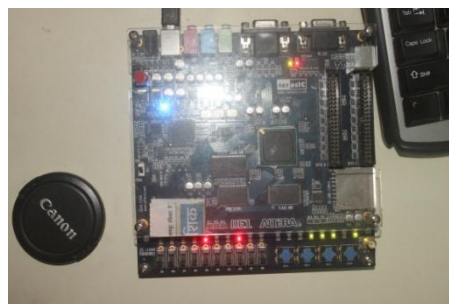
Fig.18 simulation of Transmitter

Fig.19 Synthesis report of OFDM

RTL view of baseband of transmitter.

Result show on Altera cyclon2 FPGA kit

IX. Conclusion

This project will implement as system level design in HDL language we will prefer the know language that is VHDL. In FPGA implementation we have to do both things simulation and FPGA realization in that case /for that there is a need of FPGA kit either xilinx or Altera. Finally after the compilation it will give an generalized information or result regarding total LE [logical elements] consumes which reflects the size[small/large] of the circuit ,RTL view which is nothing but a system overview block diagram, power consumption which is out come of power play analyze tool which is incorporated itself in altera / xilinx , it will give power depending on the switching activity of the signal. Normal power formula is $p = c*vdd^2*f$ where C= total capacitance , which is fix obvious. Vdd = fix supply voltage , which is also fix obvious. F = is switching frequency , which can be control by user.

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