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Performance Estimation of SVL technique based ½ frequency divider in 45nm CMOS technology

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Abstract: *The design is chosen to accomplish the desired necessity in present work we design high broadband frequency divider. It consumes less power and gives low leakage in CMOS based frequency divider with SVL technique, thereby reducing overall power consumption of the circuit. This paper presents various parameters and shows reduced leakage power (0.45×10^{-12}), Delay (6.26psec) and noise margin (11.53) of the circuit to analyze its performance in 45nm technology with U-SVL and L-SVL technology. The simulation results were done with cadence tool virtuoso environment at room temperature 27ºC with various supply voltage (0.7 to 1.2V).*

Keywords: *Cadence virtuoso tool, delay, Frequency divider circuit, leakage power, SVL technique.*

I. Introduction

The potential of CMOS frequency divider for high speed applications has been conventional in numbers of circuits, low voltage operations and low power consumption in CMOS based dividers makes them suitable for compact integration of communication system [1]. Basic gates and flip-flops can be used to design frequency synthesizers, timing recovery circuits and clock generations. Besides that, large number of buffer amplifiers is built into a single chip which creates power dissipation problem. Frequency dividers are categories under three points (1) Flip-Flop based, (2) Injection-locked, and (3) Regenerative frequency dividers. Injection locked frequency dividers utilize an oscillator whose center frequency is locked to harmonic incoming signal frequency [4]. The ½ frequency divider employs two D latches in a master slave configuration with negative feedback [2]. While dynamic and injection- locked dividers can attain high frequencies at low power consumption. This paper focuses on the design of a frequency divider that can be functional toward massively parallel I/Os, in which broad frequency range [7], area and power are the key criteria. Wireless communication industry shows terrific growth and in wireless LAN applications the IEEE 802.11 multiple standards have been extensively adopted for the short-range communication [9]. The frequency synthesizer, which is usually formed by a Phase locked loop (PLL), is a major and critical part of a wireless transceiver because it operates at high frequency and consumes a large portion of the total power consumption in transceivers [13]. Several different principles of operation such as 2.4GHz 82.11 b/g and 5.2GHz 802.11a HIPERLAN-2 networks are used, and thus a multi standard frequency synthesizer is enviable for operations under different wireless systems [14]. The performance in power utilization and channel selection of a frequency synthesizer are limited by the two important building blocks, namely frequency divider and voltage controlled oscillator (VCO). Recently, battery operated wireless communication has become admired for many applications to reduce the battery size, the power consumption of the PLL, which generally consumes the largest sum of power in a wireless front end, needs to be compact [11]. In particular, high speed frequency dividers consumption of large amount of power in PLL based devices, decreasing the number of stages by increasing the division order is efficient for the power reduction of the frequency divider. The paper carried out with new SVL (self voltage control) synchronies in circuit through which low power consumption is introduced into frequency divider circuit. This will further verified into two sections including L-SVL and U-SVL technique synchronized with divider circuit, which enhance whole circuit performance in 45 nm technology.[12], [15].

II. Circuit Description

2.1. Frequency Divider

The divider circuit illustrate Razavi topology, it consist of two latches connected in master/slave arrangement. Flip –Flop is trigger with two complementary clock signals cka & ckb [5]. Two Flip-Flop work sporadically & alternatively between two modes. When input signal ck is at small level one latch is in sense mode (it receive data at its input D and it occupy then into its output Q) while other is in latch mode (it keeps the prior output) when input signal ck goes to high level, the flip-flop changes there modes of function [4] This mechanism outcome that frequency from output signal (Q & QB) can be half that of input (CK & CKB) fig.1 shows the divider circuit, each latch contains two sense devices (M1 & M2 in the master and M7 & M8 in slave mode), a regenerative loop (M3 & M4 in the master and M6 & m16 in slave mode), two pull up devices (M5 & M6 in the, master and M11 & M12 in the slave).

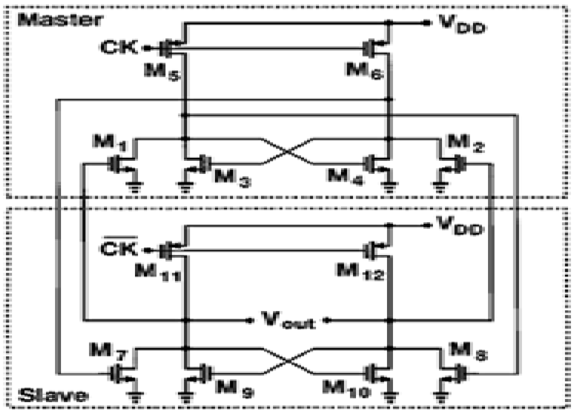

Fig. 1. Shows the circuit description of frequency divider

when CK goes high, M5&M6 are off stage, and the master is in sense mode, while M11 & M12 are on slave mode which shows store mode. When CK goes low, the reverse occurs [15]. The circuit based on stacked or pass transistors and also a gate channel capacitance of PMOS transistors almost not affects the critical path as these devices are saturated in the order of for the entire voltage swing at nodes, x1, y1 and x2, y2. In order to usual latch topologies the d-latch circuit used in divider does not disable it's I/P devices then it leads to sense to store mode. While this would causes timing problems in general digital circuit [14], [9]. Above figure 1, Shows the circuit diagram of frqunCy divider with the master nad slave circuit in 0.7V power supply in 45nm technology

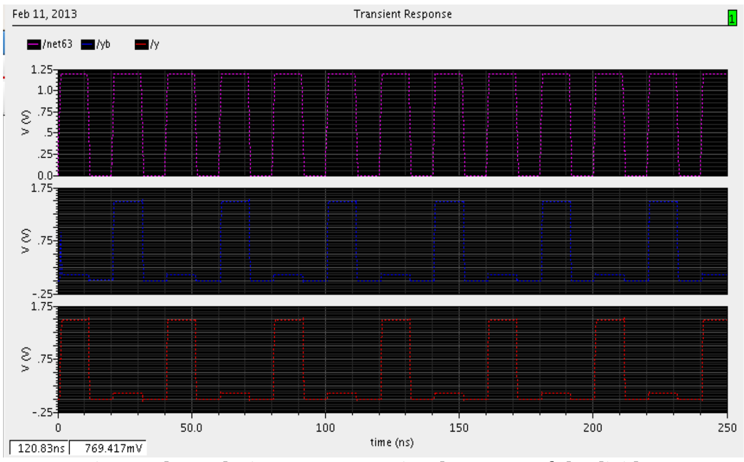

Fig. 2. Shows the input & output signal response of the divider.

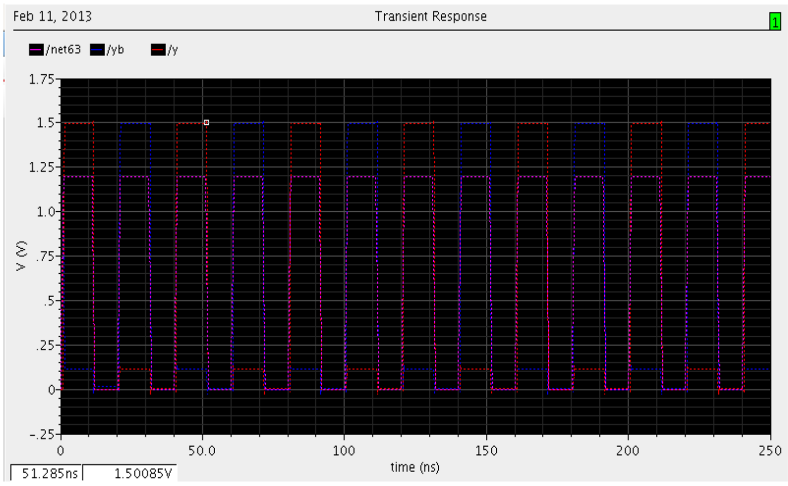

Fig. 3. Shows the input output response of frequency divider with SVL technique

Above figure 3, Shows the input and output waveforme of frequncy divider cicuit with 0.7V power supply in 45nm technology

1.2. SVL Technique

1.2.1. Frequency divider with U-SVL technique

A frequency divider using U-SVL scheme is shown in Figure 4. In this design, full supply voltage of VDD is applied to the transistor. The U-SVL circuit is intended on a wide channel pull up p-MOSFET switch (p-SW) and several n-MOSFET resistors (n-RSm) connected in series.

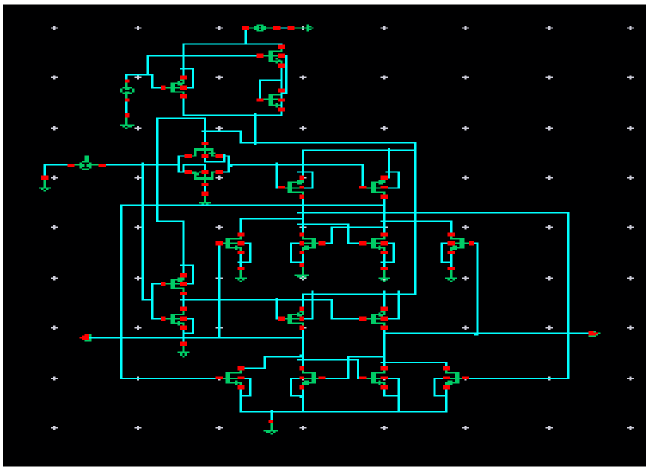

Fig. 4. Digram shows U-SVL with divider attached

1.2.2. Frequency divider circuit with L-SVL technique

Figure 5 shows a schematic of a frequency divider cell in which L-SVL scheme is functional. The switch provides 0 Volt at the ground node and a raise ground level (virtual ground). The L-SVL circuits initiates a wide channel pull down n-MOSFET switch (n-SW) and multiple series connected p-MOSFET resistors (p-RS).

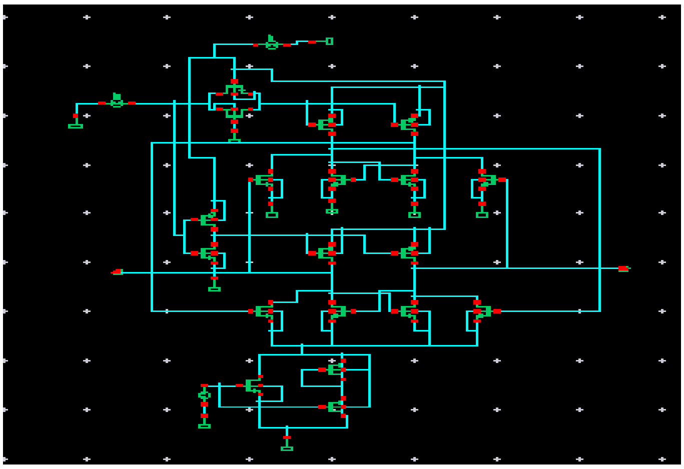

Fig. 5. Shows L-SVL with divider circuit.

1.2.3. Frequency divider with SVL technique

The SVL circuit exhibits of an upper U-SVL circuit and a lower L-SVL circuit, in it a single inverter is used as load circuit. The SVL circuit shown in Figure 6 is applied to the frequency cell array. The U-SVL circuit is designed on wide channel pull-up p-MOSFET switch (p-SW) and multiple n-MOSFET resistors (n-RSm) coupled in series. Similarly, L-SVL circuit inbuilt a wide channel pull-down n-MOSFET switch (n-SW) and numerous series connected p-MOSFET resistors (p-RSm). While the load circuit is active (i.e., CLB = 0 and CL = 1), both pSW, nSW are turned on, but the nRS1 and pRS1 are turned off. That's why, U-SVL and L-SVL circuits can supply maximum supply voltage VD = VDD and a minimum ground-level voltage VS (= VSS = 0), respectively, to the active load circuit. Thus, the operating speed of the load circuit can be maximized.

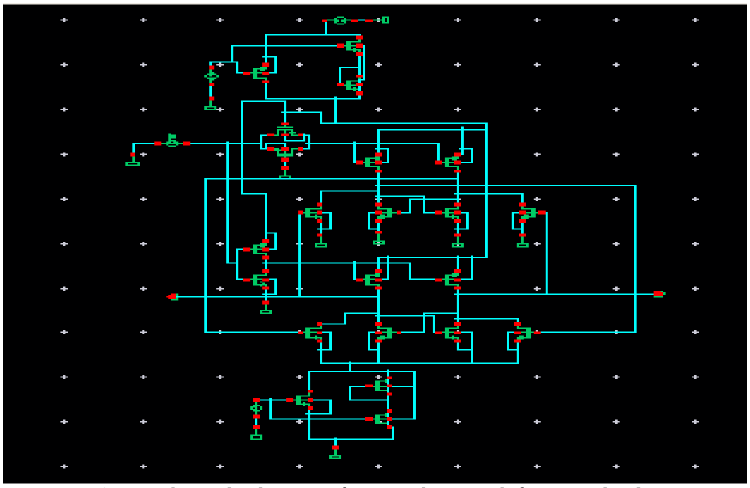

Fig. 6. Shows the diagram of SVL technice with frequncy divider

When the load circuit is in stand-by (i.e., CLB = "1" and CL = "0"), all the nRSm and pRSm switches are turned on, and both the p-SW and n-SW are turn off. Thus, the U-SVL and L-SVL circuits correspondingly generate a lower supply voltage VD = VDD vn < VDD and a comparatively higher ground-level voltage VS = VP > 0V, where vn and vp are the total voltage drops of all n-RSm and all p-RSm, correspondingly. Thus, back-gate biases (VBGs) {i.e., source voltages} of both "cut-off" p MOSFETs and then n MOSFETs in the stand-by load circuit this increased vn and -vp, respectively. The increase in VBGs will increase the Vts of the "cut-off" MOSFETs. Therefore, leakage currents of the "cut-off" MOSFETs decrease. Further, it increase in Vs increases the "write" operating edge. Similarly, the Vdss of the "cut-off" MOSFETs decrease and becomes VDD-(vn+vp). Decreasing Vds will decrease effect of drain-induced barrier, so that leakage current decrease even more. In addition, SVL circuit not only reduces the Vgd of the "cut-off" .MOSFETs but also reduce the Vgc of the "turn-on" MOSFETs. Decreasing Vgd reduces the GIDL currents of the "cut-off" MOSFETs and decreasing Vgc decreases the gate quantum tunneling leakage currents of the load circuit will greatly decreases.

III. Simulation Result

The circuit work simulated in cadence for 45nm technology, from the result table, we are getting effective and average reduction result in delay, leakage power and noise margin with SVL technique compare to U-SVL and L-SVL technique.

3.1. Leakage Power

In frequency divider either the transistors are in off mode or in ON mode due to the early switching of opposite level leakage is introduced into the devices. The power consumption in frequency divider consume a power off 1.66nW, with U-SVL and with L-SVL technique power consumes is 5.16nW then, we finally getting the average result of frequency divider with SVL (both U-SVL & L-SVL) technique 0.45pW so we achieved a power reduction of (0.45×10^{-12}), this shows more power reduction in comparison to U-SVL & L-SVL at 45nm technology, so from this we analyses a power reduction of 24% using SVL technique with frequency divider. It can also be observed through varied supply voltage as shown in comparison table below;

$$P_{leakage} = I_{leakage} \times V_{dd} \tag{1}$$

Where, $I_{leakage}$ = leakage current and V_{dd} = power supply.

The leakage power is calculated by this formula and we calculate the effective power in frequency divider with SVL technique (0.45×10^{-12}) with supply voltage Vdd= 0.7V

Table 1. Shows the Leakage Power

Voltage	Leakage power of frequency divider	Leakage power with U-SVL tech	Leakage power with L-SVL tech	Leakage power with SVL tech(both U-SVL and L-SVL)
0.7V	2.01×10-6	1.66×10-9	5.16×10-9	0.45×10-12
0.8V	11.16×10-6	2.13×10-9	6.53×10-9	5.63×10-12
0.6V	16.02×10-6	6.45×10-9	13.01×10-9	11.15×10-12
1.2V	21.02×10-6	11.02×10-9	16.06×10-9	13.11×10-12

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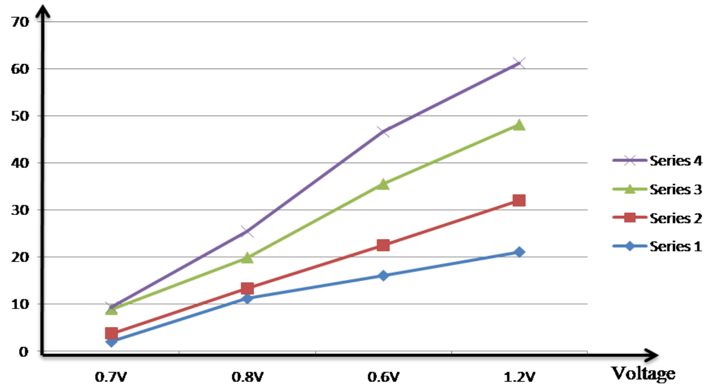

Fig. 7. Shows the greaph of Leakage power analysis

3.2. Delay

The time difference between the input increasing the reference voltage and output changing the logic state is known as the propagation delay, propagation delay time of frequency divider generally varies as a function with amplitude of input a larger input will result in a smaller delay time. Delay time of the circuit is measured as the average of response time of gate for positive, negative output transition of sine wave. The comparative analysis of various circuit delay time is shown below.

Table 2. Shows the Delay Analysis

Voltage	Delay of frequency divider	Delay with U-SVL tech	Delay with L-SVL tech	Leakage power with svl tech(both U-SVL and L-SVL)
0.7V	11.16nSec	6.16nSec	2.06nSec	6.26pSec
0.6V	19.02nSec	5.46 nSec	3.11nSec	11.65pSec
0.8V	23.14nSec	6.51 nSec	5.16nSec	17.68pSec
1.2V	27.04nSec	14.03nSec	6.011nSec	26.1pSec

Delay will reduce when the voltage is increased, the main goal of using the frequency divider in our project, that we can set the threshold limits as per our requirement. In this we observe that SVL based frequency divider gives a better performance as compared to L-SVL frequency divider and U-SVL frequency divider,

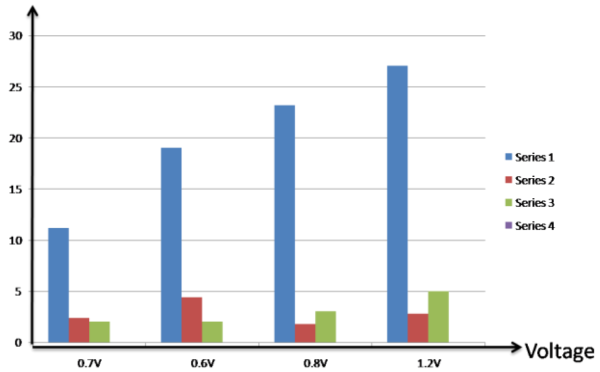

Fig. 8. Shows the greaph of Delay analysis

Due to lower threshold voltage of frequency divider, we also observe that the signal rise and fall time lower provides fast signal propagation and less delay in 45nm technology.

3.3. Noise Margin

The voltage difference between the graduate output level and the required input voltage level of a circuit is known as noise margin and we get the effective result with SVL technique as compare to U-SVL, L-SVL and conventional frequency divider, which is show below through the comparative analysis.

Table 3. Shows the Noise Margin

Voltage	Noise margin of frequency divider	Noise margin with U-SVL tech	Noise margin with L-SVL tech	Noise margin with SVL tech(both U-SVL and L-SVL)
0.7V	2.11	6.51	2.73	11.53
0.8V	3.01	6.11	4.12	13.01
0.6V	4.10	14.61	6.68	16.11
1.2V	7.11	16.41	6.12	17.10

IV. Conclusion

Proposed Frequency divider is modified by using transistors having less average power consumption with decreases in area, delay is also decreased by using only six PMOS as because delay is more concentrated to PMOS due to less mobility of holes compared to electrons, SVL based Frequency divider is created by using transistor and have better performance than the U-SVL and L-SVL Frequency divider as there are fewer transistor counts by which area is reduced and delay is also reduced; the average power consumption of the proposed Frequency divider is less in comparison to the conventional Frequency divider, measured result correctly verified the principle of operation and characteristic of the low-power Frequency divider circuit. The circuit has been used for the design of low power.

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