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Comparitive analysis of power optimization using mtcmos, transistor sizing & combined technique on 180nm technology

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Abstract: *This is a review paper in which we use various techniques for low power optimization and with the help of these techniques we perform comparative analysis. Evolution in VLSI continuously reduce the silicon technology to fulfill the increasing demands for higher functionality, low power and better performance at low cost. In today's scenario, low power design becomes an important issue. Most of the power consumption takes place during switching events i.e. dynamic power. This paper present various basic circuit in which reduction in power consumption takes place due to transistor sizing as well as MTCMOS technique separately and then we will also design the same circuit by the combination of the above two techniques which consume overall less power than conventional CMOS circuitry. Basic circuit are fundamental components of any digital design. We also see the effect of voltage scaling on these circuit and reduce the circuit using shannon's expansion theorem without changing in functionality ,to reduce the transistor count so that power decrease. The investigation has been carried out with simulation run environment on cadence virtuoso design editor using 180nm CMOS process technology at 1.8 V.*

Keywords: *MTCMOS, transistor sizing, Combined MTCMOS & transistor sizing, shannon's expansion theorem*

I. Introduction

Power optimization is a process in which power is reduce in a circuit in such a manner that it will not affecting the circuit performance**.** We require low power circuit because we know (1) To enhance the performance of a circuit and to integrate more function on a chip, the feature size is reduce, so power dissipation per unit area rise and hence increasing the chip temperature. To maintain this large cooling devices are required which enhance the cost of device. (2) Heat gradient across the chip also causes thermal and mechanical stress leading to easily breakdown of chip. (3) Technology continuously scale down so enhance power density and also current density which causes problems such as electro-migration, hot carrier induced device degradation.(4) Demand of portable system increases.

II. Fundamental Logic Design

2.1 CMOS NAND

CMOS NAND design consist 4 transistors. This circuit built by equal number of NMOS and PMOS transistor. The circuit diagram of 4T NAND circuit implemented on cadence virtuoso design editor is shown in Fig.(a) where Y =(AB)'.The output is high when both the input is low otherwise the output remains low.

2.2 CMOS ADDER

Conventional CMOS adder design consist 58 transistors. This adder circuit built by equal number of NMOS and PMOS transistor [1]. Fundamental representation of conventional CMOS adder is with the help of 2 XOR, 2AND and 1OR gates, where

SUM = A XOR B XOR C (1)

CARRY = AB+ BC +CA (2)

The circuit diagram of 58T adder circuit implemented on cadence virtuoso design editor is shown in Fig.(b).

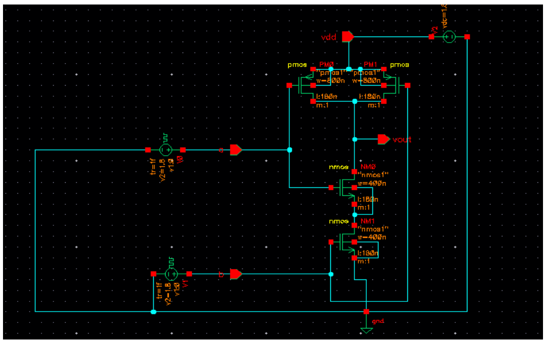


Fig.(a) Schematic View of NAND Circuit

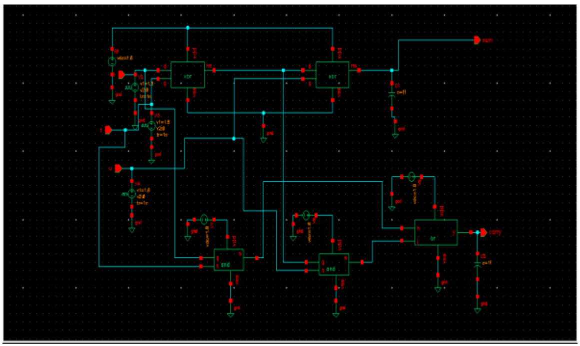


Fig.(b) Schematic View of 58T Adder Circuit

We can also build this adder by using only 9 minimum number of NAND gates as fundamental circuit which require total 36 transistors (36T) to implement it. This circuit consumes less power than the 58T adder circuit because it has less number of transistors [2]. The circuit diagram of 36T adder circuit implemented on cadence virtuoso design editor is shown in Fig.(c). We are using shannon's expansion theorem to reduce the number of transistors in the full adder circuit so we implement a 28T full adder circuit, hence power will reduce due to the reduction of transistors and then we apply transistor sizing and MTCMOS technique on it for more power reduction [11].

Reduction of sum and carry using shannon's expansion theorem

$$\text{sum} = ab'c' + a'bc' + a'b'c + abc \quad (3)$$

using shanon expansion theorem for sum

$$\text{sum} = a'(bc' + b'c) + a(b'c' + bc) \quad (4)$$

$$F_1 = b'c + bc' \quad (5)$$

$$F_2 = c'b' + cb \quad (6)$$

$$\text{carry} = a(b + c) + bc \quad (7)$$

using shanon's expansion theorm for carry

$$\text{carry} = a(b + c) + bc(a + a')$$

$$= a'bc + a(b + c) \quad (8)$$

$$F_3 = bc$$

$$= c'(0) + bc \quad (9)$$

$$F_4 = b + c$$

$$= b'c + b(1) \quad (10)$$

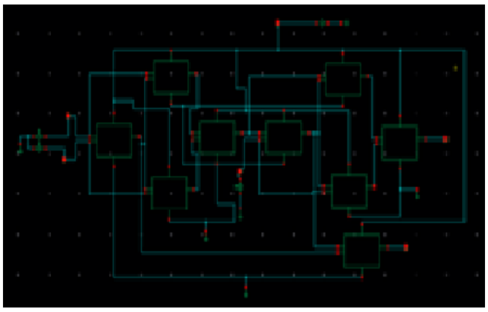


Fig.(c) Schematic View of 36T Adder Circuit

By using these reduce function we implement adder with the help multiplexer and for this we require 28 transistors (28T). [6]The block diagram of 28T adder circuit is shown in Fig.(d). The circuit diagram of 28T adder circuit implemented on cadence virtuoso design editor is shown in Fig.(e).

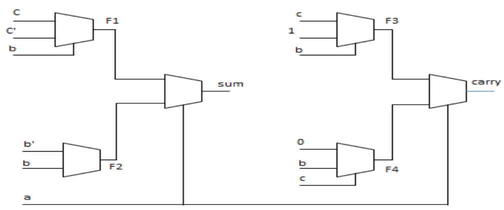


Fig.(d).28T adder circuit using shannon's expansion

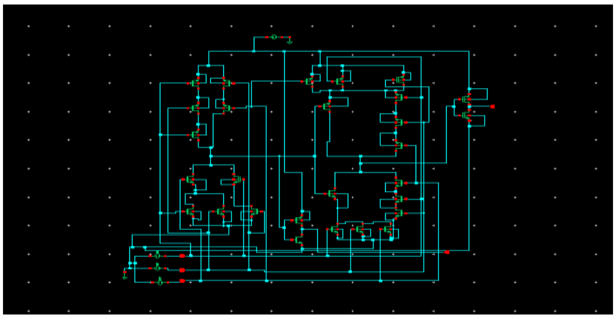


Fig.(e) Schematic View of 28T Adder Circuit

III. Transistor Sizing

Transistor sizing is basically we size the transistor according to our requirement and due to this area of the transistor is reduced. But reducing the area, increase the delay in the circuit. It is often possible to decrease the delay by increasing the sizes of transistors in the circuit. This area-delay tradeoff is known as the sizing problem[13].Sizing is mainly done by reducing the width of the transistor[16]. Here we work on the 180nm technology and first we take $W_P = 4um$, $W_n = 2um$ for the NAND circuit, after that we take $W_P = 800nm$, $W_n = 400nm$ to size the transistor. Similar dimension is taken for the 58T adder circuit, 36T adder circuit, 28T adder circuit and then analyze the power reduction.

IV. Mtcmos

In MTCMOS technology both high and low threshold voltage MOSFET used in a single chip for power reduction in a circuit and to deal with leakage problem. Dynamic power is directly proportional supply voltage ,to reduce this dynamic power supply voltage is reducing but alone reduction in supply voltage causes serious degradation to the circuit's performance. To maintain this both Supply and the threshold voltage are scale down. In MTCMOS low threshold voltage V_T (LVT) MOSFET is require to increase the speed of the device and high V_T (HVT) MOSFET require to reduce leakage current in the device. MTCMOS have a trade off with area because extra transistor is required in MTCMOS for high threshold voltage and low threshold voltage. These transistors normally known as sleep transistor. MTCMOS technique is more efficient then the VTCMOS technique[14],[18]. MTCMOS technique also increases the delay in the circuit. This technique has its own advantages and disadvantages.[7],[8] The basic circuit diagram of MTCMOS circuit is shown in Fig.(f). The circuit diagram of MTCMOS circuit implemented on cadence virtuoso design editor is shown in Fig.(g).

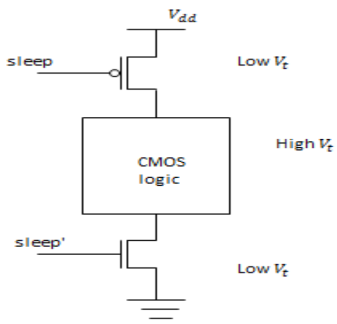


Fig.(f) MTCMOS circuit

For the MTCMOS implementation on cadence virtuoso design editor with 180nm technology we take low V_T =800n M for the CMOS logic and high V_T = 2u M for the PMOS and NMOS sleep transistors and then analyze the power.

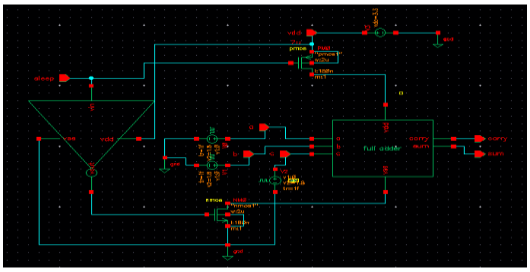


Fig.(g) Schematic View of MTCMOS Circuit

V. Result And Analysis

Here we first take the circuit and perform transistor sizing and MTCMOS technique separately as mention above and then we analyze power when we combined both the techniques. First we consider the NAND circuit and calculate the average power for switching with the help of all inputs condition and analyze the power in normal condition, transistor sizing, MTCMOS, and combined MTCMOS & transistor sizing. The results of analysis is shown in the table below:-

I/P	4T	TRANSISTOR SIZING	MTCMOS	COMBINED TECHINQUE
00	29.46 nW	18.81nW	37.15 pW	73.76 pW
01	27.8 pW	87.86pW	54.63 pW	115.17 pW
10	21.58 nW	7.69pW	17.29 nW	5.08 nW
11	13.27 pW	12.32pW	40.6 pW	40.60 pW
Avg. Pwr	12.77 nW	4.57 nW	4.35 nW	1.33 nW

Table 1 Analyzed data for NAND

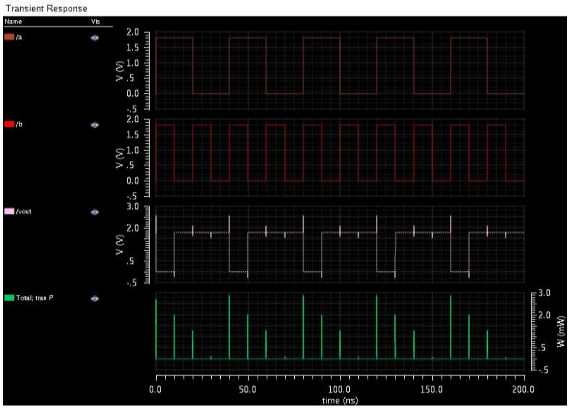


Fig.(h)NAND waveform without transistor sizing

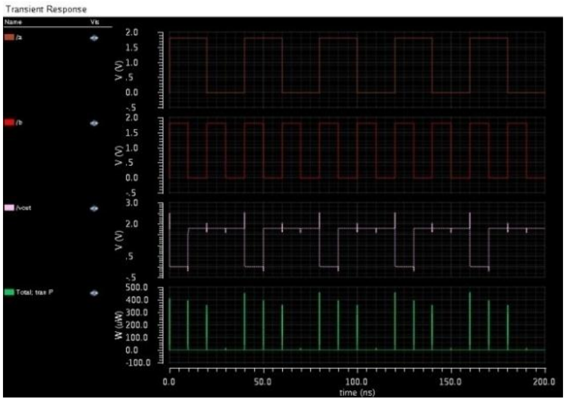


Fig.(i) NAND waveform with transistor sizing

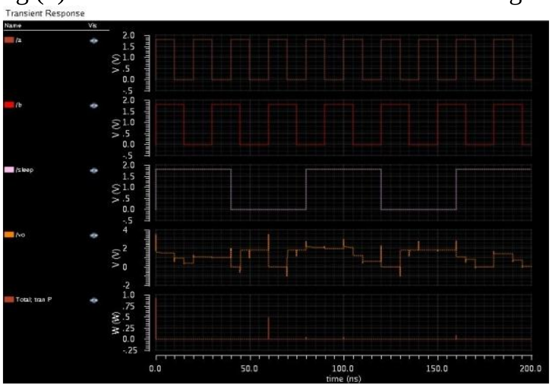


Fig.(j) NAND waveform with MTCMOS Technique

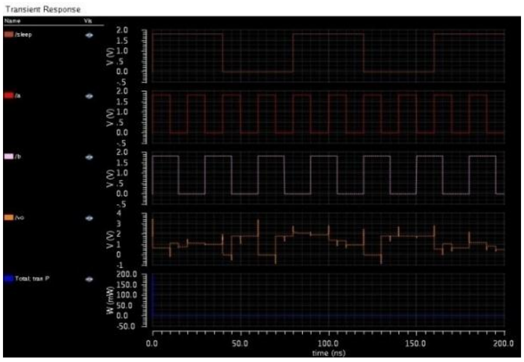
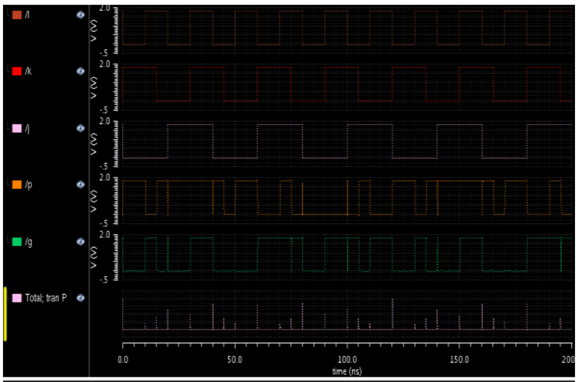


Fig.(k) NAND waveform with combined Technique

Now same procedure is applied for the 58T ,36 T, 28T adder circuit and analyze the power in different input condition and calculate the average power [5]. The results of analysis is shown in the tables.

I/P	58-T	TRANSISTOR SIZING	MTCMOS	COMBINED TECHNIQUE
000	83.62 nW	28.5 nW	19.79 nW	5.9 nW
001	20.9 nW	5.4 nW	16.86 nW	5.23 nW
010	37.33 nW	12.9 nW	15.92 nW	9.53 nW
011	10 nW	2.84 nW	10.37 nW	2.66 nW
100	113.9 nW	44 nW	24.57 nW	6.88 nW
101	92.37 nW	6.32 nW	20.61 nW	5.65 nW
110	37.03 nW	21.8 nW	32.48 nW	8.59 nW
111	31.67 nW	8.12 nW	30.05 nW	7.96 nW
Avg. Power	53.35nW	16.23 nW	21.33 nW	6.55 nW

Table 2 Analyzed data for 58-T ADDER



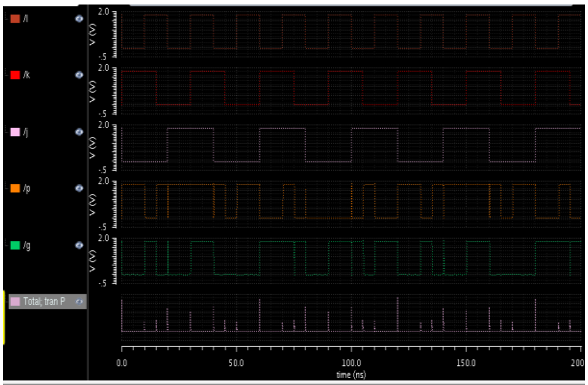
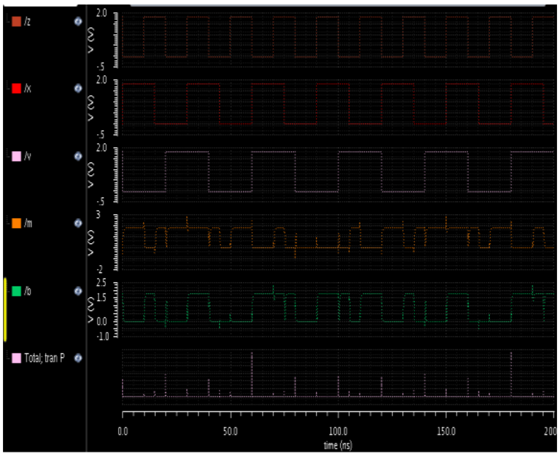


Fig.(l) 58-T adder waveform without transistor sizing

Fig.(m)58-T adder waveform using transistor sizing



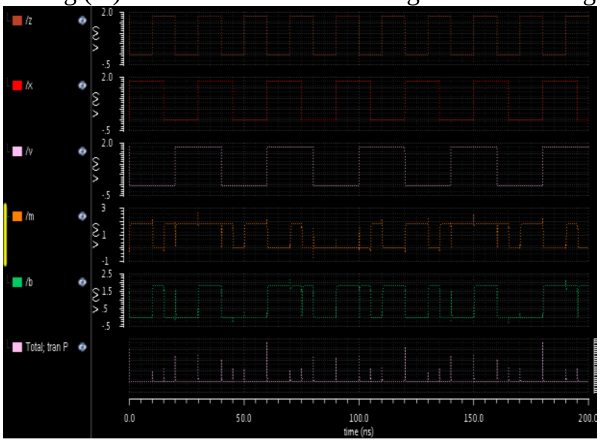


Fig.(o) 58-T adder waveform using combined

Fig.(n) 58-T adder waveform using MTCMOS

Table 3

I/P	36-T	TRANSISTOR SIZING	MTCMOS	COMBINED TECHNIQUE
000	116.37 nW	49.9nW	1.18mW	62.23 nW
001	2.27 mW	3.21mW	1.18mW	400.3 uW
010	2.27 mW	481uW	1.18mW	1.18 uW
011	4.58 mW	970uW	1.18mW	686.8 uW
100	2.29 mW	483uW	1.18mW	400.39 uW
101	4.59 mW	972uW	1.84mW	686.7 uW
110	7.36 mW	1.67mW	1.53mW	977.54 uW
111	9.65 mW	2.14mW	1.18mW	1.05 mW
Avg. Pwr	4.126 mW	1.24 mW	1.27 mW	672.72 uW

Analyzed data for 36-T ADDER

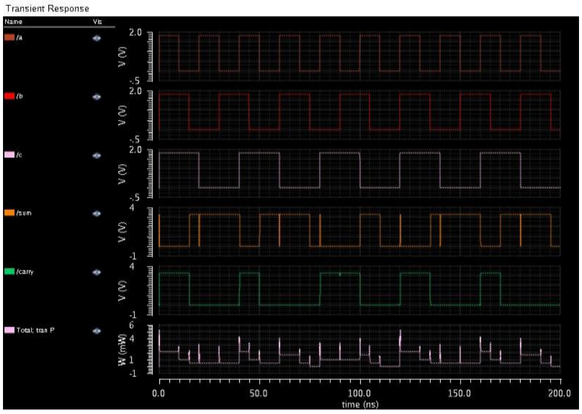


Fig.(p) 36T adder waveform with Transistor sizing

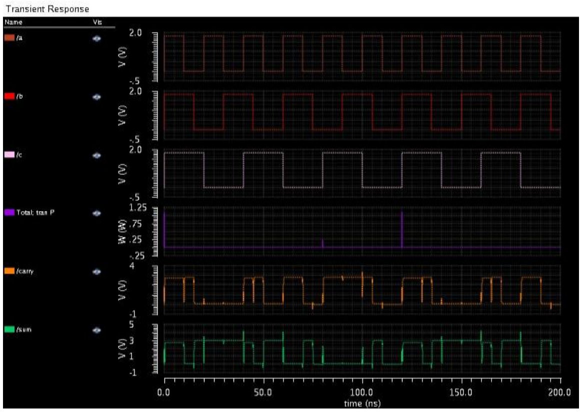


Fig.(q) 36T adder waveform with MTCMOS

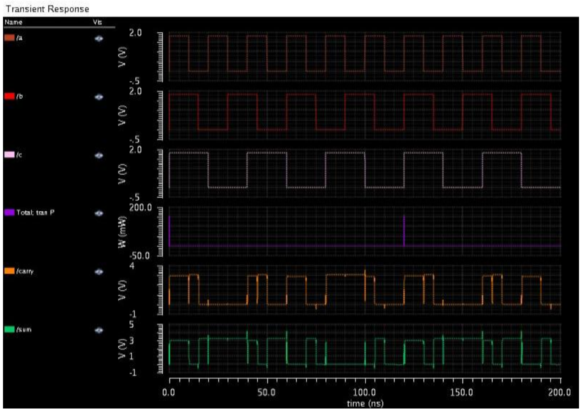


Fig.(r) 36T adder waveform with Combined Tech.

Input	28T	Transistor Sizing	MT-CMOS	Combined
0 0 0	360.442 nW	22.133 nW	349.39 uW	2.6397 nW
0 0 1	1.0601 mW	229.37 uW	282.58 nW	6.7096 nW
0 1 0	1.28253 mW	277.79 uW	10.029 nW	37.879 pW
0 1 1	3.78725 mW	783.64 uW	89.654 nW	352.41 pW
1 0 0	1.71603 mW	368.27 uW	5.3108 nW	453.91 pW
1 0 1	1.91816 mW	661.5 uW	475.3 nW	121.98 pW
1 1 0	7.839 mW	1.15 mW	14.314 nW	15.033 nW
1 1 1	1.9142 mW	955.5 uW	184.31 nW	10.44 nW
Avg.	2.4397 mW	564.6365 uW	31.73645 nW	4.473 nW

Table 4 Analyzed data for 28-T ADDER

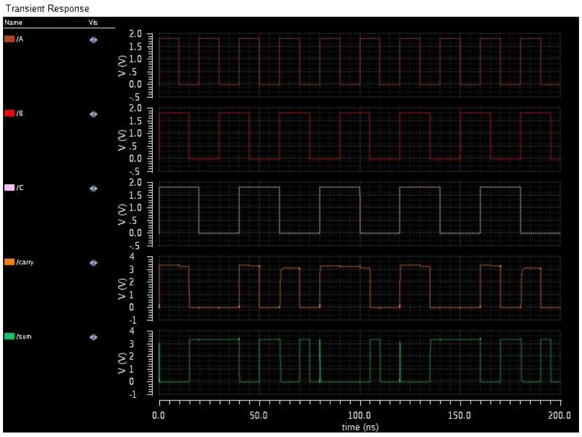


Fig.(s) 28T adder waveform without Transistor sizing

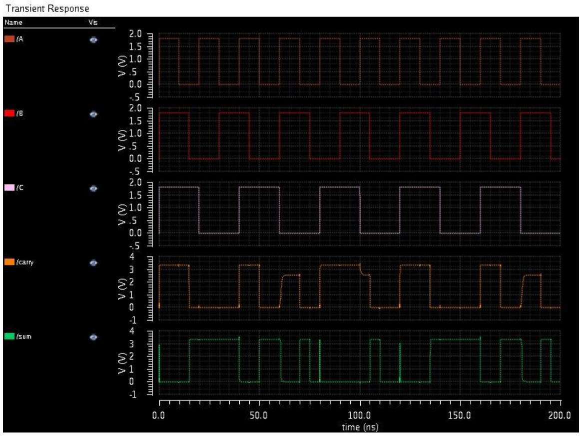


Fig.(t) 28T adder waveform with Transistor sizing

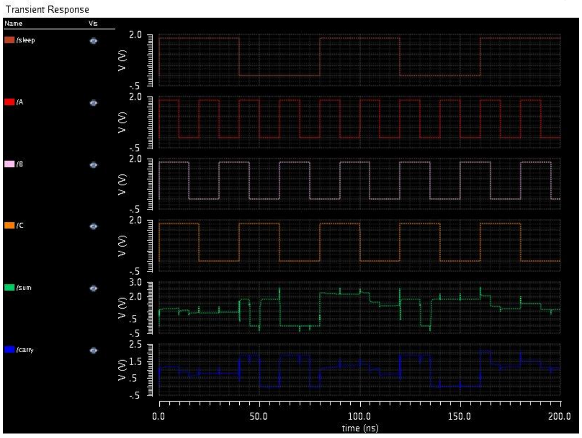


Fig.(u) 28T adder waveform with MTCMOS

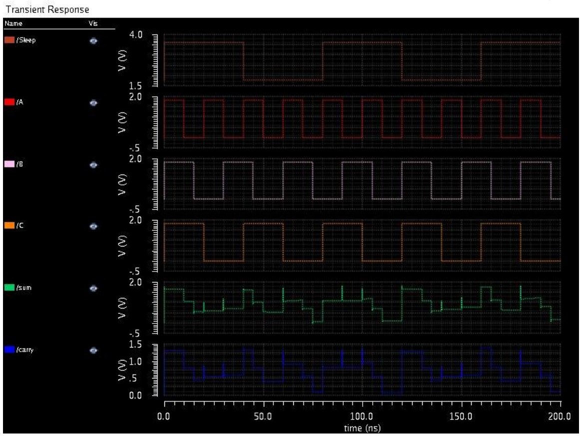


Fig.(v) 28T adder waveform with combined tech.

We analyze the waveform and calculate power at different input combination and compare power when transistor sizing and MTCMOS Technique are applied and when both are simultaneously applied. We also analyze that when we take power supply 3.3 V instead of 1.8V power consumption increases because dynamic power is directly proportional to the square of supply voltage. For experimental results of it we take basic transmission gate circuitry and analyze the power at 3.3V & 1.8V respectively. The circuit diagram of transmission gate circuit implemented on cadence virtuoso design editor is shown in Fig.(w).

Voltage	3.3V	1.8V
Avg. Power	241.5uW	199.85pW

Table 5 Analyzed data for effect of voltage scaling

For this we are take same size of transistors for the comparative study between the two voltages to see the effect of it on power.

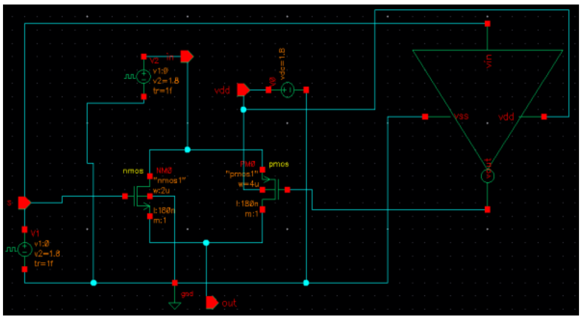


Fig.(w) Schematic of transmission gate

VI. Conclusion

In this paper we mainly focused on how much reduction of power takes place in different circuits design when we using transistor sizing and MTCMOS technique separately, as well as also yielding the result when we combine both the techniques.

In NAND circuit we attain 12.77nW power initially. Firstly when we use only Transistor Sizing technique we obtain 4.57nW power i.e. 64.21 % power reduction and then in another case we apply only MTCMOS technique in this we attain 4.35nW power i.e. 65.93% power reduction and lastly when we combine both the techniques and apply on this circuit we obtain 1.33nW power i.e. overall power reduction is 89.58%.

In 58-Transistor Full Adder we attain 53.35nW power initially. Firstly when we use only Transistor Sizing technique in this adder in which we obtain 16.23nW power i.e. 69.57% power reduction and then in another case we apply only MTCMOS technique in this adder we attain 21.33nW power i.e. 60% power reduction and lastly when we combine both the techniques and apply on this adder circuit we obtain 6.55nW power i.e. overall power reduction is 87.72%.

In 36-Transistor Full Adder we attain 4.126mW power initially. Firstly when we use only Transistor Sizing technique in this adder in which we obtain 1.24mW power i.e. 69.94% power reduction and then in another case we apply only MTCMOS technique in this adder we attain 1.27mW power i.e. 69.22% power reduction and lastly when we combine both the techniques and apply on this adder circuit we obtain 0.673mW power i.e. overall power reduction is 83.69%.

In 28-Transistor Full Adder we attain 2.439 mW power initially. Firstly when we use only Transistor Sizing technique in this adder in which we obtain 564.63uW power i.e. 76.85% power reduction and then in another case we apply only MTCMOS technique in this adder we attain 31.74nW power i.e. 92.22% power reduction and lastly when we combine both the techniques and apply on this adder circuit we obtain 4.47nW power i.e. overall power reduction is 98%.

We analyze that how much power reduction takes place. We also observe that as the number of transistor increases total average power increases, so no. of transistors in a digital design have a significant role due to the power and area of the design. The advantage of this due to power reduction we are able to reduce battery size and also able to increase life of the battery. Although there are some limitations such as use of these techniques becomes the circuit complex, Transistor sizing reduce the area & power but increases delay, and we are not considering here the other effects on area and delay if we consider this then less power reduction takes place in comparison to this. So for future enhancement in this we use buffer insertion, GDI and different algorithm like TILOS to maintain the performance in digital CMOS circuit. The application of this, we take fundamental circuit which are used in many circuits for examples like adders are widely used for the DSP application. All the results are verified by the Spectre simulator of Cadence Design System.

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