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Gate Diffusion Input: A technique for fast digital circuits (implemented on 180 nm technology)

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Abstract: *VLSI technology has developed over the years thereby enhancing the performance of chips in terms of three basic constraints viz. delay, power and area. Gate Diffusion Input technique is one such method which attempts to minimize the delay and power consumed by the circuit. The paper basically focuses on the implementation of the technique on combinational logic circuits and experimental delay results have been produced and these results have been compared with the conventional CMOS logic showing a reduction in delay and power-delay product using GDI. The graphical plots of digital circuits showing their transient behavior have also been presented. A comparative study between GDI and CMOS techniques shows GDI as the better one in terms of performance. However, GDI suffers from a few problems too, the most profound one being the problem in achieving full swing.*

Keywords: *delay, delay optimization, GDI, PTL, shannon expansion*

I. Introduction

The performance of a digital circuit is judged by its speed in producing output when an input is given to it. The most common technology for designing digital circuits is the CMOS technology. After the development of CMOS logic, there was increasing need to optimize circuit in terms of speed. One technique thought of was by using Pass Transistor Technology (PTL) which makes use of lesser number of gates to realize an operation. The Transmission Gate (TG) is one of them which is typically a combination of NMOS and PMOS transistors connected in parallel. The GDI cell represents another form of pass transistor technology which looks similar to CMOS but differs in the supply provided to the input terminals.

The main advantages of PTL over conventional CMOS design are as follows-

1) Lesser number of transistors results in low power dissipation and lesser delay.
2) Lesser number of transistors so smaller area and lesser interconnect effects.

However, PTL technologies also suffers from two main problems such as reduced circuit speed at low power operations and greater static power dissipation.

The paper presents a design technique that is the GDI technique that can be used to design fast, low power circuits using only a few transistors.

II. Gate Diffusion Input

The GDI cell is similar to a CMOS inverter structure. In a CMOS inverter the source of the PMOS is connected to VDD and the source of NMOS is grounded. But in a GDI cell this might not necessarily occur. There are some important differences between the two. The three inputs in GDI are namely-

1) G- common inputs to the gate of NMOS and PMOS
2) N- input to the source/drain of NMOS
3) P- input to the source/drain of PMOS

Bulks of both NMOS and PMOS are connected to N or P (respectively), that is it can be arbitrarily biased unlike in CMOS inverter. Moreover, the most important difference between CMOS and GDI is that in GDI N, P and G terminals could be given a supply 'V_{DD}' or can be grounded or can be supplied with input signal depending upon the circuit to be designed and hence effectively minimizing the number of transistors used in case of most logic circuits (eg. AND, OR, XOR, MUX, etc). As the allotment of supply and ground to PMOS and NMOS is not fixed in case of GDI, therefore, problem of low voltage swing arises in case of GDI which is a drawback and hence finds difficulty in case of implementation of analog circuits.

III. Operational analysis

The most common problem with PTL technique is its low voltage swing. An extra buffer circuitry may be used additionally to eliminate the problem of low swing and improve drivability. The problem of low swing can be understood with the help of a random function shown in figure 1 and table I.

Table I: Functionality Of any Random Function using GDI

A	B	Functionality	Logic
0	0	pMOS Trans Gate	V_{TP}
0	1	CMOS Inverter	1
1	0	nMOS Trans Gate	0
1	1	CMOS Inverter	0

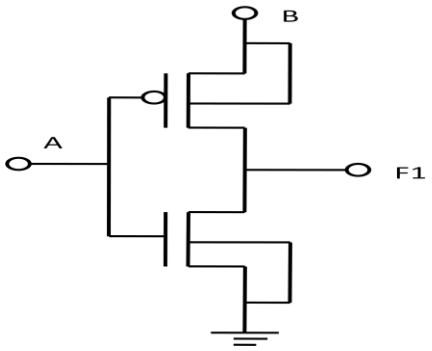


Fig 1: Schematic of any random fuction

The problem of low swing occurs only when A=0 and B=0 where the voltage level is V_{TP} instead of 0.This occurs due to the poor high to low transition characteristics of PMOS. In the rest of the cases it provides full swing.

IV. GDI Cell Using Shannon Expansion

The concept of Shannon theorem could be applied with ease to design a basic GDI cell. In Shannon expansion theorem, any function F can be written as:

$$F(x_1 \ldots x_n) = x_1 H(x_2 \ldots . x_n) + (\text{not } x_1) G(x_2 \ldots x_n) = x_1 F(1, x_2 \ldots x_n) + (\text{not} x_1) F(0, x_2 \ldots . x_n) \quad (1)$$

That is a larger function can be broken down into smaller function as shown above in equation (1). Then, the smaller functions could be further broken down if possible till the time it is not further reducible.

The output function of a basic GDI cell (where A, B, and C are inputs to G, P, and N, respectively) is given by:

$$\text{Out} = AC + (\text{not} A)\, B \quad (2)$$

Therefore, comparing equations (1) and (2) it is seen that a standard GDI cell can be used to implement any logic function based on Shannon expansion theorem as shown below taking an example.

If $A = x_1$, $C = F(1, x_1 \ldots . x_n)$, $B = F(0, x_1 \ldots .. x_n)$ then

$$\text{Out} = F(x_1 \ldots x_n) = x_1 F(1, x_2 \ldots x_n) + (\text{ not } x_1)\, F(0, x_2 \ldots x_n) \quad (3)$$

V. Implementing GDI

Table II shows the comparative study between GDI and CMOS for different logic gates showing their schematics. Table III shows the transient responses of different logic gates using GDI. Table IV represents the delay and power-delay product results of logic circuits using GDI and CMOS showing GDI as the one with lesser delay or power-delay product.

TABLE II: Comparative Study of GDI and CMOS Schematics

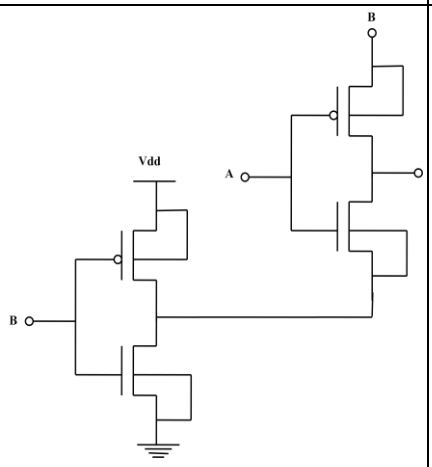
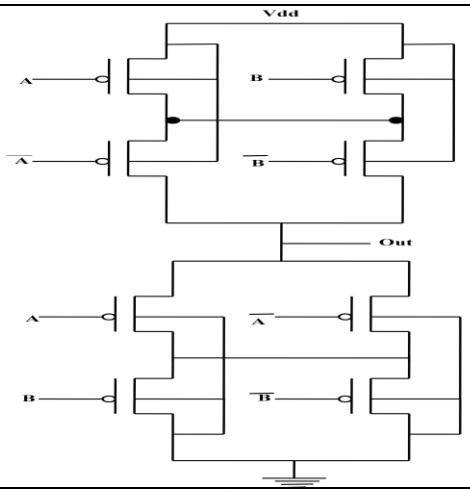
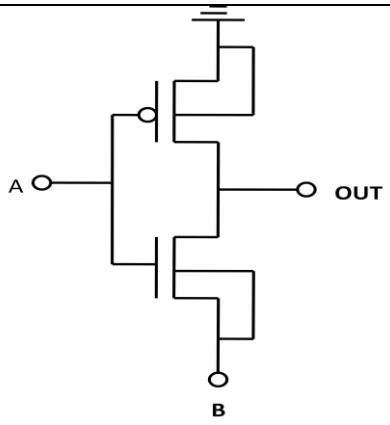
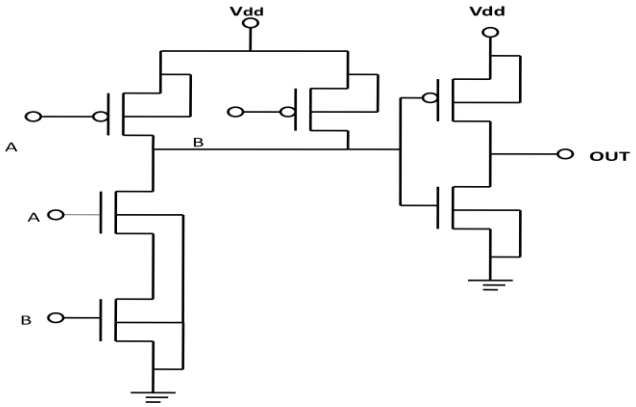
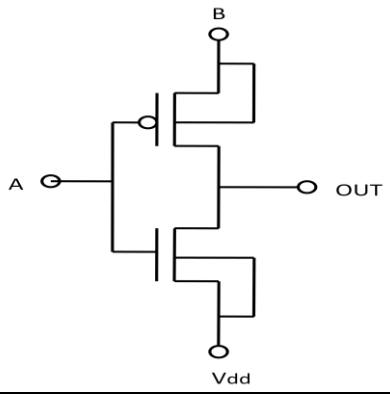
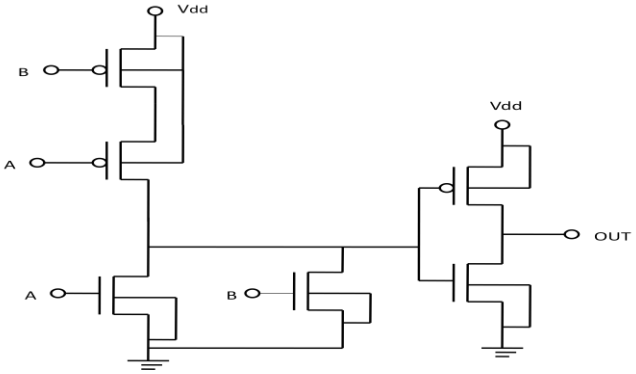
Logic Gate	GDI	CMOS
XOR		
	Transistor count- 4	Transistor count- 8 +4(for generating A' & B')
AND		
	Transistor count- 2	Transistor count-6
OR		
	Transistor count- 2	Transistor count- 6

Table III: Transient response using GDI

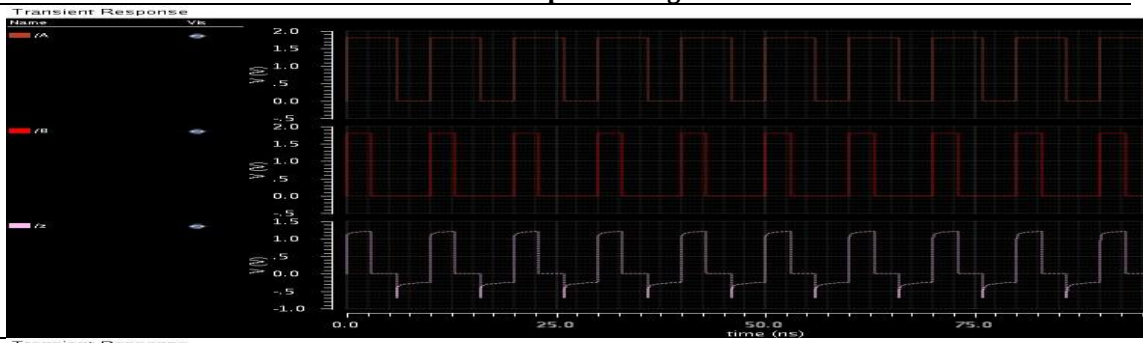
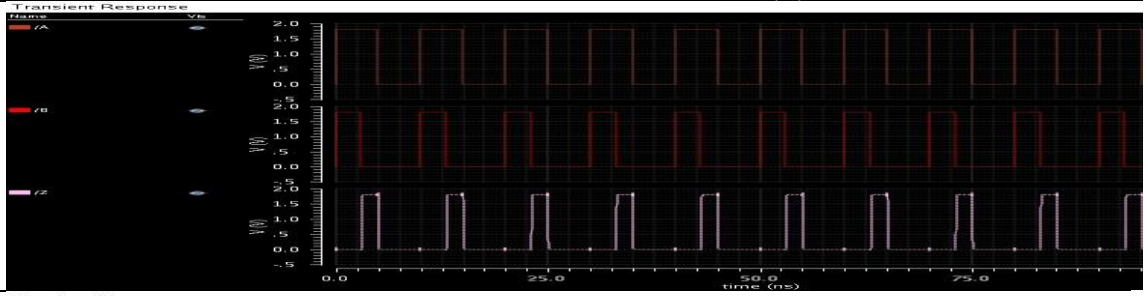
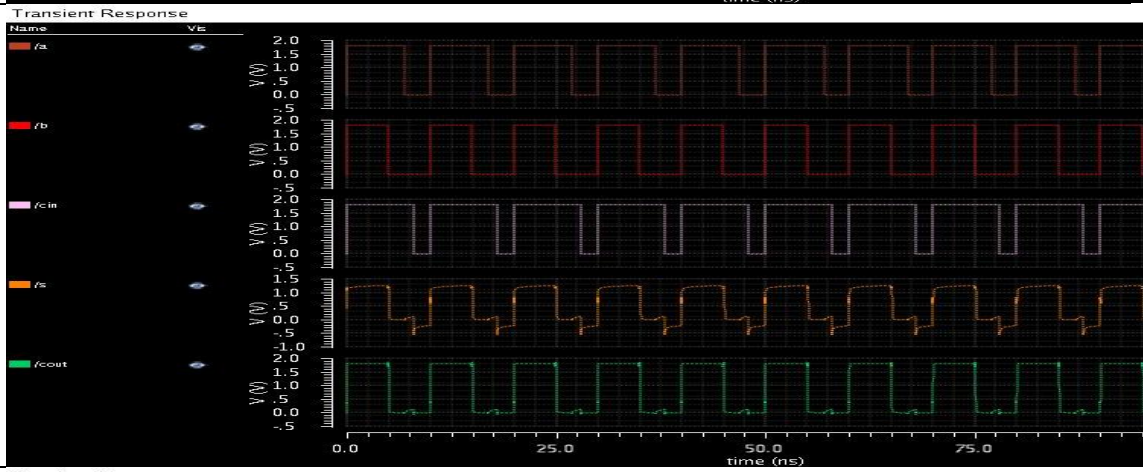
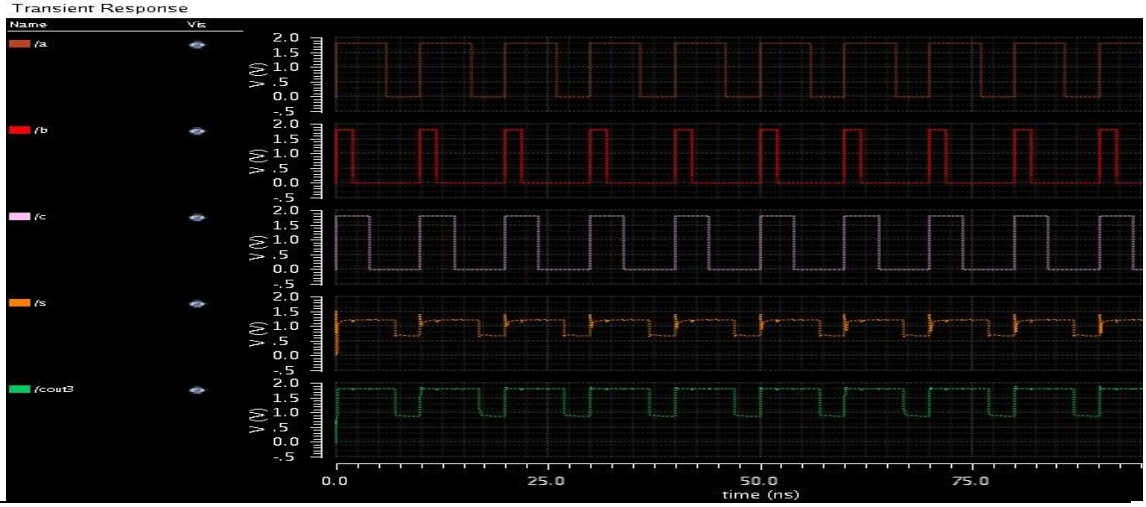
AND	
XOR	
1 bit full adder	
5:2 compr-essor	

TABLE IV: Delay results and power delay products (a comparison between GDI and CMOS)

Logic function	Delay GDI (ps)	Delay CMOS (ps)
AND	3.43	7.81
OR	4.22	9.02
1 BIT FULL ADDER	40.04	130.6

Logic function	Power delay product GDI (Ws)	Power delay product CMOS (Ws)
1 bit full adder	$198.59x10^{-15}$	$2292.03x10^{-15}$
4 bit full adder	$6342.53x10^{-15}$	$18232.22x10^{-15}$
5:2 compressor	$2519.58x10^{-15}$	$5068.65x10^{-15}$

VI. Conclusion

The GDI technique has been presented and it has been shown how it makes use of lesser number of gates to design a circuit which is desirable for fast and low power applications. The comparison between GDI and CMOS techniques has also been depicted and experimental delay and power-delay product values of both have also been produced. This technique can be successfully applied to larger digital circuits like comparators, multipliers, adders, etc. GDI together using Shannon expansion can be implemented with ease.

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