

## Reduction of Dynamic Power in Hazards for low voltage CMOS Architectures

P.Sai Raghava Reddy, Arra Ashok, J. Ravibabu,  
 M.TECH, Department of ECE, Sreenidhi Institute of Science and Technology  
 M.TECH, Department of ECE, Sreenidhi Institute of Science and Technology,  
 M.TECH, Department of ECE, Sreenidhi Institute of Science and Technology,

**Abstract:** Today, there is a large demand for portable electronics for computing and communication. In order to satisfy these requirements, we are focusing on low voltage design techniques. If we reduce the Supply voltage, we also have to reduce the Threshold voltage to maintain the performance. If we reduce the Threshold voltage to lower values, the leakage current cannot be neglected. The leakage power is dependent on the input vector control. This leakage power will get dissipated even when the gates are in ideal condition. We propose a Novel technique. This technique uses a integer linear programming(ILP) model. By using ILP model we are minimizing the leakage power in a dual-threshold static cmos circuit. We also reducing the glitch power by using the smallest number of delay elements. Experimental results show about 96% reduction of leakage power in the 70nm BPTM CMOS technology.

### I. Introduction:

Minimization of power is one of the most important power metrics in the design of portable systems. Two components determine the power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

Sources of power dissipation in CMOS devices are summarized by the following expression:

$$P = \frac{1}{2} \cdot C \cdot V_{dd}^2 \cdot f \cdot N + Q_{sc} \cdot V_{dd} \cdot f \cdot N + I_{leak} \cdot V_{dd}$$

Where P denotes the total power,  $V_{dd}$  is the supply voltage, and f is the frequency of operation.

In [1] nanoscaled CMOS devices, there are many leakage sources such as gate leakage, subthreshold leakage, BTBT based leakage, GIDL, DIBL, etc., the total leakage current in the off state n-MOSFET is given by

$$I_{leakage} = I_{SUB} + I_{BTBT} + I_{GIDL} + I_{GB} + I_{DG}$$

The different types of leakage currents can be explained as:

**Gate Induced Drain Leakage (IGIDL):** IGIDL is a current from the drain to the substrate caused by the high electric field between the gate and the drain; thin gate-oxide thickness and a high supply voltage increase GIDL.

**Band to Band Tunneling Leakage (IBTBT):** In a high electric field (greater than  $10^6$  volts per centimeter), electrons tunnel across the reverse-biased PN junction of drain and source substrates, in what is known as junction BTBT. IBTBT increases exponentially due to increased size of lightly doped drain region.

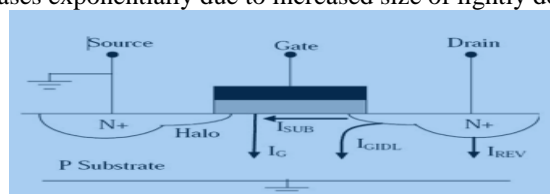


Fig1: Leakage current components in an NMOS transistor

**Gate Oxide Tunnelling Current (IG):** Reduction of gate oxide thickness[3] results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunnelling of electrons from substrate to gate and also from gate to substrate through the gate oxide, resulting in the gate oxide tunnelling current.

**Subthreshold Leakage (ISUB):** sub threshold or weak inversion conduction current between source and drain in an MOS transistor occurs when gate voltage is below  $V_{th}$ . Subthreshold Leakage is exponentially related to  $V_{th}$ .

Another factor which contributes to the power consumption in CMOS combinational logic circuits is the switching activities in the circuits. Many of such switching activities are due to spurious pulses, called glitches. A glitch is a fast spike which is unwanted. A hazard is a circuit which may produce a glitch. The power consumed in CMOS combinational logic circuits is heavily dependent on the switching activities in a circuit. Such switching activities are largely determined by the input switching patterns and the structure of the circuit. For low power design, glitching should be minimized because it causes power dissipation.

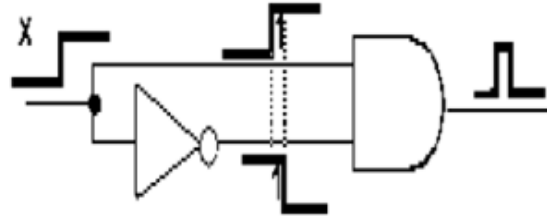


Fig2: Glitch

In static CMOS circuits, due to the imbalance of delays among the different combinational paths ending at the output of a gate, the output signal might switch more than one within a clock period before it stabilizes. These extra transitions are called glitches. Figure3 gives an example of glitch generation.

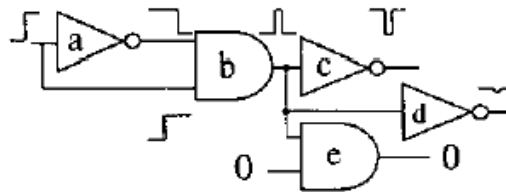


Fig3:generation, propagation & termination of a glitch

**II. Leakagecurrent Reduction Techniques:**

**A. STANDBY LEAKAGE CONTROL USING TRANSISTOR STACK:**

The stacking effect is best understood by considering a two-input NAND gate as shown in Fig. 4. When both M1 and M2 are turned off, the voltage at the intermediate node is positive due to small drain current. Positive potential at the intermediate node has three effects:

- 1) Due to positive source potential  $V_m$  gate-to-source voltage of M1( $V_{gs1}$ ) becomes negative; hence, the subthreshold current reduces substantially.
- 2) Due to  $V_m > 0$ , body-to-source potential( $V_{bs1}$ ) of M1 becomes negative, resulting in an increase in the threshold voltage (larger body effect) of M1, and thus reducing the subthreshold leakage.
- 3) Due to  $V_m > 0$  the drain to source potential ( $V_{ds1}$ ) decreases, resulting in an increase in the threshold voltage (less DIBL) of, and thus reducing the subthreshold leakage.

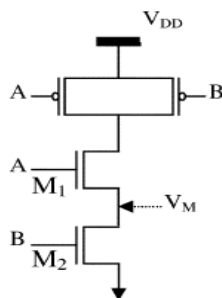


Fig4: Stacking effect in two input NAND gates

**B. Minimum leakage vector method:**

The leakage current of a logic gate is a strong function of its input values. The reason is that the input values affect the number of OFF transistors in the NMOS and PMOS networks of a logic gate.

Table 1 shows the leakage current of a two-input NAND gate built in a 0.18µm CMOS technology with a 0.2V threshold voltage and a 1.5V supply voltage. Input A is the one closer to the output of the gate.

Inputs		Output	Leakage current(nA)
A	B	O	
0	0	1	23.05

0	1	1	51.42
1	0	1	47.15
1	1	0	82.94

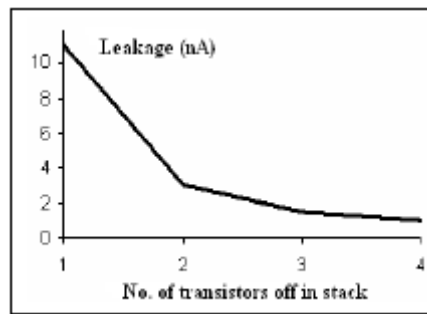
**Table1:** The leakage values of a NAND gate

The minimum leakage current of the gate corresponds to the case when both its inputs are zero. In this case, both NMOS transistors in the NMOS network are off, while both PMOS transistors are on. The effective resistance between the supply and the ground is the resistance of two OFF NMOS transistors in series. This is the maximum possible resistance. If one of the inputs is zero and the other is one, the effective resistance will be the same as the resistance of one OFF NMOS transistor. This is clearly smaller than the previous case. If both inputs are one, both NMOS transistors will be on. On the other hand, the PMOS transistors will be off. The effective resistance in this case is the resistance of two OFF PMOS transistors in parallel. Clearly, this resistance is smaller than the other cases.

In the NAND gate of Table 1 the maximum leakage is about three times higher than the minimum leakage. Note that there is a small difference between the leakage current of the A=0, B=1 vector and the A=1, B=0 vector due to the body effect. The phenomenon whereby the leakage current through a stack of two or more OFF transistors is significantly smaller than a single device leakage is called the “stack effect”.

**C. LECTOR TECHNIQUE:**

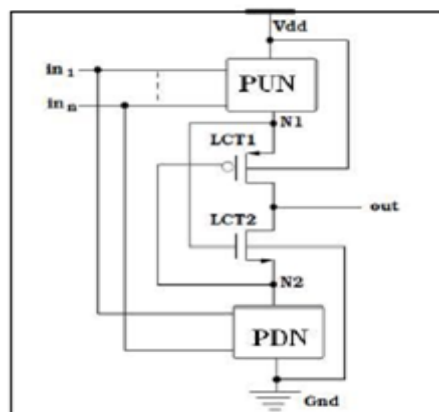
The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR[4] technique for the leakage power reduction. This is stated based on the observation that “a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path”. The number of OFF transistors is related to leakage power as shown in Figure 5.



**Fig5:** Transistor-stacking Vs Leakage power

In this technique[5], two leakage control transistors are introduced between pull-up and pull-down network within the logic gate (one PMOS for pull-up and one NMOS for pull-down) for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cutoff region.

The topology of a LECTOR CMOS gate is shown in Figure 6. Two LCTs are introduced between nodes N1 and N2. The gate terminal of each LCT is controlled by the source of the other, hence termed as self-controlled stacked transistors. As LCTs are self-controlled, no external circuit is needed; thereby the limitation with the sleep transistor technique has been overcome. The introduction of LCTs increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current.



**Fig6:** Lector cmos gate

Leakage Control Transistor (LECTOR) technique is illustrated in detail with the case of an inverter. A LECTOR INVERTER is shown in Figure7. A PMOS is introduced as LCT1 and a NMOS as LCT2 between N1 and N2 nodes of inverter. The output of inverter is taken from the connected drain nodes LCT1 and LCT2. The source nodes of LCT1 and LCT2 are the nodes N1 and N2 respectively of the pull-up and the pull-down logic. The gates of LCT1 and LCT2 are controlled by the potential at source terminal of LCT2 and LCT1 respectively. This connection always keeps one of the two LCTs in its near cutoff region for any input.

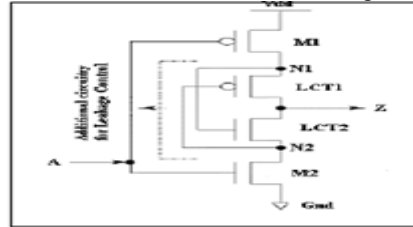


Fig7: LECTOR based cmos inverter

### III. Glitchingpower Reduction Technique:

The transmission gate will pass logic 0 and 1 respectively without effecting voltage level of the signal. The effective resistance  $R_{eff}$  of CMOS transmission gate is given by combined both transistors connected in parallel:

$$d_{1 \rightarrow 3} = R_{on} * C_{in1} + d3$$

$$d_{2 \rightarrow 3} = R_{on} * C_{in2} + d3$$

Where  $C_{in1}$  and  $C_{in2}$  are the input capacitances seen at the inputs of the gate and  $R_{on}$  is the series resistance of the ON transistors in the previous stage. The delay of the transmission gate due to  $R_{eff}$  along with  $R_{on}$  for charging  $C_{in1}$  is given by  $(R_{on} + R_{eff}) \times C_{in1}$ . The proposed physical implementation flow is shown in Fig 9.

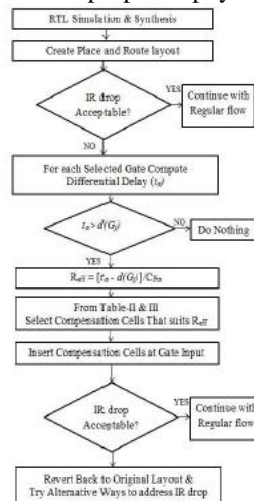


Fig9: Flow diagram for variable input delay method

#### b. An MILP for Leakage & glitch power minimization:

We use a mixed integer linear programming [7](MILP) model to determine the optimal assignment of  $V_{th}$  while maintaining any given performance requirement on the overall circuit delay. To minimize the total leakage the MILP assigns low  $V_{th}$  to the largest possible number of gates while controlling the critical path delays. Unlike the heuristic algorithms, the MILP gives us a globally optimal solution.

To eliminate the glitch power, additional MILP constraints determine the positions and values of the delay elements to be inserted to balance path delays within the inertial delay of the incident gates. We can easily make a tradeoff between power reduction and performance degradation by changing the constraint for the maximum path delay in the MILP model.

Variables:

Each gate is characterized by four variables:

$X_i$ : assignment of low or high  $V_{th}$  to gate  $i$  is specified by an integer  $X_i$  which can only be 0 or 1. A value 1 means that gate  $i$  is assigned low  $V_{th}$ , and 0 means that gate  $i$  is assigned high  $V_{th}$ . Each gate has two possible values of delays,  $DL_i$  and  $DH_i$ , corresponding to low and high thresholds, respectively.

$T_i$ : latest time at which the output of gate  $i$  can produce an event after the occurrence of an input event at primary inputs of the circuit.

$t_i$ : earliest time at which the output of gate  $i$  can produce an event after the occurrence of an input event at primary inputs of the circuit.

$\Delta d_{i,j}$ : delay of a possible delay element that may be inserted at the input of gate  $i$  from gate  $j$ . Thus, an  $n$  input gate is characterized by  $n+5$  quantities, i.e.,  $n$  input buffer delay variables, two inertial delay constants, one  $[0, 1]$  integer variable, and two output timing window variables.

The objective function for the MILP is minimization of the sum of all gate leakage currents and the sum of all inserted delays.

$$\text{Min}(\sum I_{\text{leaki}} + \sum \sum \Delta d_{i,j}) =$$

$$\text{Min}(\sum (X_i I_{li} + (1-X_i) I_{hi}) + \sum \sum \Delta d_{i,j})$$

#### **IV. Conclusion:**

We explained some techniques to reduce the leakage and dynamic glitch power & one algorithm to reduce the leakage and dynamic glitch power simultaneously.

#### **References:**

- [1]. "Leakage power estimation & minimization in VLSI Circuits" by Wen-Tsong Shine.
- [2]. "Four -Bit Cmos Full Adder Design in Submicron Technology with Low Leakage Power & Ground Bounce Noise Reduction using Dual Sleep Approach" by Y.Jagadeesh,T.Krishnamurthy.
- [3]. "Standby and Active Leakage Current Control & Minimizaion in CMOS VLSI Circuits" by Farzan Fallah,Massoud Pedram.
- [4]. "Studying Impact of Various Leakage Current Reduction Techniques on Different D-Flipflop Architectures" by UdaiyaKumar.R,Anbarasu.W.
- [5]. "Off-State Leakage Power Reduction by Automatic Monitoring & Control System" by S.Abdollahi Pour & M.Saneei.
- [6]. "Analysis of glitch power dissipation in CMOS ICs" by M.Favalli & L.Benini.
- [7]. "Leakage Current Mechanisms & Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits" by Kaushik Roy.