IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 4, Issue 2, Ver. IV (Mar-Apr. 2014), PP 05-12
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design of Testable Reversible Memory Circuits

Soumyajit Biswas[1], G.L.Kumar Moganti[2]
[1]*(School of Electronics Engineering, KIIT University)*
[2]*(School of Electronics Engineering, KIIT University)*
[1]*(email- soumyajit.5b@gmail.com)*
[2]*(email- ganesh.moganti@gmail.com)*

Abstract: *Quantum dot Cellular Automata (QCA) is the new possibility for the future of nano-electronic computing technology which employs the principle of quantum mechanics. This paper, contributes to the design of Memory circuits based on conservative reversible logic gates & also the design is made testable using two test vectors. The conservative logic gates dominates the classical gates in terms of testability, feature size scaling & high power consumption for the design of sequential circuits. Here the Memory circuits (1-bit, 4-bit & 8-bit) are designed by employing conservative logic gates(Fredkin Gate), which is being simulated and tested for the detection of unidirectional stuck-at faults using two test vectors 0s & 1s. For the simulation of the described designs Xilinx's 8.2 EDA tool is used.*

Keywords: *conservative reversible logic, Fredkin gate, QCA, stuck-at-faults, memory*

I. Introduction

Over the last few decades, the exponential scaling in feature size & increase in processing power in VLSI has cornered the CMOS technology. The challenges that are faced by CMOS are power consumption is very high, dominant factor in VLSI, also scaling of feature size is having difficulties, ultra thin gate-oxide, doping fluctuation, short channel effect are the other notable problems Thus to cope up with the growing technology needs, as an alternative to CMOS-VLSI technology, researchers have developed a new computing technology based on quantum principles, known as *Quantum Dot Cellular Automata*[QCA].

II. Background

Cellular automata (CA) are discrete dynamical systems whose evolution is based on local inter-actions. This devices operate via interaction of local forces such as Coulomb repulsion between the electrons rather than current carrying wires. The position of individual electrons determine the logical states of the device rather than voltages in case of CMOS. Each QCA cell is of square shape having four quantum dots located in 4 corners of the cell, each cell is charged with two extra electrons due to the Coulomb repulsion force, the electrons occupy diagonally opposite dots. There are two possible states logic "1" & "0" denoted as cell polarization P=+1 and P=-1, respectively. Dots are located close to each other so that electrons can tunnel between them easily. Clock densities & clock frequencies shows new possibilities in QCA domain, beyond existing CMOS technology i.e.(approximately around 10^4 Tera Hz)[4],[5].

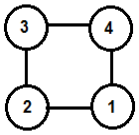


Fig-1[2]

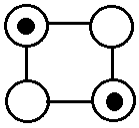


Fig-2[2]

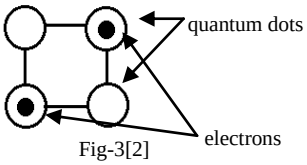


Fig-3[2]

The above Fig-1 depicts a basic QCA cell, having 4 quantum dots. Fig-2 depicts the logic '0' state, the black dots represent electrons of polarization=-1. Fig-3 depicts logic '1' state, of polarization=1.

2.1 Conservative Reversible Logic in QCA: QCA seems to be optimistic for the computational methods because it incorporates the technology of reversible logic gates[2], [3]. The prime computational method is based on conservative logic family that unveils same number of '1's in the outputs as well as in the inputs. Sometimes conservative logic is reversible and sometimes irreversible. Reversibility depicts a relation of one-to-one mapping of input and the output vectors. which means each output vector is unique for each input vector. So in contrast when reversible logic also holds the property of same number of '1's in outputs and inputs, it is called reversible conservative logic.

2.2 Benefits of reversibility: It is observed that irreversible computation produces KTln2 Joules of heat energy with the loss of each bit of information. Thus it is proved from the point of view of thermodynamics, if computation is carried out in a reversible manner that kTln2 amount of energy dissipation would not occur. Thus, adaptation of reversible logic provides a logic design methodology in ultralow power domain that is beyond KTln2 limit, is the prime motivation for the designing of emerging nanotechnologies where energy loss due to information destruction is a vital aspect for overall heat dissipation[1],[2]. In QCA computing, logic states are represented by the position of the electrons. Unlike conventional CMOS, when a bit is flipped from '1' to '0' the capacitor doesn't actually discharge in QCA cell. During transition QCA does not dissipates all its signal energy. Moreover, during signal propagation between cells, polarisation phenomenon accounts for the electron interaction in adjacent QCA cells. Since there is absolutely no electrons movement between QCA cells, there is no current flow. Results in no signal dissipation. Therefore, the significant advantage of QCA is low power dissipation as compared to CMOS technology.

III. Basic Design Elements

3.1 Fredkin gate: It was first proposed by Fredkin and Toffoli[7]. The most popularly used (3x3) reversible conservative logic gate, having the input-output mapping as (A, B, C) to (P=A, Q=A'B+AC, R=AB+A'C). Fig-2 shows two dotted rectangle in it each equivalent to a 2x2 Feynman gate and each dotted rectangle has a quantum cost of 1. Hence Fredkin gate involve 2 dotted rectangles, 1 Controlled-V gate and 2 CNOT gates resulting in its quantum cost to be 5[6].

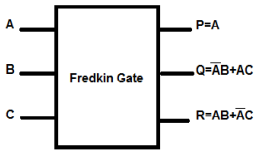


Fig-4[6]

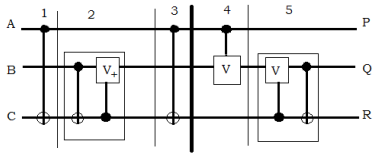


Fig-5[6]

Fig-4 shows the Fredkin gate and Fig-5 shows its quantum implementation with quantum cost equal to 5.

By implementing this reversible gate, any testable sequential circuits can be designed in low power & current nanometer scaling domain. Fredkin gate dominates the classical gates on the terms of Testing, also other parameters involved in optimization techniques are, number of reversible gates, garbage output, quantum cost, delay etc. This Fredkin gate makes the sequential circuit testable for two test vectors all 0's or all 1's. Any stuck-at-faults can be detected using this Fredkin gate in sequential circuit designs. The input & output relation of Fredkin gate are stated in the truth table below[4] [6].

Table-1

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

3.2 D-Flip-Flop: The main memory element of sequential circuits made up of conservative reversible logic gate. The characteristic equation of D-latch is given by

$$Q^{+}=D.E+E'.Q \text{ ----------(1)[6]}$$

Here the enable line (E) is used interchangeably in place of clock. When the enable signal (clock) is made high i.e. 1, the input value of D is displayed at the output as Q+ = D. While, when E becomes low, the latch maintains its previous state, i.e. Q+ = Q. Also the Fredkin gate has two of its outputs working same as that of a 2:1 MUX. The design comprises of two Fredkin gate & its operation is split into two modes- -

i. Normal Mode
ii. Test Mode

Normal Mode: Now the design consists of 4 inputs – 2 normal inputs D & E, 2 control lines C1 & C2. The operation is as follows the circuit will work as normal D-latch for C1=0 & C2=1.

Test Mode: In this mode for C1,C2 = '00', the design will be testable for all '0' input vectors, as outputs will become '0' .Thus any stuck-at-1 faults can be detected. Again for C1,C2 = '11', design becomes testable for all '1' input vectors, as outputs becomes '1'. Therefore any stuck-at-0 faults can be detected.

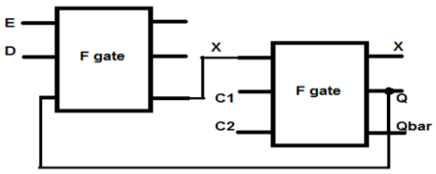


Fig-6
The above circuit Fig-6, shows the D Flip-Flop testable for two input vectors.

IV. Proposed Memory Design

Memory is an essential component of a microcomputer system, as it stores binary information and data for microprocessor and other applications. It is mainly classified into two - i) Read/Write memory (R/WM) & ii) Read-Only memory (ROM). The R/W memory is formed by registers, and each register stores bits of information by a group of Flip-Flops, which are called memory cell. On the other hand, information are permanently stored in the form of diodes for ROM. Where a group of diodes form the register. In a R/W memory, each Flip-Flop is capable of storing 1-bit at a time either '1' or '0', depending upon the control signals it performs write & read operations[8].

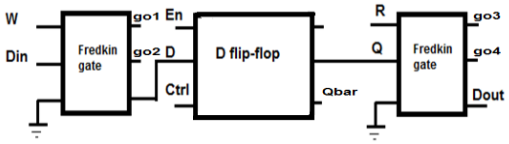


Fig-7
The above fig shows the 1-bit R/W Memory circuit comprising of a D flip-flop & two Fredkin gates as control circuits.

4.1 Working of 1-bit R/W memory: The flip-flop is the basic element of this design, since a 1-bit design so only 1 flip-flop is being employed. The control circuitry is being designed out of two Fredkin gates for writing & reading operation. The circuit has 5 input lines, the control circuit has W line for write operation, Din for input data & E , Ctrl for enabling & mode selection of D flip-flop, R line for read operation. Dout is the output data line and go1-4 are garbage outputs which doesn't contribute in the circuit operation[8].
Write operation: The input data is fed into control circuit-1 through the Din line, now with the application of an active high signal at W line the output (W.Din) is sent to the D line of D flip-flop. with the E line being held high the flip-flop is activated and store that bit info Din in it & also sent it to the output line Q of D flip-flop. After write operation is made the signal W is made low.
Read operation: With the application of active high signal at the R line the output Q of D flip-flop is fed in to control circuit-2 to the final output Dout. After read operation R is made low.

4.2 Design of 4-bit R/W memory: This design comprises of combination of four 1-bit R/W memory cell discussed above. It has the W, R , E & Ctrl line in common to all the four 1-bit memory blocks and performs the same operation as 1-bit R/W memory design. Other than this it has four data input line D3-0 & four output lines Dout3-0, also has 16 garbage outputs. The Read and Write operation are same as 1-bit design[8].

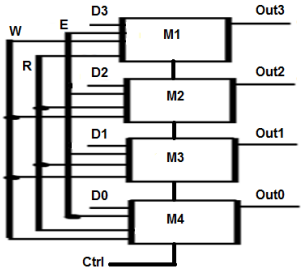


Fig-8
The above fig shows the 4-bit R/W Memory circuit comprising of four 1-bit R/W memory cells.

4.3 Design of 8-bit R/W memory: This design comprises of combination of two 4-bit R/W memory cell discussed above. It has the W, R , E & Ctrl line in common to all the two 4-bit memory blocks and performs the

same operation as 4-bit R/W memory design. Other than this it has four data input line D7-0 & four output lines Dout7-0, also has 32 garbage outputs. The Read and Write operation are same as 4-bit design[8].

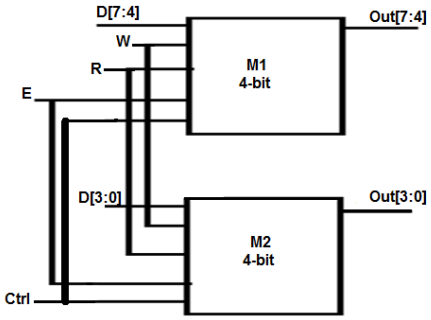


Fig-9

The above fig shows the 8-bit R/W Memory circuit comprising of two 4-bit R/W memory cells.

V. Result

This input output relation of Fredkin gate is simulated under Xilinx's 8.2 EDA tool[9], the obtained RTL schematic and the test bench wave form is given below

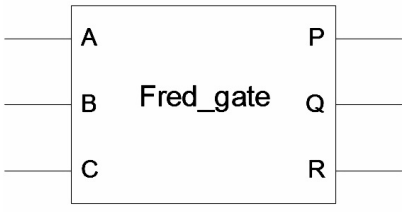


Fig-10

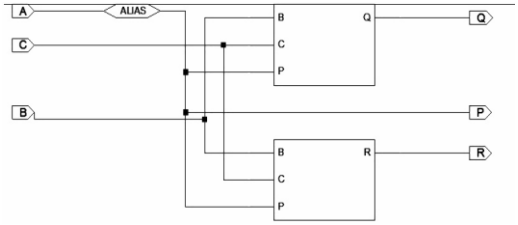


Fig-11

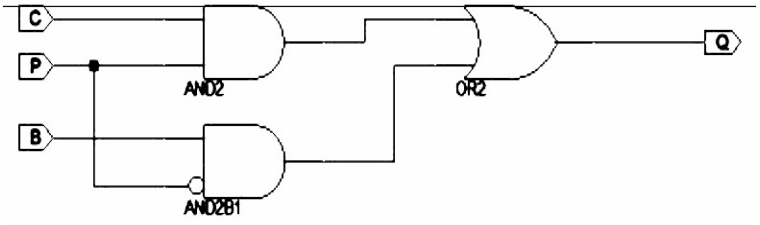


Fig-12

Fig-10 shows the basic building block of Fredkin gate, Fig-11 shows the inner blocks of main block RTL, Fig-12 shows the basic gate representation of the blocks shown in Fig-11

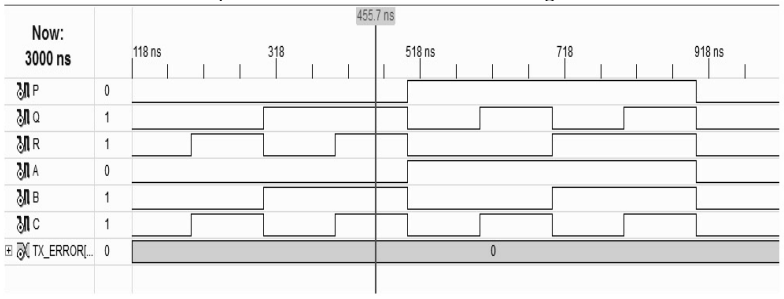


Fig-13

Fig-13 represents the test bench waveform of Fredkin gate.

The second most important element of the memory is the bit storage element i.e. the D flip-flop which is being designed by employing two Fredkin gates . The simulated results are shown below

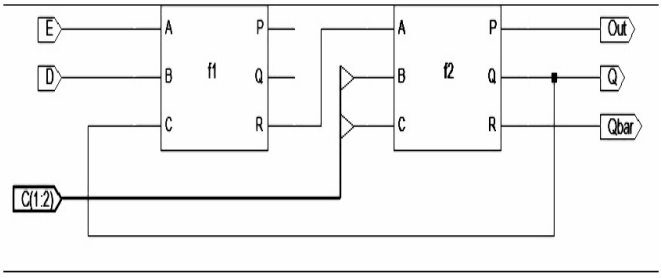


Fig-14
The above fig shows the RTL schematicof the D flip-flop.

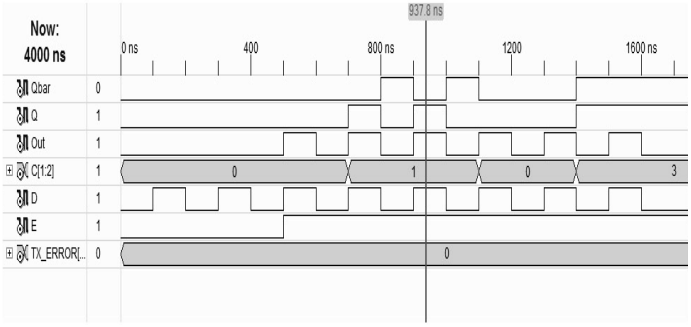


Fig-15
The above fig shows the test bench waveform of the D flip-flop operating in both normal & test mode.

The proposed 1-bit R/W Memory is being simulated and the RTL schematic & output wave form is given below.

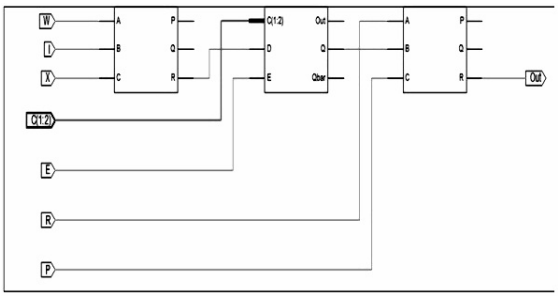


Fig-16
The above Fig shows the RTL schematic of 1-bit R/W memory

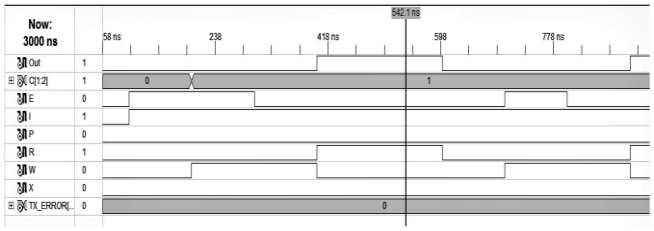


Fig-17

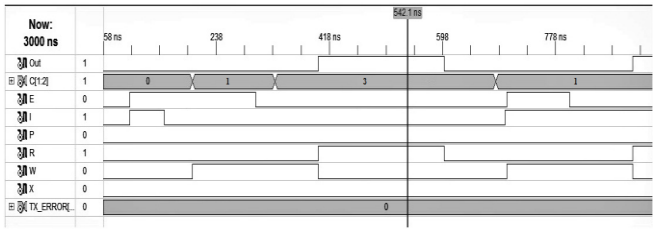


Fig-18
The above Fig-17 shows the test bench waveform in normal mode of operation of 1-bit R/W memory design & Fig-18 shows thetest bench waveform in the test mode of operation.

The proposed 4-bit R/W Memory is being simulated and the RTL schematic is shown in Fig-19 & output wave form is given below.

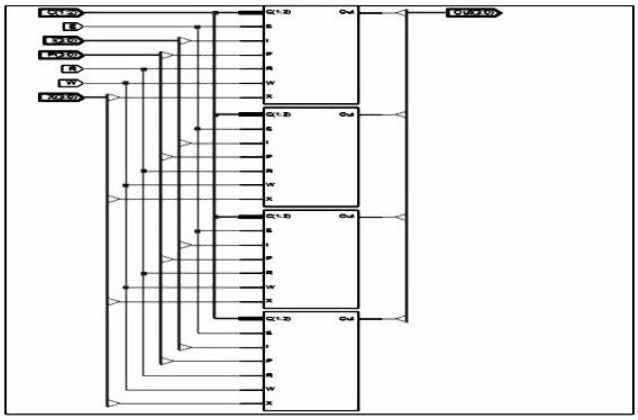


Fig-19

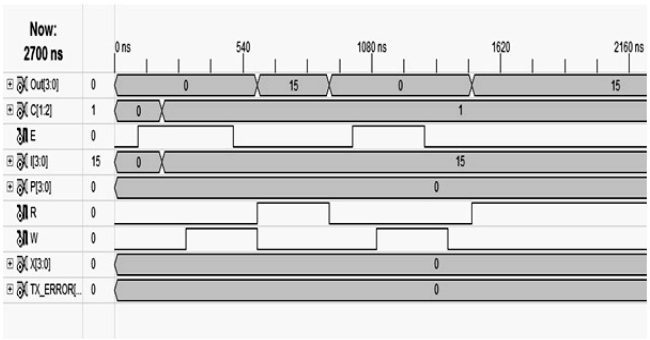


Fig-20

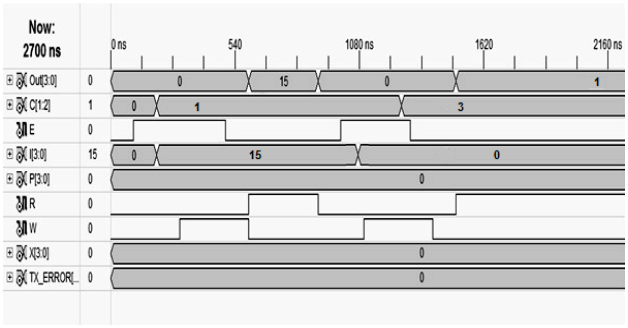


Fig-21

The above Fig-20 shows the test bench waveform in normal mode of operation of 4-bit R/W memory design & Fig-21 shows the test bench waveform in the test mode of operation.

The proposed 8-bit R/W Memory is being simulated and the RTL schematic is shown by Fig-22 & output wave form is given below.

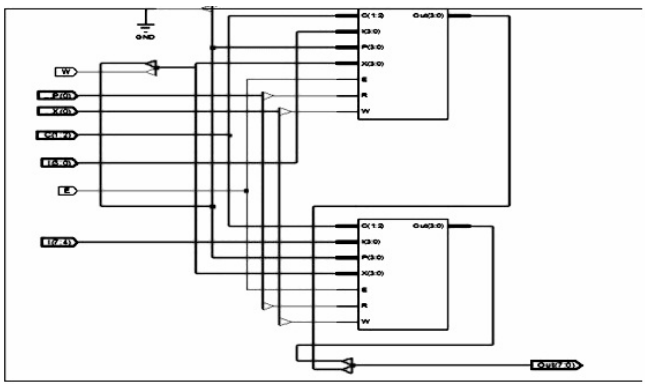


Fig-22

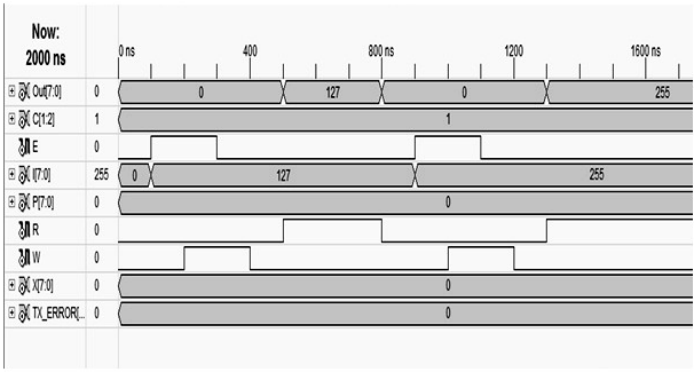


Fig-23

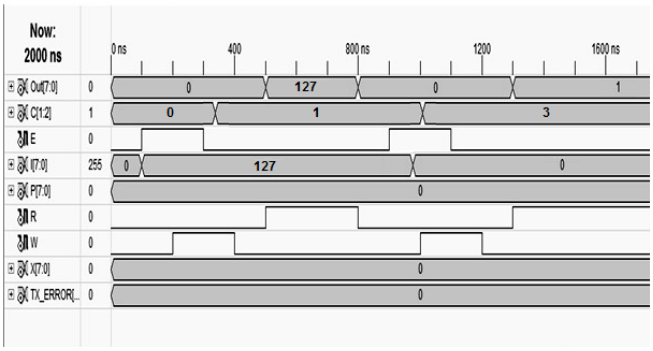


Fig-24

The above Fig-23 shows the test bench waveform in normal mode of operation of 8-bit R/W memory design & Fig-24 shows the test bench waveform in the test mode of operation.

VI. Comparative Study

Table-2

Type	CMOS		QCA		
	No, of gates	No, of input & Output	No, of gates	No, of input & Output *	Quantum cost
1-bit R/W Memory	5-Nand gate, 2-tristate buffer	4- input & 1- output	4-Fredkin gate	5- input & 5 output **	20
4-bit R/W Memory	20-Nand gate, 8-tristate buffer	7- input & 4- output	16-Fredkin gate	8- input & 20 output ***	80
8-bit R/W Memory	40-Nand gate, 16-tristate buffer	11- input & 8-output	32-Fredkin gate	12-input & 40 output ****	160
* The QCA circuits have garbage output at a cost of lesser number of gates as compared to CMOS circuits ** 1-bit R/W Memory has 4-garbage output *** 4-bit R/W Memory has 16-garbage output **** 8-bit R/W Memory has 32-garbage output					

VII. Conclusion & Future Work

This paper contributes to the design of sequential memory circuits based on conservative reversible logic which is tested on two input vectors for detection of stuck-at faults. It also serves a promising testing scheme for detection of transient and permanent faults, most responsible for parity mismatching. In terms of testability & performance the proposed memory designs outperform the memory circuit implemented through conventional designs. Conventional sequential memory circuits does not provide inherited support for testability. So it needs modification to provide the testing capability. Complex sequential circuit design requires huge number of test vectors for fault detection. At the same time the proposed design can be tested by only two test vectors, all 0s and all 1s.Also the testing methodology is based on parity preserving property of Fredkin gate useful for detection of both permanent & transient faults. In conclusion, this paper represents reversible sequential circuit design with unique testing mechanism to detect stuck-at-faults using minimum the number of

test vectors, as well as detection of single missing/additional cell defects.

Since this QCA seems to be the most promising field in nanotechnology based VLSI low power optimization designs & testing. Thus any future work is possible in field of testing & sequential circuit designs.

References

[1] J. Ren and V. K. Semenov, "Progress with physically and logically reversible superconducting digital circuits," *IEEE Trans. Appl. Super- conduct.*, vol. 21, no. 3, pp. 780-786, Jun. 2011.

[2] S. F. Murphy, M. Ottavi, M. Frank, and E. DeBenedictis, "On the design of reversible QDCA systems," Sandia National Laboratories, Albuquerque, NM, Tech. Rep. SAND2006-5990, 2006.

[3] H. Thapliyal and N. Ranganathan, "Reversible logic-based concurrently testable latches for molecular QCA, " *IEEE Trans. Nanotechnol.*, vol. 9, no. 1, pp. 62-69, Jan. 2010.

[4] P. Tougaw and C. Lent, "Logical devices implemented using quantum cellular automata," *J. Appl. Phys.*, vol. 75, no. 3, pp. 1818-1825, Nov. 1994.

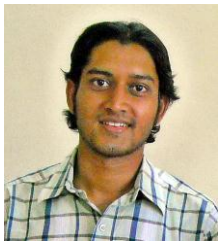
[5] P. Tougaw and C. Lent, "Dynamic behavior of quantum cellular automata," *J. Appl. Phys.*, vol. 80, no. 8, pp. 4722-4736, Oct. 1996.

[6] H. Thapliyal and N. Ranganathan, "Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs", 23rd International Conference on VLSI Design, 2010.

[7] E. Fredkin and T. Toffoli, "Conservative logic," *Int. J. Theor. Phys.*, vol. 21, nos. 3-4, pp. 219-253, 1982.

[8] Ramesh Gaonkar, "Microprocessor Architecture, Programming, and Application with the 8085", 3.2 Memory pp.63-65, fifth edition, august 2011.

[9] Xilinx's EDA tool support, http://www.xilinx.com/support/download/index.htm.



Soumyajit Biswas is pursuing M.Tech with specialization in VLSI & ES from KIIT University ,Bhubaneshwar, Odisha, India. received Master in Science degree in electronics from Devi Ahilya Vishwa Vidyalaya, Indore, M.P., India in 2012 and the Bachelor in Science degree in electronics from Calcutta University, Kolkata, West Bengal, India in 2010. His current research interest include reversible logic, its application in quantum computing, testing of reversible sequential circuits, ultra low power circuit design in VLSI, testable memory and counter designs, QCA based technologies and designs.

Ganesh Lakshmana Kumar Moganti is currently the Assistant professor in School of Electronics Engineering , KIIT University, Bhubaneshwar, Odisha, India. He received his M.Tech with specialization in VLSI & ES from Maulana Azad National Institute of Technology, Bhopal, M.P, India in 2012. received B.Tech degree in electronics & communication engineering from Gudlavalleri Engineering college, Gudlavalleru, A.P, India in 2010. His current research interest include testing of PLA, reversible sequential circuits, ultra low power circuit testing in VLSI , testing of emerging technologies and architecture.