

Operational Transresistance Amplifier Using Submicron Technology

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Abstract: Operational Transresistance Amplifier is important active element in Analog integrated circuits and system. The OTRA is receiving increasing attention as a basic building block in analog circuit design. It is relatively a new building block operating from low voltage supplies and overcomes the finite gain bandwidth product associated with traditional op-amp. The basic principle behind the design of OTRA is to provide amplification of high frequency signals with the using standard operational amplifier. In this work effort is made to study the role of OTRA as an active building block in analog circuits. Various CMOS realization of OTRA present in the literature are studied and these circuits are used to realize various signal processing and generating circuits. Based upon component sensitivity tendency and variation amount, just properly adjusting one or two resistances by a small difference, or giving approximate component values for achieving precise output responses is investigated and developed different OTRA realization.

Keywords: OTRA, CMOS, VLSI.

I. Introduction

The operational Transresistance amplifier (OTRA) plays a very important role as an active element in analog integrated circuits due to their low input and output impedances which eliminates limitations of response time due to capacitive time constants. Both input terminals are internally grounded, thereby purge parasitic capacitances of the input. OTRA has the benefits of a high slew rate & extensive bandwidth. The Differential Operational Transresistance Amplifier (OTRA) is a four terminal analog building block, besides the power terminals.

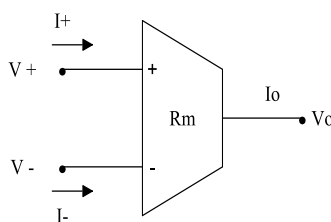


Fig 1. Block diagram of OTRA

The port relationship of OTRA may be characterized by the following matrix form:

$$\begin{bmatrix} V+ \\ V- \\ Vc \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ Rm & -Rm & 0 \end{bmatrix} \begin{bmatrix} I+ \\ I- \\ Io \end{bmatrix}$$

Where Rm is the Transresistance of the OTRA. Since input terminals of this element are internally grounded, most effects of parasitic capacitances at the input disappear. For ideal operation, the Transresistance (Rm) approaches infinity, forcing the input currents to be one and the same. Thus, OTRA must be used in a feedback configuration in a way that is similar classical operational amplifier.

II. OTRA CMOS Realization For Signal Processing.

A. Differential Operational Transresistance Amplifier as signal processing system.

The Differential Operational Transresistance Amplifier (OTRA) is a four terminal analog building block, besides the power terminals, with a describing matrix in the form given by

$$\begin{bmatrix} V_1 \\ V_2 \\ V_{oA} \\ V_{oB} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_m & -R_m & 0 & 0 \\ -R_m & R_m & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_{oA} \\ I_{oB} \end{bmatrix}$$

Circuit symbol of the Differential OTRA.

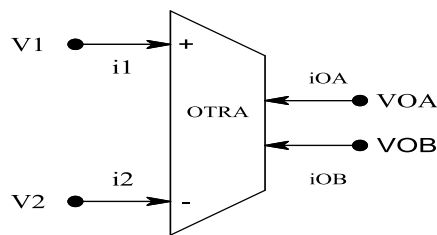


Fig.2. Block diagram of Differential OTRA

Input as well as output terminals are identified by low impedances. The input terminals are virtually grounded, leading to circuits that are inconsiderate to the stray capacitance. For ideal operation, the Transresistance gain, R_m approaches infinity forcing the input currents to be identical. Thus the OTRA must be used in a negative feedback configuration in a way that is similar to conventional opamp. OTRA has indistinguishable transmission belonging to the current-feedback op-amp, but with two low-impedance inputs and two low-impedance outputs for the Differential OTRA. Since the input terminals of these circuits are virtually grounded, they are suitable for cascade connection

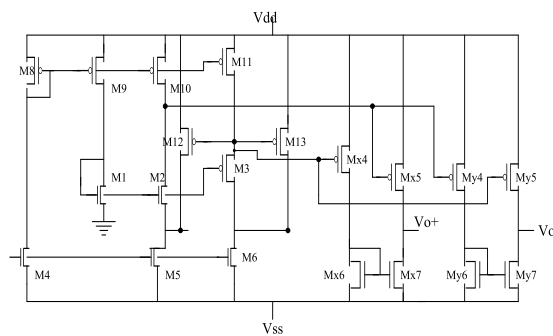


Fig.3. CMOS Realization of OTRA

The proposed CMOS differential OTRA is illustrated in Figure 3. This circuitry also includes the four power-down transistors which generates the enabled power-supply. OTRA is active when the EN input is at the VSS voltage level. When the EN input is at the VDD voltage level, all the system is in the power-down mode.

This basic input cell consists of four transistors which are illustrated in Figure 4. These four transistors generate two Class AB current mirror connection. In the static state I_1 and I_2 are biased automatically to the half of the power supply. For this design the initial value for I_1 and I_2 is 0V as virtually grounded. The input currents are directly connected to the I_1 and I_2 nodes. So the input current directly flow through the drain of the transistors. If one basic cell is used, the OTRA input will not be symmetrical. Because, for the given basic cell, the input I_1 is formed by the use of two diode connected NMOS (M9) and PMOS (M21) transistors, but at the input I_2 there are no diode connections. For that reason, a second basic cell is placed into the design, by replacing the input pins, which input I_2 is applied to the two diodes connected input part of the basic cell and input I_1 is applied to the other input as given in Figure 4.

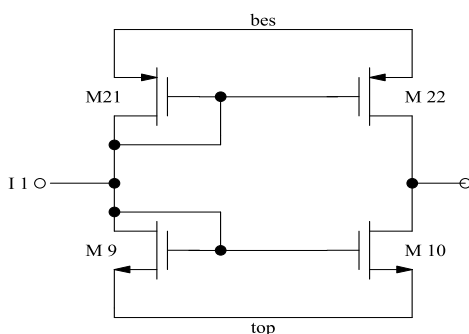


Fig.4. Basic input cell

B. Technology used for designing operational transresistance amplifier.

This paper introduces the technology, design and simulation of CMOS integrated circuits. The evolution of integrated circuit (IC) fabrication techniques is a unique fact in the history of modern industry. The improvements in terms of speed, density and cost have kept constant for more than 30 years. By the end of 2004, “System-on-Chips” with about 300,000,000 transistors will be fabricated on a single piece of silicon no larger than 2x2 cm. In this paper present some information illustrating the technology scale down. semiconductor industry which has witnessed an explosive growth of integration sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. As the CMOS process technology shrinks, it has driven the VLSI industry towards very high integration density and system on chip designs and beyond few GHz operating frequencies, critical concerns have been arising to the severe increase in power consumption and the need to further reduce it. Moreover, the explosive growth driving the designers to strive for smaller silicon area, higher speeds, longer battery life, and more reliability. Power is one of the premium resources a designer tries to save when designing a system.

III. Proposed Work

To achieve the proposed OTRA, different methodology and techniques can be used for research and design OTRA using CMOS technology for low power consumption.

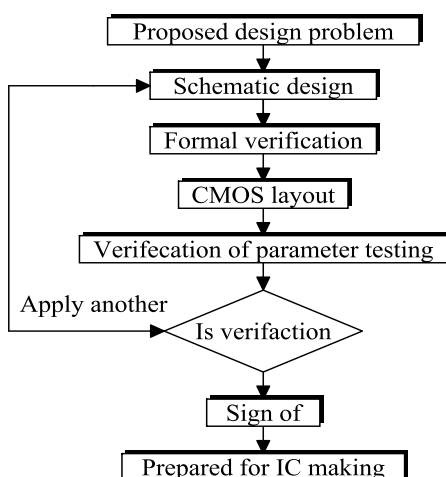


Fig.6. Flow chart of proposed work

V. Implementation

5.1. Cmos Layout Design

The layout of power amplifier circuit shown in Figure 5 is done using professional software Microwind 3.1. The layout has area 9.1um², which is fairly small as compared to other power amplifiers. Parasitic extraction and Post simulation is performed successfully.

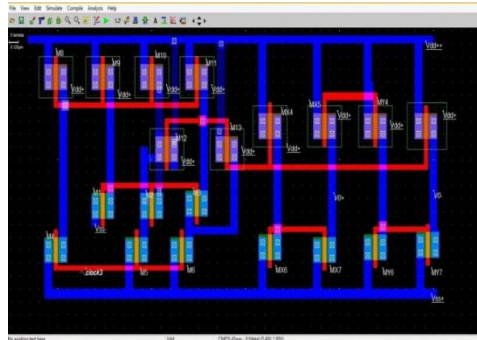


Figure 5.1. Layout of Power Amplifier using 45nm technology

5.2.Simulation Result

Simulations at the schematic level were performed using microwind 3.1 tool. Power consumption can be calculated from DC simulations. Simulated output voltage wave forms of differential trans-resistance power amplifier shown in figure 6. Output voltages v_{o+} & v_{o-} are amplified voltage of difference between two input voltage with 1v operating voltage given by clock3. Figure 7 shows simulated voltage and current wave forms of power amplifier. It is evidence that current depends on the input clock of power amplifier. V_{o+} and V_{o-} - Simulated output voltage wave forms of power amplifier for two different input voltages.

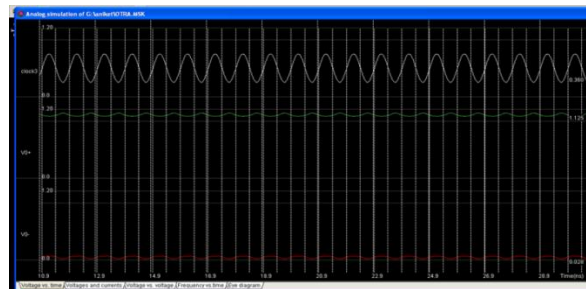


Figure5.2.Stimulated output voltage waveform

Simulated voltage and current waveforms of power amplifier.

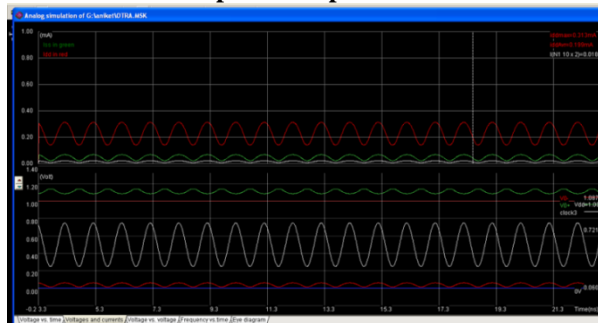


Figure5.3. Simulated voltage and current wave forms of power amplifier.

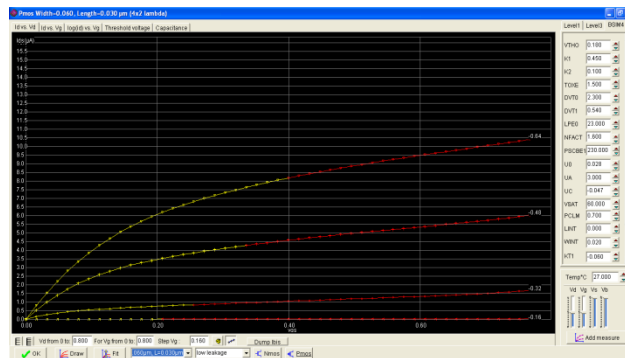


Figure5.4.VI characteristics of Transistor

MOS	W (μm)	L (μm)
P1-P7	0.250	0.050
N1-N10	0.250	0.050

Table 1 Transistor aspect ratio of circuit

VI. Conclusion

This paper presents a modified CMOS realization of the differential operational Transresistance amplifier and its application. In many applications high speed and efficient power consumption is required is desired. For this purpose conventional transistor technique are usually chosen, but this results in lower power consumption. So, the different sub-micron technologies are used. A sub-micron system integrates millions and millions of Electronic components in a small area .The main objective behind the use of this technology is to make the analog and digital system as compact as possible and more power efficient with the required functionality of OTRA and VLSI. The Low Power is the key contribution of the main processing blocks in OTRA system. In research there is used of CMOS 45nm –High/metal/strain-8metal copper.

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