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Review of Electromagnetic failure, optimization techniques and stress prediction in Interconnect

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***Abstract**: The ever increasing demand of digital computing and wireless communication have been driving the semiconductor technology to change with passing days. Modern electronics system integrates more complex component and devices, which result in a very complex electromagnetic field environment Moore's law has driven the scaling of digital electronic devices, dimensions and performances over the last 40 years. In today's world, there is demand of devices which are faster, better and having less power consumption. Now we need to better optimize the circuit at available technologies. Interconnection used to connect components on a VLSI chip, chips on a multichip module and to connect multichip modules on a system board. Most of the chips are covered by Interconnects. On-chip interconnects which was considered only as a parasitic load before 1990s became the real performance bottleneck due to its extremely reduced cross section dimension [31]. Today, on-chip global interconnect with conventional Cu/low-k and delay optimized repeater scheme faces great challenges in the nanometer regime, imposing problems of slower delay, higher power dissipation and limited bandwidth.*

***Key words:** On chip interconnect, low-k dielectric, stress prediction*

I. INTRODUCTION

The ever decreasing interconnects cross section dimensions give rise to increase in resistance. In addition, surface and grain-boundary scattering of electrons in Cu becomes a serious problem as the wire size becomes almost comparable to the grain size of Cu. Eventually leading to higher resistivity than bulk Cu. Putting all these together, degradation of the RC time constant of on-chip metal wires becomes more serious. As a consequence, the continuous performance degradation of on-chip Cu/low k interconnects is one of the greatest challenges to maintain Moore's law alive while the scaling of transistors‟ dimension has provided relentless delay improvement. The scaling of interconnects dimension deteriorates not only delay time, but also all related interconnect performance metrics, such as power dissipation, reliability, and bandwidth, for local, semi-global and global levels. The on-chip power dissipation problem is coupled with an increasing number of repeaters to alleviate long RC time constant of Cu wire, switching activity factor, an increase of operating frequency.

II. REVIEW PROCESS ADOPTED

The review process is divided into five stages in order to make the process simple and adaptable by every researcher. As it reflects from the literature that while beginning the finding of research objectives, it is necessary to start with a broader domain of any area / sub area of interest and narrow down to the specific issue, the process described in the diagram includes the narrowing down. We have followed one of the typical processes to make a literature review and frame the objectives of the research. The process diagram is shown in Fig. 1, which includes all five stages defined as below:

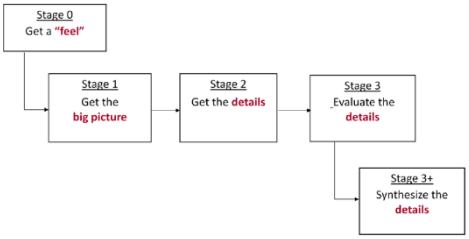

Fig1: Literature Review Process

Stage 0: Get the Feel
Stage 1: Get the Big Picture
Stage 2: Get the Details
Stage 3: Evaluate the Details
Stage 3 +: Synthesize the Details.

III. METHODOLOGIES/SOLUTION APPROACHES

After reviewing the 30 research papers we categories the review in four major issues

(1) Interconnection properties
(2) Design optimization
(3) Interconnect material
(4) Interconnection technology

IV. Findings Of Interconnection Properties

- Two failure modes (2D & 3D Agglomeration) are induced by thermal stress in 140 nm Cu interconnects which leads to low yield & structure change.
- Two kinds of test patterns, Electrical & EXAFS Analysis has done [6].
- Mechanical stresses in metal interconnects cause void formation or metal extrusion into the passivation which leads to failure.
- A numerical solution scheme has been implemented to calculate the atomic fluxes and the evolution of mechanical stress in interconnects.
- Simulation runs were performed using the developed numerical scheme using MathCAD. Stress calculations were simulated for units with known geometry, Electro migration stress conditions and TTF [12].
- Degenerated Exhaustive Direct Charge Measurements (DEDCM) method is used to measure the interconnect capacitance [21].

V. Findings Of Design Optimization

- Optimized Spin-on-Glass processes and a thin layer of CVD silicon dioxide and a curing temperature below the sintering temperature of the metal interconnect layer produced less cracking, no gaps, and smooth features.
- It is able to planarize the surface smoothly without any cracks [5].
- Scheduling Algorithm uses segmented buses to minimize area and energy consumption in interconnect design without performance degradation.
- Dynamic energy consumption can be reduced by about 71% and static energy consumption by about 35% on average when the proposed algorithm is compared with the existing communication cost-conscious scheduling techniques [21].
- Partial Element equivalent circuit model efficiently verifies the signal integrity of highly complex nano scale based interconnect structure.
- It can be used as an indicator for predicting the level of deterioration in the system performance [20].

VI. Findings Of Interconnect Material

- Near Noble Metal Silicides Nisi2 can serve for first level metallization on planar surfaces.
- It shows low resistivity, high current capability & long term stability [1].
- MWCNT/Nano composite Cu films produced by a low cost & low temperature electrochemical method.
- MWCNT content in the film is varied by Cu grain size & CNT Concentration in the electrolyte.
- MWCNT shows enhanced mechanical properties & dense structure without voids [14].
- Liquid metal interconnect used to produce the flexible skin sensor to be used in robots.
- The liquid metal interconnect is better to develop the super flexible skin sensors than the solid metal interconnect in terms of robustness & Flexibility [10].

VII. FINDINGS OF INTERCONNECTION TECHNOLOGY

- Advanced ALIVH Interconnection technology has improved features like low moisture uptake, High Tg, Low CTE & high elastic modulus.
- In this technology, new functional materials have been used & electric interconnections were computed by controlling thickness & viscosity of resin [7].
- ACF interconnection technology is used in flexible electronics to improve the efficiency of flat panel display and the requirement of fine pitch capability.
- It controls the volume fraction of conducting particles into the adhesive film & the problem of larger size and bad resolution quality of flexible electronics has improved [11].
- The Optical interconnection technology is used to improve the efficiency, densities and speed performance of IC.
- It provides better results than the metal interconnection technology in terms of improvement in the overall performance of IC. Planar Interconnects Technology overcomes the electrical performance of Al wire bonding such as in the terms of on-resistance and stray inductance by replacing Al wire bonds with Cu wire bonds [3].

- CMP Process can be used to accommodate the higher degree of process control required in the finer geometry or dual inlaid structures.
- It provides better oxide erosion control for the finer geometry & multiple level structures [29].
- Space Division Multiplexed Microstructure optical fiber bus to be used for a chip to chip optical interconnects (C2OIs) [24].
- Multicore MFs featured several solid cores surrounded by a cladding region, was modeled using a Finite difference BPM Algorithm. Novel copper ball interconnection technology for 60 GHz band 3-D System-in-Package (SiP) modules using organic substrates, used for providing interconnections between substrates. Two balls are used for signal line connection & eight balls are used for ground connection [24].
- Photonics-Electronics Convergence system was used to solve the B.W. Bottleneck problem in inter-chip interconnects.
- This system enables us to replace the function of conventional electronic wires on a printed circuit board (PCB) with the optical interconnects on a silicon substrate with error free data transmission at 12.5 Gbps NRZ [25].
- The solder joint based flip chip interconnection technology has strong potential in terms of its high electrical and mechanical performance and its low manufacturing cost.
- It is used for fine pitch (100 micrometers) and high density requirement [9].
- The T-G2BGA (Tape Gold-Gold gang bond BGA) has a low cost, highly reliable CSP (Chip Size Package) for compactness, and light memory device package to be used in mobile computers and cellular phones for large data storage.
- The parameters in T-G2BGA technology are bump shape, substrate pad surface plating specification, and flip chip bonding conditions [4].
- Photonic technologies are used to relieve the increasing power consumption for the ICT (Information and communication Technology) system.
- The Optical-component technologies, which include LDs, PDs, drivers, and TIAs, are key factors in realizing a high-speed, compact, and low-power 100GbE interface [18].
- VCI technology has introduced to reduce the package size or to enhance the electrical performance of stacked die packages.
- The key processes of VCI technology are coating, laser ablation and conductive glue which have used after die attach, to replace traditional wire bonding technology [19].

VIII. Issue Wise Solution Approaches

Interconnection properties	
Solutions	***Strength***
Math CAD Simulator Tool	It measures Line Stress at Total Time Failure (TTF) [12].
Power/Thermal Management Algorithm.	Significant improvements in reliability [27]
DEDCM method.	Obtain complete capacitance information of interconnect network more accurately and faster [21]
Lead-free solders with a low Ag-content	Stress reduction [17].
Collinear Transition Differential Scanning Calorimetry (DSC).	Large Bandwidth and wide range of coupling coefficient [2].
Dynamic Reliability Model.	Explore the design space [28]
Interconnection Materials	
Multi Walled CNT / Nanocrystalline Copper Film.	1. Cu films show dense structure (without any voids) 2. Enhanced Mechanical properties [14].
Liquid Metal interconnect	Robustness and flexibility [10].
Near Noble Metal Silicides	1. High oxidation rate 2. Low resistivity 3. Low formation temperature of Ni rich phase 4. Provides High current capability 5. Long term stability 6. Metallization level increases [1]
Design Optimization in Interconnects	
Optimized Spin on Glass Process.	Less cracking, no gaps, and smooth features in multilevel interconnect layers [5].
Scheduling Algorithm.	Dynamic energy consumption can

	be reduced by about 71% and static energy consumption by about 35% [20]
Partial Element Equivalent Circuit Model.	Computing the stress evaluation in the line [23]
Interconnection Technology	
Sand Blasting & Laser Filling Method.	Smaller size circuits with high electrical performance & reliability [13]
Advanced ALIVH Interconnection Technology	A short wire length between substrate and via hole shape remains preserved [7].
Anisotropic Conductive Films in Flexible Electronics.	Avoids the problem of larger size and bad resolution quality of flexible electronics [11].
T-G2BGA Interconnection Technology	Low cost, highly reliable CSP (Chip Size Package) for compactness, and light memory devices package [4]
Metal & Optical Interconnection	Improves overall performance [3].
Planar Interconnects Technology.	R_{th} reduces to 0.69K/W to 0.55K/W (approx 20%) [22]
G-Helix Low-K Interconnects	Fabrication of the interconnects at 100 um pitch [15].
CMP Process	It provides better oxide erosion control for the finer geometry & multiple level structures [29].
Space Division Multiplexed Micro structured optical fiber bus	Micro structured optical fiber bus low cross talk & low bend loss [24]
Copper balls interconnection technology	Improves the Transmission Characteristics of interconnects simultaneously providing low cost & keeping flat & stable spaces v/w substrates [16].
Photonics-Electronics Convergence system	Error Free Data Transmission in inter-chip Interconnects [25]
VCI Technology	Reduce the package size [19]
CNT Array as High Impedance Interconnects.	Radiative heating mode technique keeps the substrate temperature, low [26].

IX. Common Findings

- Out of 30 Research Papers which we reviewed, we found 4 Main issues.
- First Issue is Interconnects Materials, The Best Approach used in this issue is Near Noble Metal Silicides (NiSi2) as it provides low resistivity, high critical current density & long term stability of interconnect lines While the approach Multi walled CNT/ Nano Crystalline Cu Film is not so good as in this technology the thermal conductive of interconnects drastically decreases.
- The Second Issue is Design Optimization of Interconnects. The Best Approach used in this issue is Scheduling Algorithm as this approach minimizes the interconnection's dynamic energy consumption by 71% and static energy consumption by about 35 % without performance degradation. While the approach Partial Element Equivalent Circuit Model is very complex.

Technology	Limitation	Scope of work
Near Noble Metal Silicides	Surface roughness caused by micro cracks & broken steps after high temperature metal layer formation [1]	$Nisi_2$ along with the refractory metal silicide i.e. $TiSi_2$ & WSi_2 $Nisi_2$ along with the refractory metal silicide i.e. $TiSi_2$ & WSi_2
MWCNT	Thermal conductivities were drastically decreased & Resistivity Increases [14]	New additives in order to enhance the thermal & electrical
Metal interconnect technology	Degrades the performance of IC [5].	A combination of metal and optical interconnects to improve the overall performance of the chips.

Dynamic Reliable model	Not suitable to Compare model Prediction with Experimental data [28]	Further modified by considering other failure mechanisms such as fast thermal cycling, stress-migration
Low k dielectric	The fabrication process is not cost competitive [15]	Number of masking steps should be reduced
Wire bond technology	Increase the size of package body with respect to the number of dice stacked in the package [19]	Optical interconnect

X. Conclusion

Hereafter finding the solution approaches, we concluded that Interconnect Technology is the main area into which the future work can be done. We found 15 Solution approaches out of which Advanced ALIVH Interconnection Technology, CMP Process, Planar Technology, Photonics-Electronics Convergence system & G-Helix Low-K Interconnects are most promising due to their advantages & properties. The exhaustive review could finally lead to extract findings in the area, strengths and weaknesses and scope of work during M. Tech thesis.

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