

## Power Efficient Standby Switch Based Domino Logic Circuit

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**Abstract:** As the technology is continuously scaled, leakage currents become a major contributor to the total power dissipation. A reduction in power supply voltage is necessary to reduce dynamic power and avoid reliability problems in deep sub-micron regions. Threshold voltage reduction accompanies supply voltage scaling to maintain the performance but it exponentially increases the sub threshold leakage currents. Domino logic circuits are extensively used in high performance microprocessors due to their superior speed and area characteristics compared to static CMOS circuits. But these circuits are susceptible to high leakage. In this work, a standby switch is used which turns off all the high threshold voltage transistors and thereby enhances the effectiveness of dual threshold voltage CMOS technology to reduce sub threshold leakage current. Also CMOS NAND gates are employed instead of the output inverter to pre charge both the dynamic node and output to logic 1 during its pre charge phase, so that the subsequent logic function will be evaluated correctly in its evaluation phase. The proposed techniques are compared by performing detailed transistor level simulations on benchmark circuits in 45nm technology using Microwind3 and DSCH3 CMOS layout CAD tools.

**Keywords:** Domino logic, keeper transistor, Power Delay Product, sleep switch.

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### I. Introduction

In recent years, the demand for power-sensitive designs has grown significantly. Semiconductor devices are aggressively scaled by each technology generation to achieve high-performance and high integration density. Due to increased density of transistors in a die and higher frequencies of operation, the power consumption in a die is increasing.

Supply voltage is scaled to maintain the power consumption within the limit. However, scaling of supply voltage is limited by the high-performance requirement. Hence, the scaling of supply voltage only may not be sufficient to maintain the power density within the limit, which is required for power-sensitive applications. Circuit technique and system-level techniques are also required along with supply voltage scaling to achieve low-power designs.

While the supply voltage is scaled down to achieve lower switching energy per device, to maintain high performance there is a need for commensurate scaling of the transistor threshold voltage ( $V_{th}$ ). Scaling of transistor threshold voltage is associated with exponential increase in sub threshold leakage current [1]. Aggressive scaling of the devices not only increases the sub- threshold leakage but also has other negative impacts such as increased Drain-Induced Barrier Lowering (DIBL),  $V_{th}$  roll-off, reduced on-current to off current ratio, and increased source-drain resistance. In the nano-meter regime, a significant portion of the total power consumption in high-performance digital circuits is due to the leakage current. High-performance systems are constrained to a predefined power budget and the leakage power reduces the available power and impacting performance. It also contributes to the power consumption during standby operation and reduction in battery life. Hence, appropriate techniques are necessary to reduce leakage power while maintaining the high performance.

The focus of this paper is to design low power domino logic circuit techniques which offer reduced power delay product and minimized leakage current in DSM technology. The organization of the paper is as follows. A brief review of the sub threshold leakage conduction in CMOS circuits is provided in Section 2. In Section 3, various existing techniques are revised. In Section 4 Proposed Technique using standby switch is explained. In Section 5 simulation results and performance analysis are presented. Finally, conclusions are presented in Section 6.

### II. Sub Threshold Conduction

Sub threshold conduction or sub threshold leakage or sub threshold drain current is the current between the source and drain of a MOSFET as shown in Fig.1, when the transistor is in sub threshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. In the past, the sub threshold conduction of transistors has been very small, but as transistors have been scaled down, leakage from all sources

has increased. For a technology generation with threshold voltage of 0.2 V, leakage can exceed 50% of total power consumption.

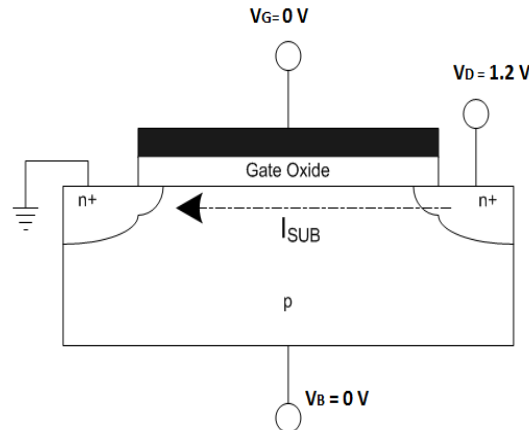


Fig.1 Sub threshold leakage conduction

In current CMOS technologies, the sub threshold leakage current is larger than the other leakage current components. This is mainly because of the relatively low  $V_{th}$  (threshold voltage) in modern CMOS devices.  $I_{sub}$  is calculated using the equation (1),

$$I_{sub} = \frac{W}{L} \mu V_{th}^2 C_{sth} \exp \left[ \frac{V_{gs} - V_t + nV_{ds}}{nV_{th}} \right] \left[ 1 - \exp \left( -\frac{V_{ds}}{V_{th}} \right) \right] \quad (1)$$

Where  $W$  and  $L$  denote the transistor width and length,  $\mu$  denotes the carrier mobility,  $V_{th} = kT/q$  is the thermal voltage at temperature  $T$ ,  $C_{sth} = C_{dep} + C_{it}$  denotes the summation of the depletion region capacitance and the interface trap capacitance both per unit area of the MOS gate, and  $n$  is the drain induced barrier lowering (DIBL) coefficient.  $n = 1 + C_{sth}/C_{ox}$  is the slope shape factor, where  $C_{ox}$  is the gate input capacitance per unit area of the MOS gate.

Clearly, increasing the threshold voltage can decrease the leakage current exponentially. In fact, increasing the threshold voltage by 100mV decreases the leakage current by a factor of 10. However, the large threshold voltage would reduce the operation speed of the circuits.

### III. Survey of Existing Systems

#### 3.1 Standard Dual $V_{th}$ Domino Logic Circuit

Dual-  $V_{th}$  transistors in domino logic circuits are used for reducing the sub-threshold leakage energy consumption [2]-[4], in which the high threshold voltage (high-  $V_{th}$ ) transistors are represented by a thick line are employed on the noncritical precharge paths, alternatively, low-  $V_{th}$  transistors are employed on the speed critical evaluation paths. A two-input standard dual-  $V_{th}$  domino OR gate is shown in Fig.2. The critical signal transitions that determine the delay of a domino logic circuit occur along the evaluation path.

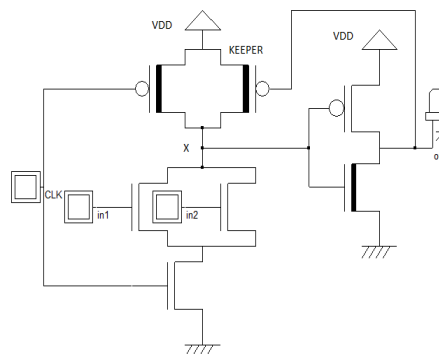


Fig.2 Standard dual  $V_{th}$  domino circuit

In a dual-  $V_{th}$  domino circuit, therefore, all of the transistors that can be activated during the evaluation phase have a low-  $V_{th}$ . Alternatively, the precharge phase transitions are not critical for the performance of a domino logic circuit. Therefore, those transistors that are active during the precharge phase have a high-  $V_{th}$ . Provided that all of the high-  $V_{th}$  transistors are cutoff in a dual- $V_{th}$  domino logic circuit, the sub threshold leakage current is significantly reduced as compared to a low-  $V_{th}$  circuit. The clock is gated high, turning off

the high- pull-up transistor when a domino logic circuit is idle. In a standard dual domino logic circuit, the modes of the remaining high- transistors are determined by the input vectors applied after the clock is gated high. However, the circuit technique does not address energy and delay overhead for entering and leaving its standby mode.

### 3.2 Sleep Switch Dual $V_{th}$ Domino Logic Circuit

To lower the sub threshold leakage currents in an idle domino logic circuit the circuit technique employs sleep switches to place a dual-  $V_{th}$  domino logic circuit into a low leakage state within a single clock cycle. A two-input domino OR logic circuit based on the sleep switch dual-  $V_{th}$  circuit technique is shown in Fig 3. A high-  $V_{th}$  NMOS switch is added to the dynamic node of a domino circuit. The operation of this transistor is controlled by a separate sleep signal [5]. During the active mode of operation, the sleep signal is set low, the sleep switch is cut-off, and it operates as a standard dual-  $V_{th}$  domino circuit.

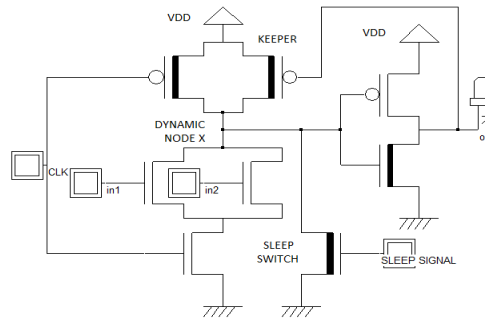


Fig.3 Sleep switch dual  $V_{th}$  domino logic circuit

During the standby mode of operation, the clock signal is maintained high, turning off the high- pull-up transistor of each domino gate. The sleep signal transitions high, turning on the sleep switch. The dynamic node of the domino gate is discharged through the sleep switch, thereby turning off the high-  $V_{th}$  NMOS transistor within the output inverter. The output transitions high, cutting off the high- keeper. Following the low-to-high transition of the output of a sleep switch dual-  $V_{th}$  domino gate, the subsequent gates (fed by the non inverting signals) also evaluate and discharge in a domino fashion. After the node voltages settle to a steady state, all of the high-  $V_{th}$  transistors are strongly cut-off, significantly reducing the sub threshold leakage current [6]. Also, this technique does not require any additional gating on the input signals while strongly turning off all of the high-  $V_{th}$  transistors within a single clock cycle, is significantly more power, delay, and area efficient as compared to the standard dual  $V_{th}$  technique.

### 3.3 Modified Dual $V_{th}$ Domino Logic Circuit

In Fig.3 it can be seen that the circuit output will be logic 0 during its pre charge phase. Hence the second stage cannot evaluate the function itself in its evaluation phase as in a standard two stage dual  $V_{th}$  domino logic circuit to construct a pipeline structure.

To resolve such a problem modified dual  $V_{th}$  domino logic circuit was introduced [7] as shown in Fig.4. In this technique when the clock is gated high, evaluation phase begins and the logic function is evaluated depending on the inputs. When clock is gated low, pre charge phase begins. The clock controlled NMOS transistor which is inserted in the discharging path of the output inverter is used to hold the circuit output logic during the pre charge phase.

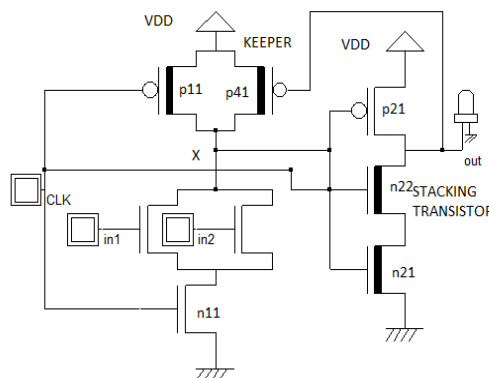


Fig.4 Modified dual  $V_{th}$  domino logic circuit

However simulation results shows that the circuit output has neither charging path nor discharging path in the pre charge phase, since when clock is gated low ( $clk=0$ ), p11 is on, n11 and n22 are both switched off, so node X is pre charged by p11 to  $V_{DD}$  which is system supply voltage, thus, p21 is switched off, so that the circuit output is a tri-state not keeping the previous state.

#### IV. Proposed Technique

In order to deal with the difficulty of previous circuits configuration, a low energy and delay overhead dual-  $V_{th}$  circuit scheme which employs standby switch to place a dual-  $V_{th}$  domino logic circuit into a low leakage state within a single clock cycle was proposed to lower the sub-threshold leakage currents in its idle mode, as shown in Fig 5. A high-  $V_{th}$  standby switch (an NMOS transistor) which is controlled by a separate standby-clock is connected parallel to the low-  $V_{th}$  evaluation block which is the discharging path of node X. The standby switch can lead the circuits enter and leave its standby mode easily with a single clock cycle. Also CMOS NAND gates are employed instead of the output inverter in conventional domino logic to pre charge both node X and circuit output to  $V_{DD}$  (logic 1) during its pre charge phase, so that the subsequent stage will evaluate its logic function correctly in its evaluation phase.

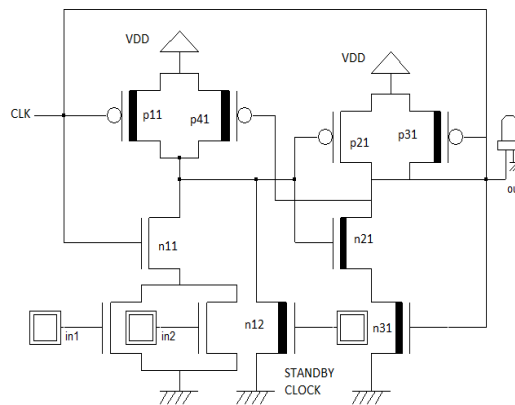


Fig.5 standby switch domino logic circuit

In pre charge mode,  $clk=0$ , p11, p31 is on, n11, n31 is off, and so both node X and circuit output will be pre charged to  $V_{DD}$  (logic 1) by p11 and p31 respectively regardless the state of standby-clock. Meanwhile, the NAND gate output configuration does not affect the circuit operation in its evaluation and standby phase. The operation of proposed dual-  $V_{th}$  domino logic circuit is similar to that of the standard dual-  $V_{th}$  domino logic circuit apart from the pre charge and standby phase.

During the standby mode of operation, the clock signal is maintained high, turning off the high-  $V_{th}$  pull-up transistor p11, p31 and turning on the pull-down transistor n11, n31. The standby-clock transitions high, turning on the standby switch n12, the dynamic node X is discharged through n11 and n12, thereby turning on PMOS transistor p21 and turning off the high-  $V_{th}$  NMOS transistor n21, the circuit output is charged to  $V_{DD}$  (logic 1), cutting off the high- $V_{th}$  PMOS “keeper” transistor, p41. Following the low-to-high transition of the circuit output, the subsequent gates also evaluate and discharge in a domino fashion. After the node voltages settle to a steady state, all of the high-  $V_{th}$  transistors are strongly cut off, significantly reducing the sub-threshold leakage current.

Also this technique, does not require any additional gating on the input signals while strongly turning off all of the high- $V_{th}$  transistors within a single clock cycle, is significantly more power, delay, and area efficient as compared to the existing techniques. In addition, as node X maintains logic 0 during the standby mode operation regardless the input vectors of low-  $V_{th}$  evaluation blocks, it avoids the float state in traditional domino circuits which will cause large leakage current in the output inverters.

Furthermore, the proposed circuits differ from the traditional domino logic circuits by moving the standby switch n12 from node X to the source of n11. This can decrease the capacitance load effects of node X and enhance the circuit operation speed. Also by connecting the discharging transistor n11 of low-  $V_{th}$  evaluation block from ground to node X, the body effect of n11 will be enhanced which increases the threshold voltage and decreases the cut off leakage current. In addition, connecting n11 with node X can partly avoid the charge sharing problems in domino circuits styles, since during pre charge phase, n11 is cut off, preventing the charge redistribution on node X.

### V. Simulation Results and Performance Analysis

To assess the reduction in power offered by the above discussed circuit techniques, Domino logic gates were simulated according to the test circuit for the various existing circuit techniques in 45-nm technology using MICROWIND3 and DSCH3 CAD CMOS layout tools.

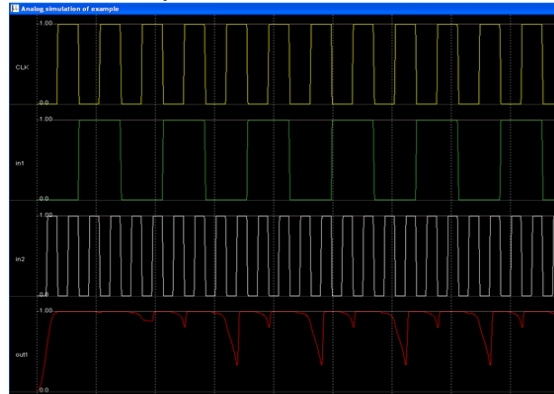


Fig.6 output waveform for standard dual  $V_{th}$  domino circuit

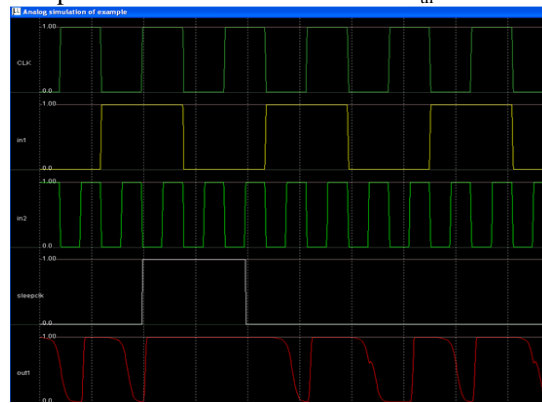


Fig.7 output waveform for sleep switch dual-  $V_{th}$  domino circuit

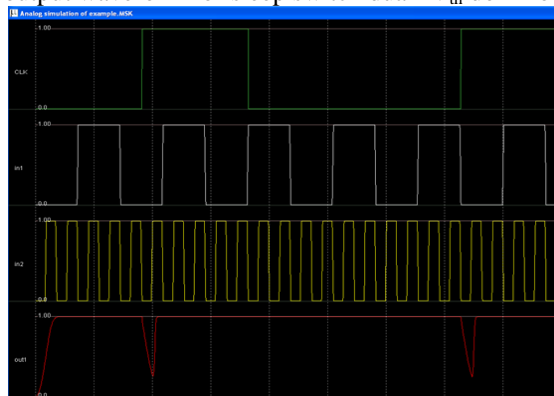


Fig.8 output waveform for Modified dual  $V_{th}$  domino circuit

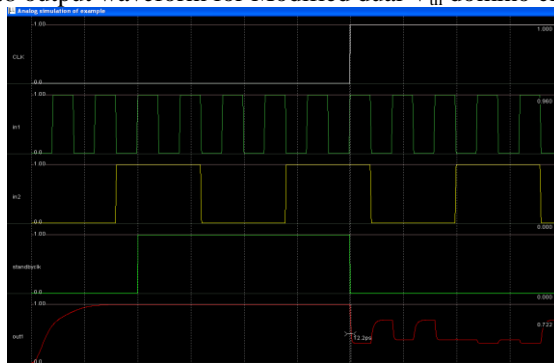


Fig.9 output waveform for proposed technique

Table 1: Optimum Values For 2 Input OR Gate.

Circuit Techniques	Area ( $\mu\text{m}^2$ )	Power ( $\mu\text{W}$ )	Delay (ns)	PDP (fJ)
Standard dual $V_{th}$ technique	10.1	9.689	0.035	0.339
Sleep switch dual $V_{th}$ technique	12.0	8.050	0.035	0.281
Modified dual $V_{th}$ technique	11.3	2.161	0.025	0.054
Proposed technique	14	1.902	0.020	0.038

From the Table 1, it is observed that the PDP of proposed technique reduces by 29% when compared with the modified dual  $V_{th}$  technique and reduces by 88% when compared with standard dual  $V_{th}$  technique. The performance comparison is shown as graph in Fig.10.

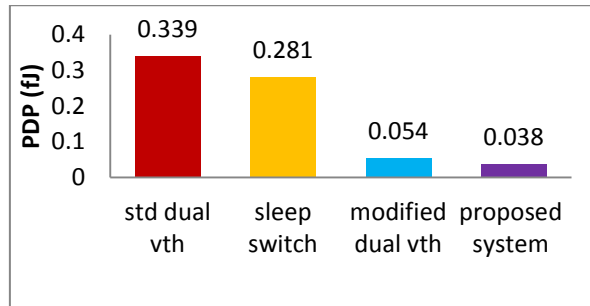


Fig.10 PDP comparison for various circuit techniques

## VI. Conclusion

In this work, an efficient method to minimize power and increase the speed of arithmetic circuits is designed using standby switch dual- $V_{th}$  domino logic techniques. Charge sharing problems associated with dynamic and domino families are also removed in the proposed design. By avoiding these power wastages, our proposed dual- $V_{th}$  domino logic technique reduces the total power consumption in its idle or sleep mode where no computation is taking place. Simulation has demonstrated that high speed and low power were obtained from the proposed dual- $V_{th}$  domino logic technique by performing detailed transistor level simulation on benchmark circuits using Microwind 3 and DSCH3.1 layout CAD tools.

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