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Design of Hybrid Pulsed FlipFlop Featuring Embedded logic

N. Karthika[1], S. Jayanthy[2]
[1,2](Department of ECE-PG,Sri Ramakrishna Engineering College, India)

Abstract: *This paper introduces a novel power efficient hybrid pulsed flip-flop (HPFF) with embedded logic module (HPFF-ELM) based on transmission gate scheme. The HPFF possess a hybrid architecture that combines the merits of dynamic and static structures. The performance of modern high performance flip-flops are compared with that of HPFF at different data activity. The proposed HPFF architecture is power efficient and has the ability to incorporate logic functions into the flip-flop which forms HPFF-ELM. The performance comparisons and analysis is made in TSMC process using mentor graphics EDA tool. The HPFF and HPFF-ELM is compared with other state-of-the-art design. The performance improvements indicate that the proposed designs are well suited for modern high-performance circuits where power dissipation and area overhead are of major concern.*

Key words: *Flipflops, area, power dissipation, speed, delay, embedded logic*

I. INTRODUCTION

Sequential logic circuits, such as registers, memory elements, counters etc., are heavily used in the implementation of Very Large Scale Integrated (VLSI) circuits [1]. As VLSI circuits continue to evolve and technologies progresses, the level of integration is increased and higher clock speed is achieved [2]. Flip-flop is a data storage element. The operation of the flip-flops is done by its clock frequency [3]. When multistage Flip-Flop is operated with respect to clock frequency, it processes with high clock switching activity and then increases time latency. Therefore it affects the speed and energy performance of the circuit [4]. Various classes of flip-flops have been proposed to achieve high-speed and low-energy operation. Understanding and selecting the appropriate choice of flip-flop topology for a particular application is difficult, since it involves a large number of existing topology, and depends on area, power dissipation and transistor sizing. In specific, efficient topology and good layout design is necessary to achieve reliable results that are usable in practical design.

Several researchers have worked on flip-flop design, but they are mostly focused on one or a few types of flip-flops or applications [4]. The need for comparing different designs and approaches is the main motivation for this paper. The flip-flops considered for analysis are PowerPC 603, Hybrid-Latch flip-flop (HLFF), Semi-dynamic flip-flop (SDFF), conditional data mapping flip-flop (CDMFF), Cross charge control flip-flop (XCFF) and Dual Dynamic pulsed flip-flop (DDFF). The main trade-offs of any flip-flop are very important for a design engineer when designing a circuit or for a tool that automates the process of design. A new Hybrid Pulsed flip-flop (HPFF) and a novel embedded logic module (HPFF-ELM) based on HPFF is proposed. The proposed design is based on transmission gate scheme. Observing the delay discrepancy in latching data "1" and "0", the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speedup the data transition. This mechanism is implemented by introducing a simple transmission gate for extra signal driving. When combined with the pulse generation circuitry it forms a new pulsed flip-flop design with enhanced speed and power delay product performances. The performance of modern high performance flip-flops are compared at different data activity. The HPFF-ELM provides the speed, area and power efficient method to reduce the pipeline overhead and to incorporate logic functions into the flip-flop. The rest of this paper is organized as follows. Section 2 presents background information about various flip-flop designs and its characteristics. Section 3 explains the proposed architectures and Section 4 shows the performance comparison of these flip-flops. Finally, Section 5 gives the conclusion.

II. FLIPFLOP TOPOLOGIES ANALYZED

The flip-flop circuits shown in Fig. 1 are extracted from references [1], [2]. They were built using mentor graphics EDA tool and sized for minimum size to function correctly. The following is a short description of the flip-flop circuits. Power PC master-slave latch. It is one of the fastest classical structures and its main advantage is the short direct path and low power feedback [5]. This flip-flop is the transmission gate flip-flop, it has a fully static master–slave structure, which is constructed by cascading two identical pass gate latches and provides a short clock to output latency.

Hybrid–latch flip-flop (HLFF) that is one of the fastest flip-flop structures [8]. It is robust to clock signal slopes, but it does have a positive hold time. This is very suitable for high performance systems [7]. Also

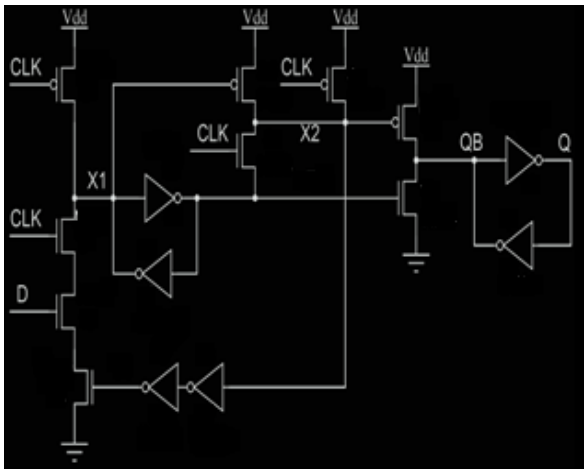
it is inefficient in embedding logic. This structure is basically a level sensitive latch which is clocked with an internally generated sharp pulse [8]. Another hybrid flip-flop, the semi-dynamic flip-flop (SDFF) [9]. It is one of the fastest structures if not the fastest of all the flip-flops described in this paper. This is still best suited for high performance designs, though its power consumption is moderate [10]. Similar to hybrid-latch flip-flop semi-dynamic flip-flop is also classified in the group of pulse-triggered flip-flops. Two main building blocks are a level sensitive latch and a pulse generator [12].

The conditional data mapping flip-flop (CDMFF) is one of the most efficient among the state-of-the-art. It uses an output feedback structure to conditionally feed the data to the flip-flop [13]. This reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. Also, the additional transistors added for the conditional circuitry make the flip-flop bulky and cause an increase in power dissipation at higher data activities.

Cross charge control flip-flop (XCFF) reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors as in Fig. 1(a). Since only one of the two dynamic nodes is switched during one CLK cycle, the total power consumption is considerably reduced without any degradation in speed. Also XCFF has a comparatively lower CLK driving load [15]. The large precharge-capacitance in a wide variety of designs results from the fact that both the output pull-up and the pull-down transistor are driven by this precharge node [16]. These transistors being driving large output loads contribute to most of the capacitance at this node. This common drawback of many conventional designs was considered in the design of XCFF. The effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design.

Dual Dynamic Hybrid flip-flop (DDFF) has large precharge-capacitance in a wide variety of designs results from the fact that both the output pull-up and the pull-down transistor are driven by this precharge node. These transistors being driving large output loads contribute to most of the capacitance at this node. This common drawback of many conventional designs was considered in the design of XCFF [1]. It reduces the power dissipation by splitting the dynamic node into two, each one separately driving the output pull-up and pull-down transistors as shown in Fig.1(b). Since only one of the two dynamic nodes is switched during one CLK cycle, the total power consumption is considerably reduced without any degradation in speed. Also XCFF has a comparatively lower CLK driving load. One of the major drawbacks of this design is the redundant precharge at node *X*2 and *X*1 for data patterns containing more 0s and 1s,respectively. In addition to the large hold time requirement resulting from the conditional shutoff mechanism, a low to high transition in the CLK when the data is held low can cause charge sharing at node *X*1. This can trigger erroneous transition at the output unless the inverter pair INV1-2 is carefully skewed. This effect of charge sharing becomes uncontrollably large when complex functions are embedded into the design.

The revised structure of the dual dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) is shown in Fig. 1(c). Note that in the revised model, the transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of nMOS transistors in the stack increases. The same reason makes XCFF also incapable of embedding complex logic functions. In order to gets a clear picture of the charge sharing in XCFF it was simulated with different embedded functions and the amount of worst case charge sharing was calculated.



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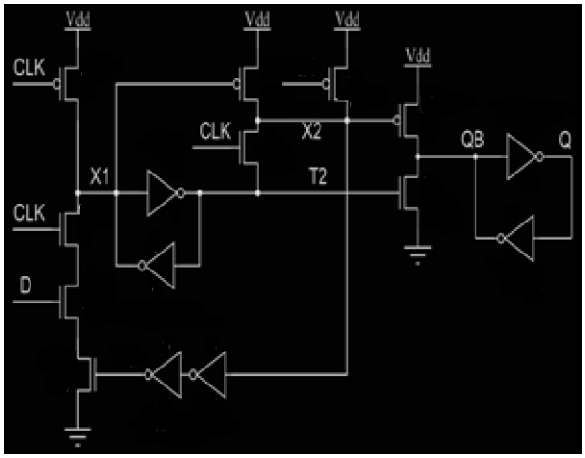

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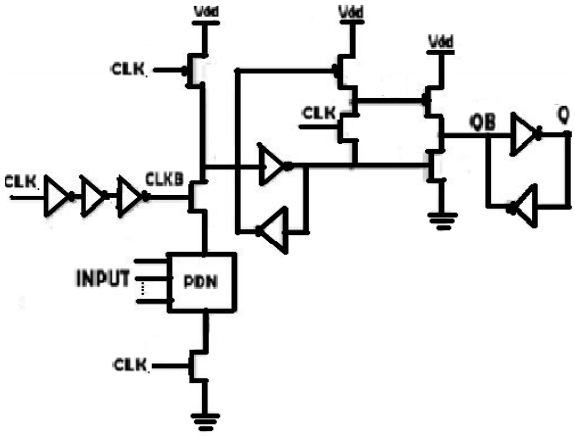
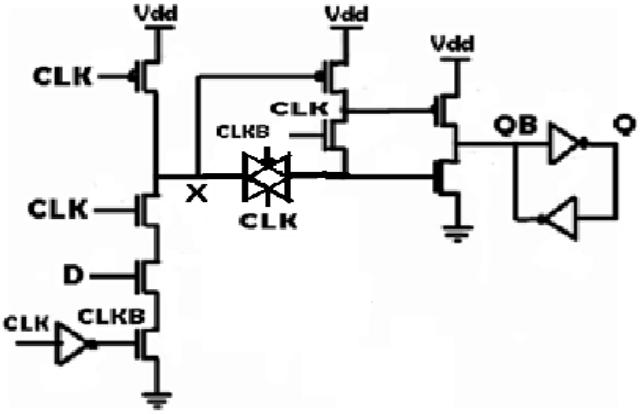


(c)

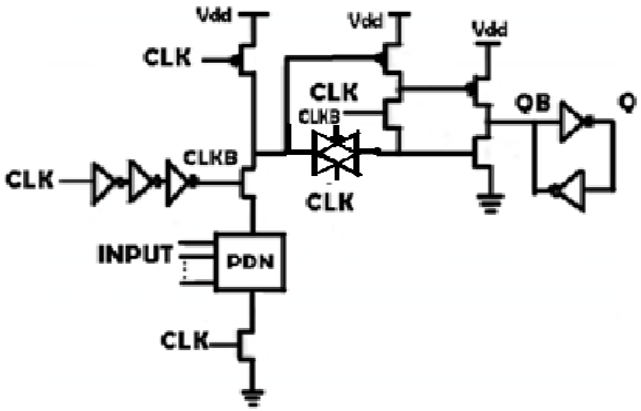
Fig. 1 Schematic view of Flip-flop topologies analyzed (a) XCFF (b) DDFF (c) DDFF-ELM

III. PROPOSED ARCHITECTURES

The novel hybrid pulsed flip-flop (HPFF) is designed based on transmission gate scheme. Referring to fig. 2(a), when a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the transmission gate, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback assume complementary signal levels and the pull-down path of node X1 is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node X1 is discharged to turn on transmission gate, which then pulls node Q high. This corresponds to the worst case timing of the FF operations as the discharging path conducts only for a pulse duration. However, with the transmission gate scheme, a boost can be obtained from the input source via the transmission gate and the delay can be shortened. Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because pass transistor conducts only for a very short period. When a "1" to "0" data transition occurs, transmission gate is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of "0" to "1" data transition, the input source bears the sole discharging responsibility. Since transmission gate is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking too enhance the speed. In addition, since a keeper logic is placed at output node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted. The hybrid pulsed flip-flop has the ability to incorporate various logic functions into the flip-flop as of DDFF. The HPFF-ELM provides delay, area and power efficient technique. Based on signal feed through scheme, the HPFF-ELM is also designed as shown in fig. 2(b).



(a)



(b)

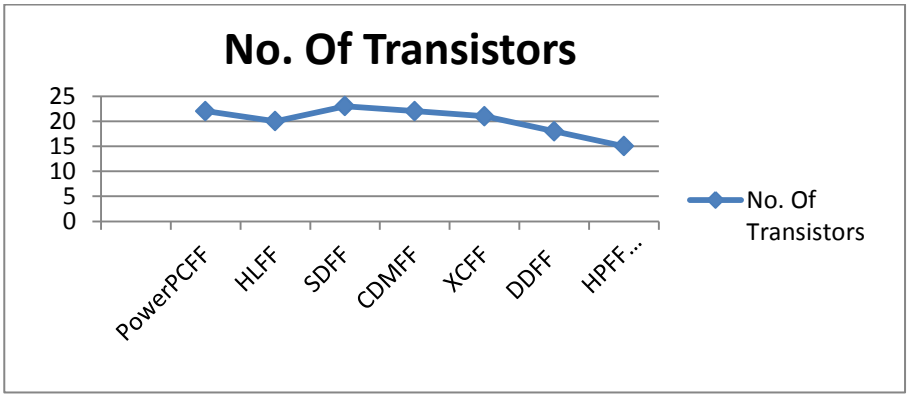
Fig. 2 Schematic of proposed design (a) HPFF (b) HPFF-ELM

IV. PERFORMANCE ANALYSIS

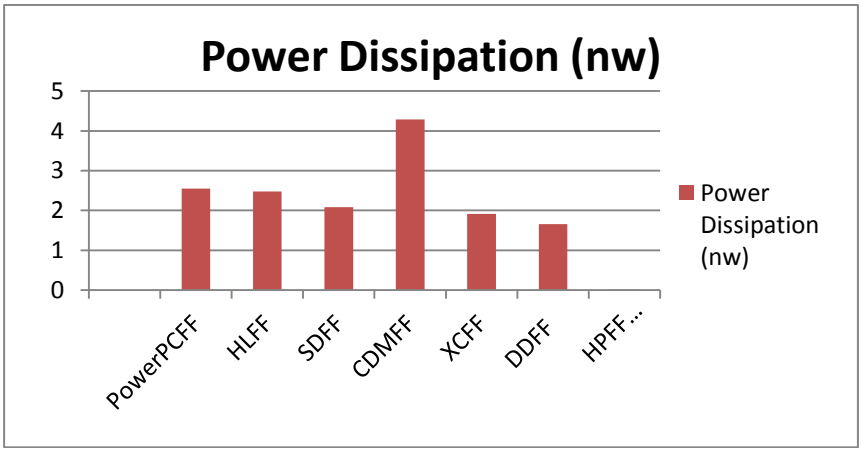
To highlight the advantages of the various designs, the proposed HPFF and HPFF-ELM architectures are compared with state-of-the-art designs. Features like number of transistors, power dissipation, D-to-Q delay, layout area and power-delay-product (PDP) are compared. Table I depicts the performance comparison of various flip-flop designs and Fig. 3 shows the performance comparison chart. From the Table 1, the HPFF consists of less number of transistors by using transmission gate instead of back-to-back inverters in the previous XCFF and DDFF architectures. Thus the layout area and delay consumed by the design is reduced. The power dissipation produced by the proposed HPFF is reduced from nano-watts(nW) to pico-watts(pW). Fig. 3(a) shows comparison of number of transistors with various flip-flop designs and Fig. 3(b) shows the comparison of power dissipation with state-of-the-art designs.

TABLE I PERFORMANCE COMPARISON OF PROPOSED HPFF DESIGN

Flipflop Design	No. of Transistors	Total Layout Area (μm^2)	Power Dissipation (nW)	D-Q Delay (ns)	PDP(fJ)
PowerPCFF	22	933.37	2.547	49.68	0.126
HLFF	20	1147.55	2.476	99.58	0.246
SDFF	23	856.19	2.088	50.55	0.104
CDMFF	22	519.65	4.290	301	0.0001
XCFF	21	603.58	1.919	50	0.095
DDFF	18	421.15	1.655	50.65	0.082
HPFF(proposed)	15	119.96	0.00643	50.33	0.000325



(a)



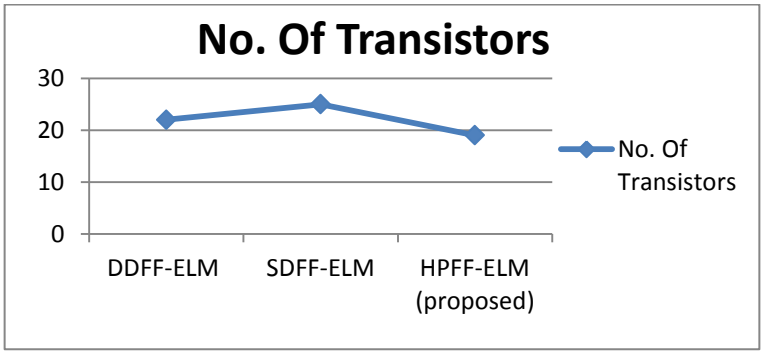
(b)

Fig. 3 Performance comparison charts of proposed HPFF design (a) No. of transistors vs flip-flop designs (b) Power dissipation vs flip-flop designs

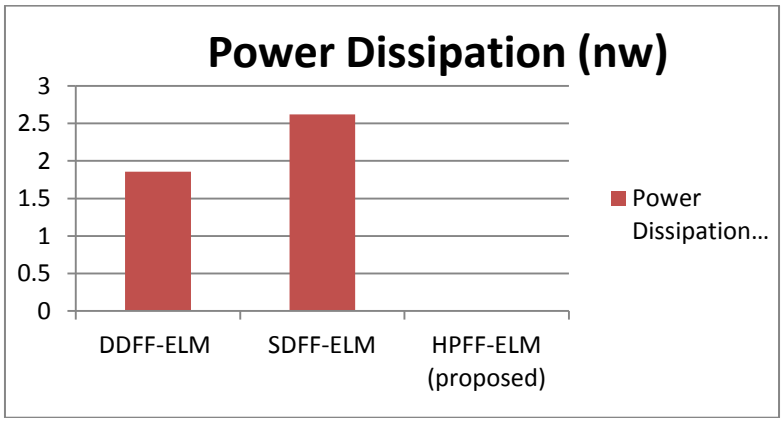
The proposed HPFF-ELM design has the ability to incorporate logic functions into the flip-flop. From the Table II, the performance comparison of embedded logic module with three flip-flop designs are compared. The number of transistors used by HPFF-ELM is very less when compared with DDFF-ELM and SDFF-ELM. Thus the layout area and the delay are also reduced. The power dissipation produced after embedding logic functions is decreased dramatically. Fig. 4 shows the performance comparison charts for the number of transistors in Fig. 4(a) and power dissipation in Fig. 4(b). This shows a clear comparison with the existing state-of-the-art. From the Table III, the performance of embedding various logic functions like AND, OR and MULTIPLEXER are compared. All the logic functions discussed here produces the similar power dissipation and almost equal number of transistors. The layout of the proposed HPFF and HPFF-ELM is shown in Fig. 5(a) Fig. 5(b) respectively.

TABLE II PERFORMANCE COMPARISON OF PROPOSED HPFF-ELM DESIGN

Flipflop Design	No. Of Transistors	Total Layout Area (μm^2)	Power Dissipation (nW)	D-Q Delay (ns)	PDP(fJ)
DDFF-ELM	22	488.47	1.856	100.02	0.092
SDFF-ELM	25	621.10	2.618	50.82	0.130
HPFF-ELM (proposed)	19	194.25	0.00668	50.55	0.000337



(a)

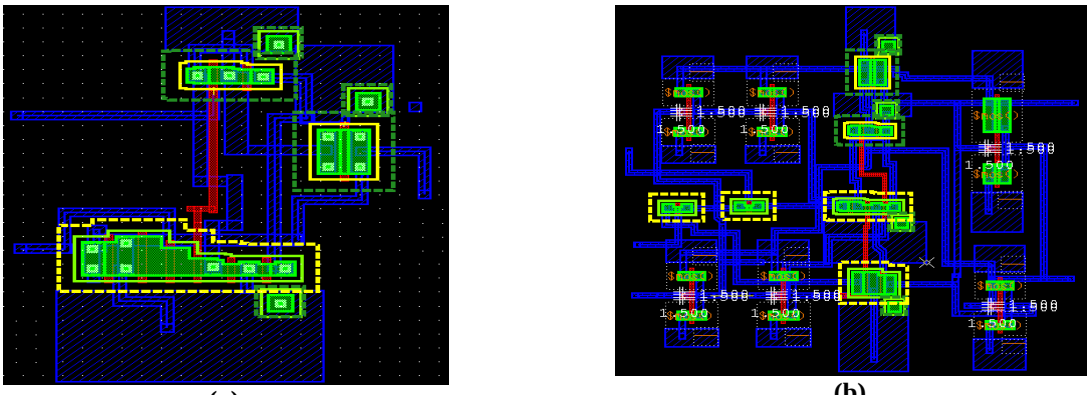


(b)

Fig. 4 Performance comparison charts of HPFF-ELM (a) No.of transistors vs flip-flop design (b) Power dissipation vs flip-flop designs

TABLE III PERFORMANCE COMPARISON OF VARIOUS LOGIC FUNCTIONS IN HPFF-ELM

Embedded logic function	No. Of transistors	Total layout area (μm^2)	Power dissipation (pW)	Delay (ns)
AND	19	194.25	6.683	50.57
OR	19	194.15	6.683	50.57
MULTIPLEXER	21	195.13	6.683	100.02



(a) **(b)**

Fig. 5 Layout of proposed design (a) HPFF (b) HPFF-ELM (incorporating AND logic)

V. CONCLUSION

A low power HPFF and a novel HPFF-ELM were proposed based on transmission gate scheme. The proposed HPFF eliminates the redundant power dissipation present in the XCFF and DDFF.A comparison of the proposed flip-flop with the conventional flip-flops showed that it exhibits lower power dissipation along with comparable speed performances. By eliminating the charge sharing, the revised structure of the proposed flip-flop, HPFF-ELM, is capable of efficiently incorporating complex logic into the flip-flop which reduces the pipeline overhead. It was proven that the proposed architectures are well suited for modern high performance designs where area, delay-overhead, and power dissipation are of major concern.

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