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Study of Design and Analysis of Low-Power 10-Transistor Full Adders Using Novel XOR–XNOR Gates

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***Abstract**: Full adders are vital components in applications such as digital signal processors (DSP) architectures and microprocessors. In this paper, we propose a technique to build a total of 41 new 10-transistor FA using novel XOR and XNOR gates in combination with existing ones.We have done over ten thousand HSPICE simulation runs of the entire the different adders in different input patterns, frequencies, and load capacitances. Almost all those new adders consume less power in high frequencies, while 3 new adders consistently use on average 10% less power and have higher speed compared with the previous Ten-transistor full adder and the conventional 28-T CMOS adder. One draw back of the novel adders is the threshold-voltage loss of the pass transistors.*

***Index Terms:** Arithmetic circuit, F.A., low power, very large-scale integration (VLSI), XOR–XNOR.*

I. INTRODUCTION

THE EXPLOSIVE growth in laptop, portable systems, and cellular networks has intensified the examine efforts in low-power microelectronics. Today, there is an ever increasing no. of portable applications requiring low power and high throughput circuits. Therefore, low-power design has become a major design consideration [2], [4], [6].

The adder is one of the most necessary components of a processor, as it is used in the automatic logic unit (ALU), in the floating-point unit, and for address generation in case of cache or memory access [2]. The full adder performance would affect the system as a whole. A variety of full adders using static or energetic logic styles have been reported in the literature [2]–[8]. In total, we have found 34 different full adder implementations, as indicated in [9]. The conventional adder uses 28 transistors implemented in CMOS technique. A new full adder called static energy-recovery full-adder (SERF) uses only 10 transistors, which has the least number of transistors and has reported to be the best in power consumption, according to [2]

Many low-power adders apply circuit level techniques using various pass transistors, such as the SERF [2]. Compared to the complementary static CMOSadders, such low-power adders have the problem of threshold loss, i.e., the logic value 1 is not the value of and the logic value 0 may not be the value of 0 vol. This kind of threshold-loss logic gates may not be used as widely as the complementary static CMOS gates. However, they are positively useful in building up larger circuits such as multiple- bit input adders and multipliers. One such established application is the Manchester carry-look ahead chain (MCC) [10] where pass transistors are used to generate carry functions and all pass transistors suffer the threshold-loss problem, yet the final adder circuit functions correctly as reported in [10].

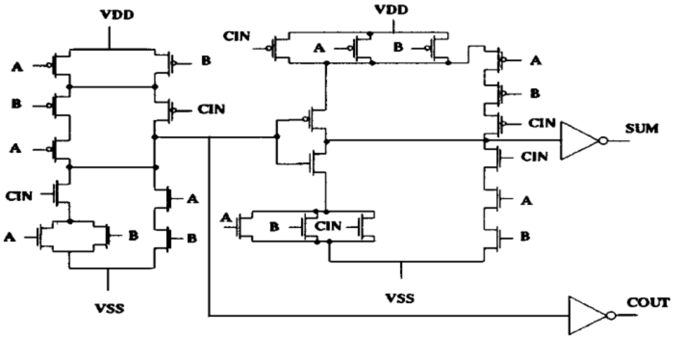


Fig. 1. 28-transistor CMOS adder schematic.

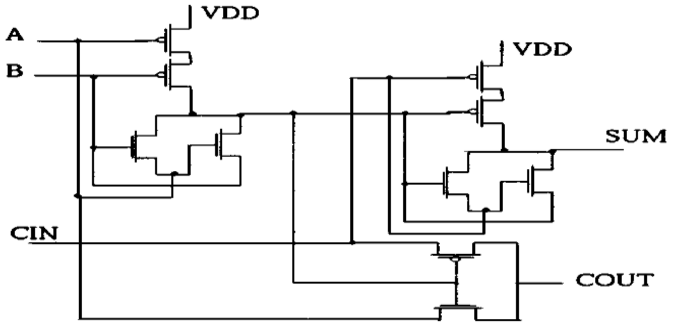
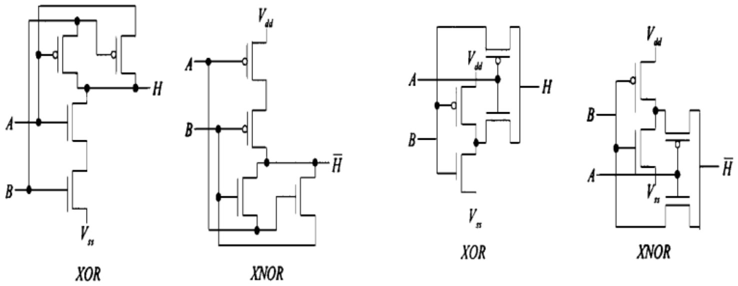


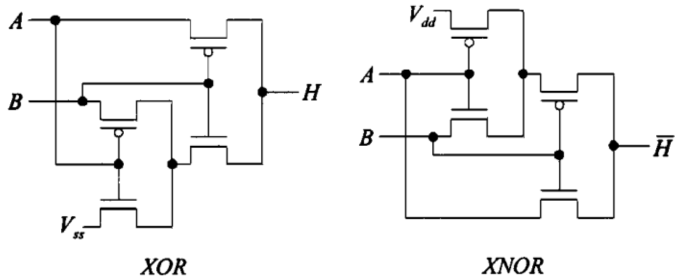
Fig. 2. SERF adder.

In this paper, we propose a systematic approach to designing many 10-transistor full adders. Our new adders also have the threshold-loss problem; however, the adders are useful in bigger circuits such as multipliers despite the threshold-loss problem. Using a novel set of XOR–XNOR gates in combination



with existing ones, a total of 41 new 1-bit full-adders are created. We have conducted over 10 000 HSPICE simulation runs of all the different adders in dissimilar input patterns, frequencies, and loading conditions. The reason to do these many simulations is to give a better confidence to how the new adders would perform under all the possible practical applications. Of course we can never cover all the possible practical cases, since no one can do so due to the fast change in the circuit and technology areas. Almost all those new adders show low-power consumption in high frequencies. In particular, three new adders consistently consume on average 10% less power and have higher speed compared with the previous 10-transistor full adder and the conventional 28-transistor CMOS adder.

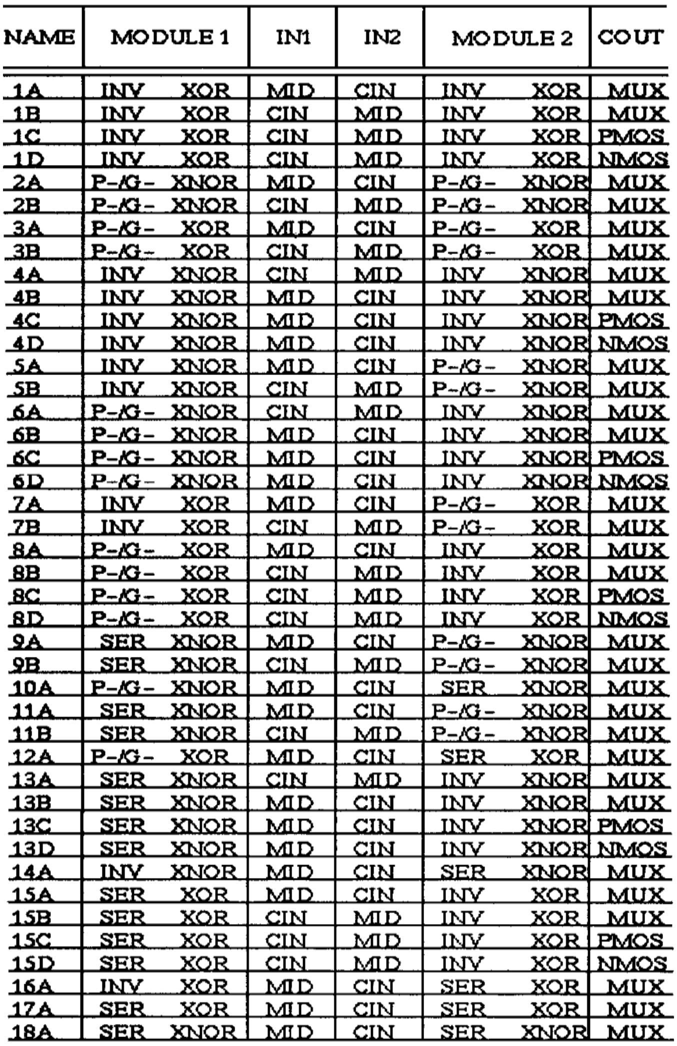
The rest of the paper is organized as follows: In Section II we briefly describe the previous work in literature. In Section III we propose the new adders. In Section IV we present the simulation methodology and simulation results. In Section V, we draw the conclusions.



II. Previous Work

The addition of 2 A and B with Cin yields a SUM and A Cout bit. The integer equivalent of this relation is shown by the (2) and (3) or (4)–(6)

TABLE I
DESCRIPTIONS OF ALL ADDERS



NAME	MODULE 1	IN1	IN2	MODULE 2	COUT
1A	INV XOR	MID	CIN	INV XOR	MUX
1B	INV XOR	CIN	MID	INV XOR	MUX
1C	INV XOR	CIN	MID	INV XOR	PMOS
1D	INV XOR	CIN	MID	INV XOR	NMOS
2A	P-/G- XNOR	MID	CIN	P-/G- XNOR	MUX
2B	P-/G- XNOR	CIN	MID	P-/G- XNOR	MUX
3A	P-/G- XOR	MID	CIN	P-/G- XOR	MUX
3B	P-/G- XOR	CIN	MID	P-/G- XOR	MUX
4A	INV XNOR	CIN	MID	INV XNOR	MUX
4B	INV XNOR	MID	CIN	INV XNOR	MUX
4C	INV XNOR	MID	CIN	INV XNOR	PMOS
4D	INV XNOR	MID	CIN	INV XNOR	NMOS
5A	INV XNOR	MID	CIN	P-/G- XNOR	MUX
5B	INV XNOR	CIN	MID	P-/G- XNOR	MUX
6A	P-/G- XNOR	CIN	MID	INV XNOR	MUX
6B	P-/G- XNOR	MID	CIN	INV XNOR	MUX
6C	P-/G- XNOR	MID	CIN	INV XNOR	PMOS
6D	P-/G- XNOR	MID	CIN	INV XNOR	NMOS
7A	INV XOR	MID	CIN	P-/G- XOR	MUX
7B	INV XOR	CIN	MID	P-/G- XOR	MUX
8A	P-/G- XOR	MID	CIN	INV XOR	MUX
8B	P-/G- XOR	CIN	MID	INV XOR	MUX
8C	P-/G- XOR	CIN	MID	INV XOR	PMOS
8D	P-/G- XOR	CIN	MID	INV XOR	NMOS
9A	SER XNOR	MID	CIN	P-/G- XNOR	MUX
9B	SER XNOR	CIN	MID	P-/G- XNOR	MUX
10A	P-/G- XNOR	MID	CIN	SER XNOR	MUX
11A	SER XNOR	MID	CIN	P-/G- XNOR	MUX
11B	SER XNOR	CIN	MID	P-/G- XNOR	MUX
12A	P-/G- XOR	MID	CIN	SER XOR	MUX
13A	SER XNOR	CIN	MID	INV XNOR	MUX
13B	SER XNOR	MID	CIN	INV XNOR	MUX
13C	SER XNOR	MID	CIN	INV XNOR	PMOS
13D	SER XNOR	MID	CIN	INV XNOR	NMOS
14A	INV XNOR	MID	CIN	SER XNOR	MUX
15A	SER XOR	MID	CIN	INV XOR	MUX
15B	SER XOR	CIN	MID	INV XOR	MUX
15C	SER XOR	CIN	MID	INV XOR	PMOS
15D	SER XOR	CIN	MID	INV XOR	NMOS
16A	INV XOR	MID	CIN	SER XOR	MUX
17A	SER XOR	MID	CIN	SER XOR	MUX
18A	SER XNOR	MID	CIN	SER XNOR	MUX

A+B+Cin = 2*Cout+SUM………………..(1)
Cout = (A∧B)∨((A∨B)∧Cin)………………(2)
SUM = (A∧B∧Cin)∨(A∨B∨Cin)∧(Cout')……….(3)
SUM = A exor B exor Cin……………….(4)
SUM = A exnor B exnor Cin………………(5)
Cout = (A∧(A exnor B)) ∨ (Cin ∧(A exor B))…….(6)

Many full adder designs can be found in the literature. In [3], a 28-transistor adder shown in Fig. 1 implements (2) and (3) using complementary CMOS design. The SERF adder, shown in Fig. 2, implements (5) and (6) using only ten transistors.

Our newly proposed adders also implement (4) or (5) and (6), using XOR–XNOR gates as the basic building blocks. Several designs of XOR–XNOR have been proposed in the literature. At the time of this publication, the smallest XOR–XNOR gates have four transistors. Two of such XOR–XNOR gates are shown in Fig. 3(a) and (b) [1].

III. EW DESIGN

a. *Novel XOR and XNOR Gates*

Before we present the new adders, we first propose a new XOR gate, shown in Fig. 4. It resembles the inverter-based XOR shown in Fig. 3(b) but the difference is that the VDD connection in the inverter-based XOR is connected to the input A. Because the new XOR gate has no power supply, it is called *Powerless*

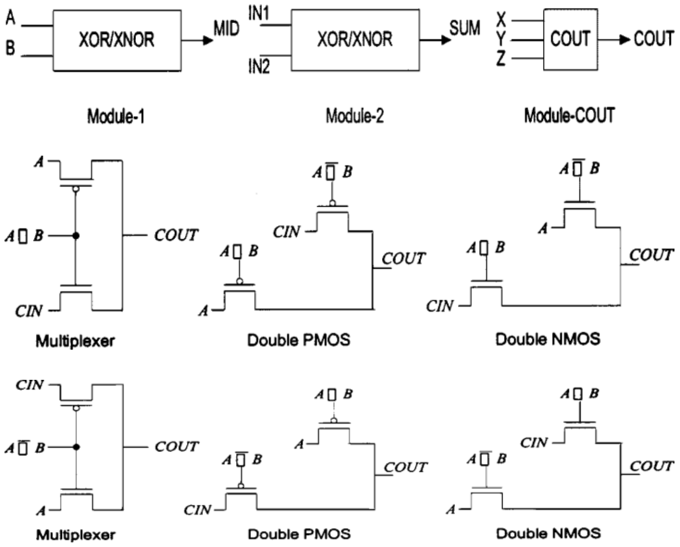
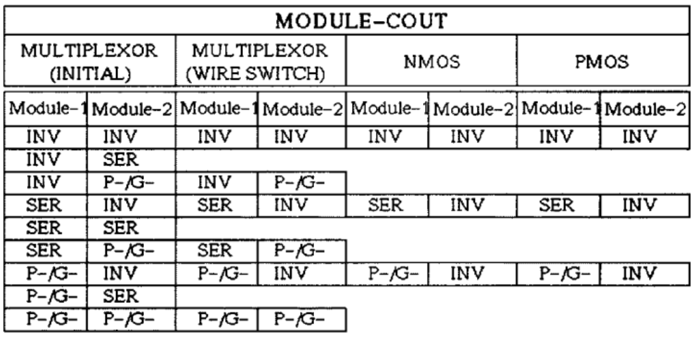


Fig. 6. Choices for module-COUT. (a) Module-COUT for module-1 = module-2 = XOR. (b) Module-COUT for module-1 = module-2 = XNOR.

B. Full Adder

We use three modules, shown in Fig. 5, to implement the full adder based on (4) or (5) and (6). Module-1 and module-2 can be XOR or XNOR gates and module- can be a multiplexer, double PMOS or double NMOS transistors. The sum is generated by cascading module-1 and module-2. This implements (4) or (5). The function is implemented by module-1 and module- according to (6). If module-1 and module-2 are XOR gates, module- can have one of the configurations shown in Fig. 6(a). If module-1 and module-2 are XNOR gates, the choices for the moduleare shown in Fig. 6(b). The first 18 full adders use the multiplexer as module- Modules 1 and 2 either have to be both XOR or both XNOR. They can be inverter-based XOR–XNOR, static energy-recovery XOR–XNOR or P-/G-XOR–XNOR. For example, with an inverter-based XOR module-1, module-2 can be inverter-based XOR, static energy-recovery XOR or P-/G-XOR. There are three possible choices for module-1 and three possible choices for module-2. This gives nine combinations for the case when modules 1 and 2 are XOR and nine more when they are XNOR. They are referred to as the *initial* adder subset shown in Fig. 7. They are also listed in Table I as all the adders whose names end with the letter "A" (1A–18A). A new adder subset, called the *wire switch*, is derived from the *initial* adder subset by exchanging the two inputs to module-2. An adder from the *wire switch* adder subset has the



MODULE-COUT							
MULTIPLEXOR (INITIAL)		MULTIPLEXOR (WIRE SWITCH)		NMOS		PMOS	
Module-1	Module-2	Module-1	Module-2	Module-1	Module-2	Module-1	Module-2
INV	INV	INV	INV	INV	INV	INV	INV
INV	SER						
INV	P-/G-	INV	P-/G-				
SER	INV	SER	INV	SER	INV	SER	INV
SER	SER						
SER	P-/G-	SER	P-/G-				
P-/G-	INV	P-/G-	INV	P-/G-	INV	P-/G-	INV
P-/G-	SER						
P-/G-	P-/G-	P-/G-	P-/G-				

Fig. 7. Adder variations.

same three modules as its corresponding adder from the *initial* adder subset. Each *initial* adder produces a *wire switch* adder. There are six cases when module-2 is a static energy-recovery XOR–XNOR (Fig. 7). Static energy-recovery XOR–XNOR gates are symmetric and thus, a wiring change does not alter their performance. These six adders are, therefore, identical to their *initial* adder subset counterpart and are not counted. The *wire switch* adder subset consists of 12 adders (18 minus 6 that have static energy-recovery XOR–XNOR). The *wire switch* adders are shown in Fig. 7 and are listed in Table I as adders whose names end with the letter "B." Using the *wire switch* adder subset, we can obtain more variations by replacing module Cout- while keeping modules1 and 2. Module Cout- is replaced by one of the choices shown in Fig. 6. These choices for module- Cout require both A exor B and A exnor B .With the available XOR–XNOR gates, the only way is to have an inverter-based XOR–XNOR as module-2. The first signal to module- Cout is taken from the output of

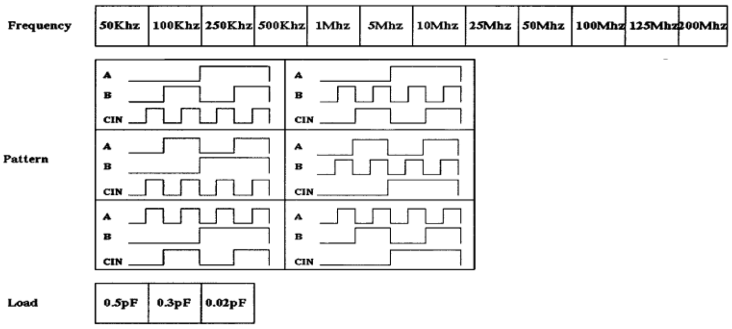


Fig. 8. Simulation setups: input patterns and loading conditions.

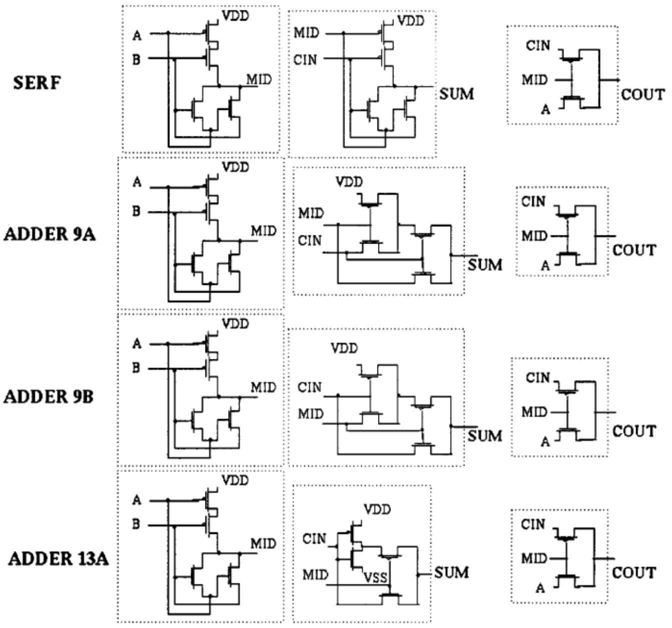


Fig. 9. Construction modules to build various adders.

module-1 and its complement is taken after the CMOS inverter of module-2. There are six adders that use the inverter-based XOR–XNOR as module-2. Thus, there are six new adders that use the double PMOS and six more that use the double NMOS as their module-Cout . They are listed in Table I as adders whose names end with the letter "C" for PMOS and "D" for NMOS.

The above process creates a total of 42 adders which are listed in Table I. One of the adders generated through this process is the SERF adder, listed as 18A. Hence, there are 41 different new full adders. The columns *IN1* and *IN2* in Table I show which wires are connected to the two inputs of module-2. The Cout column shows the selected module- Cout.

IV. Experiment Description And The Results

We have performed experiments on the 41 newly designed 1-bit full adders along with the SERF adder and the conventional CMOS adder at the schematic level. The transistors have a channel length of 0.6 m and a channel width of 2.4 m using 3.3 V logic. Each circuit is simulated with the same testing conditions. The netlists of those adders are extracted and simulated using HSPICE on an Ultra-SPARC 2 machine.

A circuit responds differently to different input patterns. So we use six input patterns to cover all input combinations. Those patterns are shown in Fig. 8. Each pattern is simulated 12 times using frequencies ranging from 50 kHz to 200 MHz. Three different capacitor values (0.5, 0.3, and 0.02 pF) are used to load the outputs.

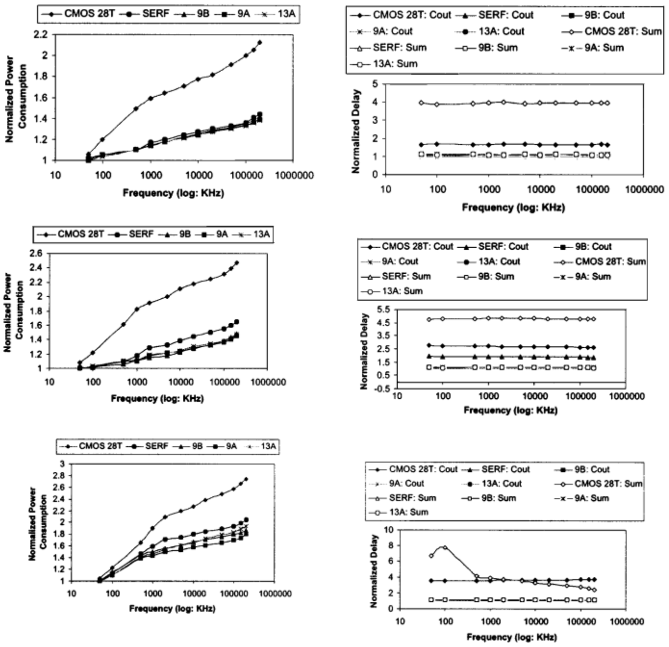


Fig. 10. Comparison of power consumption and critical delay.

Thus, for each adder, 216 HSPICE simulation runs (6 patterns * 12 frequencies * 3 loads) are made. This gives a total of 9288 simulation runs for the preliminary part of the experiment (43 adders * 216 simulations/adder). The simulation setup is shown in Fig. 8. For every pattern, frequency and load combination, we have 1 SUM power measurement, 1 Cout delay measurement and 1 delay measurement. For a given load, input pattern and frequency, four complete pattern cycles are simulated. All input signals have a rise time and a fall time of 500 ps. This is a suitable arrangement for the adopted technology in this study. For finer technologies, we shall expect lower rise and fall times. The simulation results shall be very similar to what is reported to our simulation runs. During a simulation session, a single power measurement is taken by averaging the instantaneous power over a period of three pattern cycles starting from the beginning of the second cycle to the end of the fourth cycle. The measurement does not include the first cycle to avoid transient glitches. The average power of an adder is the average value of the six different pattern power measurements. Thus, for a specific load, an adder has 12 different average power measurements, accounting for each of the 12 input frequencies.

Propagation delay is the time between the fastest input signal and the output signal. We use the first rising edge of all signals at the beginning of the second pattern cycle. The critical propagation delay is the value of the highest delay measured for the Cout and SUM output for the six different patterns with a specific load and frequency.

After the simulations, three of the new full adders stand out as being the best: adder 9A, adder 9B, and adder 13A, shown in Fig. 9. Along with the SERF adder and the CMOS adder (Fig. 1), these adders have been simulated under 11 new loading conditions varying from 0.01 to 0.5 pF. Each load simulation is done with six different patterns at 12 different frequencies. This gives an additional 3960 simulation runs (72 simulations/load * 11 loads/adder * 5 adders), in addition to the previous 9288 simulations. In total, there are 13 248 simulation runs.

In power consumption, adder 9B consistently has better power consumption than the SERF adder. It consumes up to 12% less power. Adder 9A and adder 13A have better power consumption except when the load is 0.01 pF. Adder 9A consumes up to 20% less power whereas adder 13A consumes up to 10% less.

The CMOS adder dissipates more power than the other adders. The left-hand side of Fig. 10 shows the power measurement for loads of 0.01, 0.25, and 0.5 pF, respectively, starting from the top.

Adders 13A and 9B have better critical delay than the SERF adder in all loading condition. They have up to 93% better speed than the SERF adder. The right-hand side of Fig. 10 shows the propagation delay at key loading conditions: 0.02 pF at the top, 0.15 pF at the middle, and 0.45 pF at the bottom.

As mentioned earlier, the performance of many larger circuits are strongly dependent on the performance of the full adder circuits that have been used. The new 10-transistor adder circuits presented in this study, are good candidates to build these large systems, such as high performance multipliers with low power consumption. The small area of these adders can also significantly reduce the area of the systems built upon them.

V. Conclusions

In this paper, we have presented a systematic approach to construct full adders using only ten transistors. In total we can construct 42 ten-transistor adders of which 41 are new. Based on our extensive simulations, we conclude that three new adders consume on average 10% less power and have 90% higher speed compared to the previous ten-transistor adder.

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