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Design of Low Power 4-bit ALU Using Adiabatic Logic

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Abstract: *This paper presents the implementation of a 4-bit Arithmetic Logic Unit (ALU) using Complementary Energy Path Adiabatic Logic (CEPAL). This static adiabatic logic has proved its advantage through the minimization of the 1/2CVdd2 energy dissipation occurring every cycle. Firstly, the performance characteristics of CEPAL 4-to-1 multiplexer and full adder are compared against the conventional static CMOS logic counterpart to identify its adiabatic power advantage. Finally, A 4-bit Arithmetic Logic Unit (ALU) is implemented with both the technologies and comparisons have been made. The analysis is carried out using the industry standard EDA design environment using 250 nm technology libraries from Tanner. The results prove that the CEPAL 4-bit ALU is 55% more power efficient than the CMOS 4-bit ALU at 100MHz and at 2.5V operating voltage.*

Keywords*: Low Power; Static Adiabatic logic; Complementary Energy Path Adiabatic Logic (CEPAL); Power Clock(PC); Full Adder; Arithmetic Logic Unit (ALU); Multiplexer(MUX); Very Large Scale Integration(VLSI)*

I. INTRODUCTION

With the advancement in technology it has become possible to scale down the electronics involved in numerous applications. The advantage being that the technology becomes more portable and its applications increase, the tradeoff being that the power levels utilized at that scaled down level induces other effects on the circuit, i.e the power dissipation as heat increases, the stability decreases, the performance decreases and so on. Numerous techniques have been suggested over the years to overcome these problems. Adiabatic logic is a promising alternative to CMOS in reducing the power dissipation without having to compromise with noise immunity and driving ability. Many adiabatic Logics have been presented in the literature [4]-[17] over the years, but the fundamental principle remains the same.

Energy recovery techniques and adiabatic logic topologies minimize energy dissipation by maintaining low voltage drop across conducting devices at all times. The undissipated energies related to the charges are recycled and is not dissipated as heat. Many of the energy recovery techniques have been presented in the literature. [1]- [3]

Most of the adiabatic circuits have dynamic circuit properties and have high switching activity. This property makes the implementation of this logic on larger circuits difficult. In addition, the requirements of multiphase and multi clock also make them unfavorable in terms of design complexity and area. [20,21]

Quasi static energy recovery logic (QSERL) shown in the literature [18,19] has been known to overcome the drawbacks of these dynamic adiabatic logics. Its simplicity, static nature and use of only two complementary clocks make it easy to design and apply in complex circuits than the dynamic circuits which use triangular or trapezoidal clocking scheme. In spite of these advantages, this logic suffers from the output floating node associated with alternate hold phases in operation. Although this floating node can be avoided by adding clocked feedback keeper, there is still significant power loss and the added area would restrict its application. [20,21]

Complementary Energy Path Adiabatic Logic (CEPAL) is proposed in this paper. Motivated by the design constrains of the QSERL, CEPAL is designed which inherits all the advantages of the static logic QSERL and also eliminates the hold phases of the QSERL thus increasing its robustness and throughput. [20,21] This logic presents an effective alternative to conventional CMOS for the realization of low power electronics. The performance of CEPAL has been analyzed using excessive experiments. This paper presents the design and experimental evaluation of a 4- bit ALU and a 4-to-1 multiplexer. In addition to this, our paper contains the simultaneous comparisons of power consumption and transistor count of both CMOS and CEPAL technology. It was found that the CEPAL ALU was 55% more power efficient compared to the CMOS ALU.

II. COMPLEMENTARY ENERGY PATH ADIABATIC LOGIC

The Structure and working of the CEPAL is shown in figure 1. [20,21] It consists of a pair of charging and discharging transistors. A pull up network and a pull down network.This logic makes use of two sinusoidal power clocks, PC and PCbar, which are complementary to each other. Let us understand the working of this

structure. Assuming the initial Vout is low, with the P- network on and the N-network off, Vout follows the power clock PC or PCbar which ever swings to the high level. Since the power clock is sinusoid in nature it ramps down which makes the Vout to follow it and generating a floating node. This situation is however avoided by the complementary clock which swings high, thus eliminating this weak high signal and also eliminating the hold state seen in two phase clock operated circuits. Similarly the weak low signal is also eliminated by the complementary clock. [22]-[24]

Let us assume the other case in which Vout is high with the P-network on and the N-network is off. The Vout remains high unless and until there is a change in the input. CEPAL has two more diodes in comparison to quasi static energy recovery logic (QSERL) shown in the literature [18,19], but power dissipation due to these additional diodes is not very large as there is only one charging or discharging diodes turned on at an instant of time. Thus QSERL and CEPAL circuits have similar power consumption, however considerable improvements in area and power overheads can be achieved in CEPAL circuits because the keeper is used in QSERL circuits to avoid erroneous operation during hold phase. [20,21]

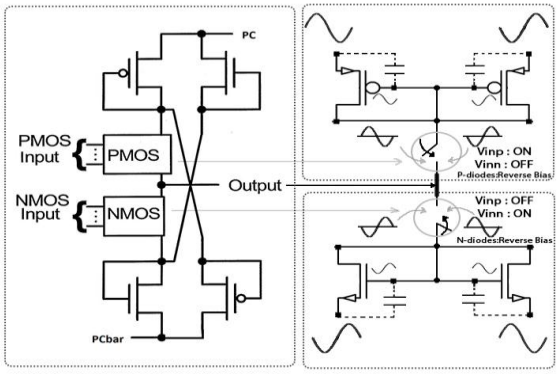


Figure 1: Complementary Energy Path Adiabatic Logic

III. DESIGN OF CEPAL 4-TO-1 MUX AND FULL ADDER

A. 4-to-1 Mux

The experimental work consists of simulating the circuit shown in Figure. 2. A MUX is a device used to handle multiple signals by selecting one of several input signals and forwarding it into a single line. This MUX is implemented using Tanner EDA with all the transistors of equal sizes of W/L=0.35µm/0.25µm. The supply voltage and power clock frequency (PC) are 2.5V and 100MHz respectively.

The number of transistors and the average power of the CMOS and the CEPAL for the MUX are shown in Table 1.

Table 1: MUX Transistor count & Power Comparison

Logic	P-MOS	N-MOS	Total Transistors	Average Power
CMOS	13	13	26	5.980uW
CEPAL	17	17	34	1.768uW

Though there is an increase in the number of transistors in the CEPAL technology, significant decrease in power can be seen. The CEPAL MUX is 70% more efficient compared to its CMOS counterpart.

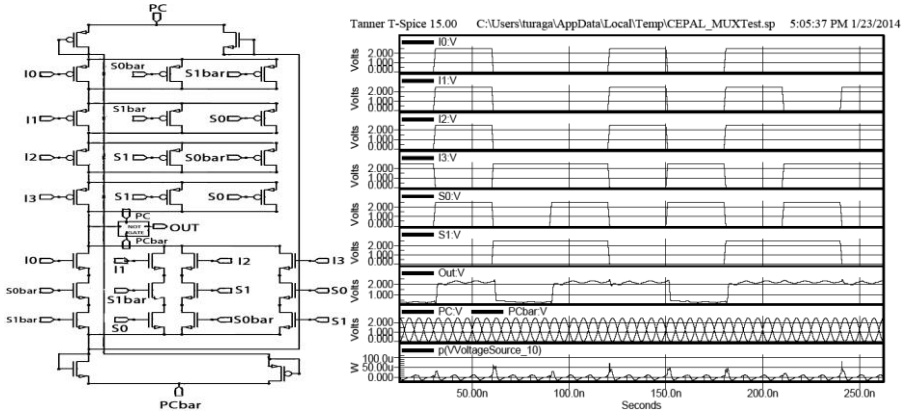


Figure 2: CEPAL 4-to-1 Multiplexer

Figure 2 also shows the output waveforms of the CEPAL MUX. PC and PCbar are the two complementary power clock. The plot p(VVoltageSource_10) shows the power consumption of the power clock. The average of p(VVoltageSource_10)is given in table 1.

B. Full Adder

The Full Adder accepts three one bit inputs and generates a sum and carry output. The sum is generated by the XOR operation of all the inputs. This Full Adder is implemented here using the CEPAL technology. Figure 3 shows the schematic of the Full Adder which consists of forty five pMOS and forty five nMOS transistors. The number of transistors and the average power of the CMOS and the CEPAL for the Full Adder are shown in Table 2.

Table 2: Full Adder Transistor count & Power Comparison

Logic	P-MOS	N-MOS	Total Transistors	Average Power
CMOS	21	21	42	9.922uW
CEPAL	45	45	90	2.607uW

The CEPAL Full Adder is found to be 73% power efficient compared to CMOS technology this added advantage is a well worth tradeoff for the increased transistor count. Figure 3 shows the output waveforms of the CEPAL Full Adder. The logic '1' is 2.24V and logic '0' is 0.31V. Plot PC and PCbar show the power clock given. The plot p(VVoltageSource_10) show the power consumption of the powerclock.

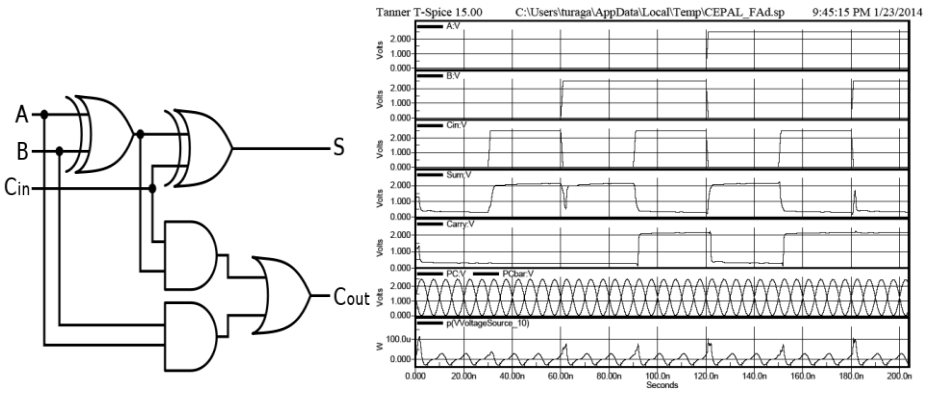
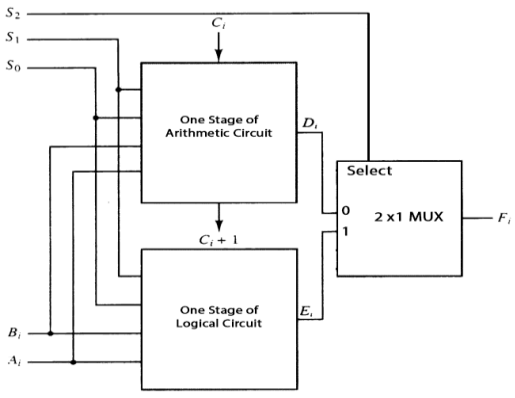


Figure 3: CEPAL Full Adder

IV. STRUCTURE AND DESIGN OF CEPAL MUX AND 4-BIT ALU

Arithmetic Logic Unit is a common operational unit with number of storage registers connected to it, using which it performs micro operations. To perform a micro operation, the contents of specified registers are placed in the inputs of the common ALU. The ALU performs an operation and the result of the operation is then transferred to a destination register. The ALU is a combinational circuit so that the entire registers transfer operation from the source register through the ALU and the destination register can be performed during one clock pulse period.

The ALU used here is the CEPAL ALU shown below in figure 4. It consist of two components the arithmetic unit and the logical unit.



Operation select					
S_2	S_1	S_0	C_{in}	Operation	Function
0	0	0	0	$F = A$	Transfer A
0	0	0	1	$F = A + 1$	Increment A
0	0	1	0	$F = A + B$	Addition
0	0	1	1	$F = A + B + 1$	Add with carry
0	1	0	0	$F = A + \overline{B}$	Subtract with borrow
0	1	0	1	$F = A + \overline{B} + 1$	Subtraction
0	1	1	0	$F = A - 1$	Decrement A
0	1	1	1	$F = A$	Transfer A
1	0	0	×	$F = A \wedge B$	AND
1	0	1	×	$F = A \vee B$	OR
1	1	0	×	$F = A \oplus B$	XOR
1	1	1	×	$F = \overline{A}$	Complement A

Figure 4: Structure of an ALU and its Truth Table

A. The Arithmetic Unit

The arithmetic operations in the table can be implemented in one composite arithmetic circuit. The basic component of an arithmetic circuit is a full adder. By controlling the data input to the adder it is possible to obtain different types of arithmetic operations. The diagram of the 4-bit arithmetic circuit is shown in figure 5. It has four full adder circuits that constitute the 4 bit adder and 4 multiplexers for choosing multiple operations. There are two 4 bit inputs A and B and 4 bit output D.

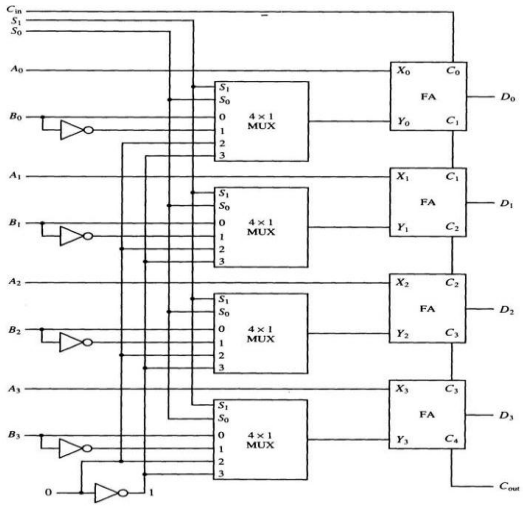


Figure 5: Schematic of 4-bit Arithmetic Unit

B. Logical Unit

Logic micro operations specify binary operations for strings of bits stored in registers. These operations consider each bit of registers separately and treat them as binary variables. Figure 6 shows one stage of a circuit that generates the four basic logic micro operations. It consists of 4 gates and a multiplexer each of the four logic operations is generated through a gate that performs the required logic. The outputs of the gates are applied to the data inputs of the multiplexer. The two selection inputs S1 and S2 choose one of the data inputs of the multiplexers and direct it values to the output. Figure 8 shows one typical stage of logical unit.

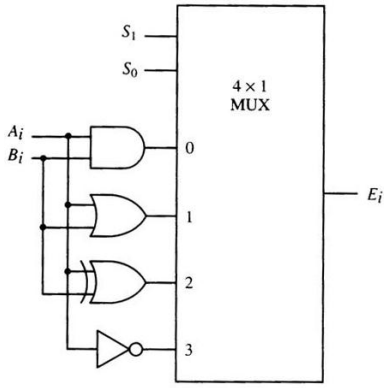


Figure 7: Schematic of 1-bit Logic Unit

V. RESULTS AND DISCUSSIONS

The adiabatic Arithmetic Logic Unit were implemented using 250nm technology of the Tanner EDA with a W/L = 0.35um/0.24um and at 2.5V operating voltage with power clock frequency at 100MHz. The simulation results of both CMOS and CEPAL are compared with the same logic implementation. The simulation environment was maintained the same to provide justified results.

Figure 8 shows the output waveforms of the CEPAL Arithematic and Logic unit. The output clearly follows the truth tabe shown in figure 4 for the input bit sequence given is A= "0011" and B= "1010" . The logic '1' is 2.24V and logic '0' is 0.18V. The plot p(VPC) show the power consumption of the power clock.

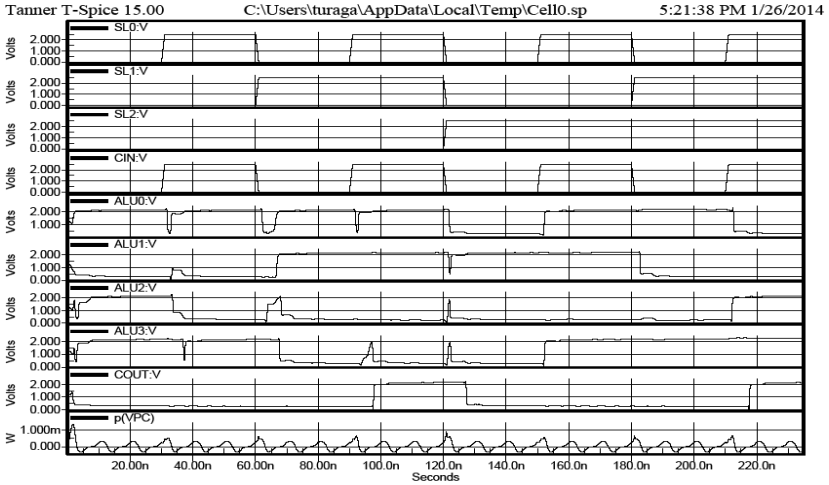


Figure 8: Output of CEPAL 4-bit ALU.

The number of transistors and the average power of the CMOS and the CEPAL 4-bit ALU are shown in Table 8.

Table 4: 4 bit ALU Transistor count & Power Comparison

Logic	P-MOS	N-MOS	Total Transistors	Average Power
CMOS	329	329	658	78.341uW
CEPAL	556	556	1112	35.723uW

VI. CONCLUSION

The results clearly show that the CEPAL circuits offer better power efficiency compared to its CMOS counterpart. Though there is an increase in transistor count, it's very low power consumption outweighs this drawback. The simulation results show that the CEPAL ALU is 55% more power efficient as compared to the CMOS ALU. CEPAL consumes significantly less power in contrast to CMOS in each and every case. CEPAL certainly does open many doors in design of low power VLSI circuits and is a promising alternative to the conventional CMOS in design of low power electronics. Its relatively high immunity to noise and increased throughput does facilitate its use in future electronics which is yet to come.

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