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III-V Mosfet as Advance Low Dimensional Transistor

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Abstract: *The workhorse of the present electronics industry, silicon MOSFET, is having a unique attribute; its logic characteristics improve as its dimensions are reduced. Without further reductions in operating voltage, future scaling may not be feasible. One possible solution is to introduce a new channel material in which charge carriers travel at a much higher velocity than in silicon and this would allow a reduction in voltage without a loss of performance. This factor has drowned the attention of research community around the world towards III–V compound semiconductors. No other family of materials currently being considered to replace the silicon channel in a MOSFET has such an impressive list of attributes. Today, III–V CMOS technology is a mainstream part of semiconductor research. Their future role has recently been recognized in the International Technology Roadmap for Semiconductors 7.The application of simulation tools in the development of new processes and novel device structures has become a worthwhile and an alternative to the experimental route. For all these tasks the technology computer-aided design (TCAD) was coined.*

I. Introduction

Driven by tremendous advances in lithography, the semiconductor industry has followed Moore's law by shrinking transistor dimensions continuously for the last 40 years. The big challenge going forward is that continued scaling of planar, silicon, CMOS transistors will be more and more difficult because of both fundamental limitations and practical considerations as the transistor dimensions approach ten nanometers. The issues at small gate lengths are many fold. First, transistor scaling increases the number of gates on a chip and the operating frequency. To prevent the chip from overheating, the power dissipation should be limited, which requires lowering the power supply voltage while maintaining the ability to deliver high on currents for each new generation of technology. Secondly, the drain bias decreases the energy barrier height between the source and channel in a transistor due to 2D electrostatics. Degraded short channel effects become more significant as the gate length gets shorter, and the increased off-state leakage has pushed the standby power to its practical limit. Thirdly, the accompanying scaled oxide thickness provides better gate control of the channel potential, but this inevitably increases the gate leakage and makes it very difficult to obtain both high on-currents and low off-currents at lowered supply voltage. Lastly, the parasitic resistance and capacitance have become comparable to, or even larger than the continuously decreasing intrinsic channel capacitance and resistance, which may provide a practical limit to scaling [1]. A 45 nm process based on high-k, metal gate, and strained silicon was introduced in 2007 [2]. With such technologies, scaling will continue to the 32 nm node and beyond [3].. Further improvements in transistor speed and performance may have to come from new channel materials. To address the scaling challenge, both industry and academia have been investigating alternative device architectures and materials, among which III-V compound semiconductor transistors stand out as promising candidates for future logic applications because their light effective masses lead to high electron mobilities and high on-currents, which should translate into high device performance at low supply voltage.

II. Compounds

The III–V compound semiconductors, such as GaAs, AlAs, InAs, InP and their ternary and quaternary alloys, combine elements in columns III and V of the periodic table. Some III–V compounds have unique optical and electronic properties. Their ability to efficiently emit and detect light means they are often used in lasers, light-emitting diodes and detectors for optical communications, instrumentation and sensing. A few, notably GaAs, InGaAs and InAs, exhibit outstanding electron transport properties. Transistors based on these materials are at the heart of many high-speed and high-frequency electronic systems6. In fact, there is a large and mature industry manufacturing.

III–V integrated circuits in great volumes for applications as diverse as smart phones, cellular base stations, fibre-optic systems, wireless local-area networks, satellite communications, radar, radioastronomy and defence systems. The recent widespread use of handheld devices and their enormous consumption of data has been a boon to the III–V integrated-circuit industry, which is now characterized by highly automated and rigorous large-scale manufacturing, relatively large-area wafers, sophisticated device and circuit design tools,

well-established device reliability, and a rich and competitive industrial ecosystem. No other family of materials currently being considered to replace the silicon channel in a MOSFET has such an impressive list of attributes.

MOSFET

The rationale for using III–V compounds

The case for III–V CMOS technology is often made by drawing attention to the extraordinary electron mobility of certain III–V compounds (Fig. 1). In InGaAs or InAs, the electron mobility is more than 10 times higher than in silicon at a comparable sheet density. The outstanding frequency response of III–V transistors is also frequently invoked. For example, current-gain and power-gain cutoff frequencies of InGaAs-based high-electron-mobility transistors (HEMTs) a well-established transistor design in its own right exceed 600 GHz and 1 THz, respectively8–10. Impressive as these attributes are, such arguments do not address what really matters for a logic transistor.A logic transistor operates as a switch that toggles between an 'on' state and an 'off' state. For fast switching, a high on current (*I*ON) is desired. To limit standby power consumption, the off current (*I*OFF) must be minimized. It is in terms of *I*ON and *I*OFF that the suitability of a transistor for logic should be assessed (for these and other definitions, see Fig. 2 in the Review by Colinge and colleagues1). In an NMOS transistor in saturation, *I*ON is determined by the product of the sheet electron concentration and the electron injection velocity, *v*inj, at the 'virtual source'11, the location on the channel that presents the highest energy barrier in the conduction band. This is the bottleneck to electron flow.We can learn about the injection velocity of future III–V transistors byexamining III–V HEMTs. In this regard, HEMTs provide an excellent model system to study issues of importance in future III–V MOSFETs12. Measurements in InGaAs and InAs HEMTs13 have revealed values for that approach 4 × 107 cm s–1 at 0.5 V (Fig. 2). This value of voltage has been selected to compare future technology options because it delivers a sizeable reduction in power dissipation from the present supply of 1 V. In the III–V HEMTs in Fig. 2, *v*inj is more than twice that of comparable silicon MOSFETs at less than half the voltage14. For devices shorter than about 50 nm, the injection velocity becomes independent of gate length. Monte Carlo simulations indicate that electron transport through the channel takes place in a ballistic fashion, that is, with almost no collisions15. In this instance, the injection velocity is determined by the band structure of the channel material, and *v*inj increases with InAs composition in the channel as a result of a lower electron effective mass13.Sheet carrier concentration also affects *I*ON. Concerns have been expressed about the limitation that a low effective mass

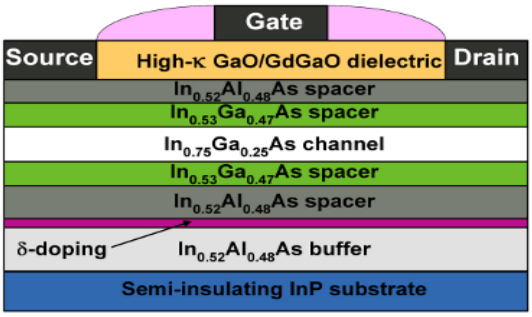

Fig3.structure of III-V MOSFET

imposes on the maximum sheet electron concentration that can be obtained16. Recent measurements in InGaAs and InAs HEMTs suggest that the electron effective mass is significantly greater than the bulk value17. This is explained by the strong non-parabolicity of the conduction band of these materials, coupled with electron quantization in the thin channel and biaxial compressive stress from lattice mismatch with the InP substrate.

InGaAs and InAs 'quantum-well' FETs with the potential to deliver outstanding *I*ON at a low supply voltage, *V*DD, something essential in future CMOS transistors.But *I*OFF is just as important as *I*ON. In quantum-well devices without source and drain junctions, such as HEMTs, *I*OFF is set by the subthreshold swing, *S*, which quantifies the sharpness of the drop of the drain current below threshold. In InAs and InGaAs HEMTs, the quantum nature of the channel effectively confines electrons and yields a steep subthreshold behaviour with respect to comparable silicon MOSFETs18. The thinner the channel, the closer the subthreshold swing approaches its ideal value of ~60 mV per decade (that is, the current increases by a factor of 10 for every 60-mV increase in gate voltage) at room temperature.

Co-integration of NMOS and PMOS transistors on silicon

Perhaps progress is most needed in the side-by-side integration of III–V NMOS and PMOS transistors on a silicon substrate. Economics dictates the use of silicon wafers for at least two reasons. First, a large wafer is essential to achieving the cost structure central to Moore's law. An additional consideration is the effective use of the tool base that will be in place when the new technology moves into advanced development. The fabrication of III–V heterostructures on silicon has been underinvestigation for some time. The interest was

fuelled by the integration of optical devices and CMOS logic circuits, multijunction solar cells, and the heterogeneous integration of CMOS circuitry and III–V electronic devices, among other applications. Nanometre-scale III–V CMOS transistors pose some unique requirements for heterogeneous integration. One is the need for a very thin buffer structure that converts the silicon lattice constant into the desired one. The thickness of the buffer layer matters for economic reasons, because long growth times limit process throughput, and for thermal reasons, because heat produced in the transistors must be effectively dissipated. Most buffer layers are made of ternary compound semiconductors, such as InAlAs or AlGaAs, which have poor thermal conductivity86.

Results And Discussion of Trans conductance in III-V MOSFET

The transfer characteristics for an InGaAs surface-channel MOSFET are shown in Fig. 5. Here, the transconductance is deduced both from dc and RF measurements (20 GHz). The curves have similar shape and show a peak transconductance close to *VG* = 0.1 V; however, *gm* is about three times higher at RF. Also, it should be noted that all measurements on the surface channel MOSFET presented in this work were conducted about six months after device fabrication. During this time, the peak dc transconductance has degraded by a factor of three and the threshold voltage has shifted more than 0.5 V, indicating the creation of excess defects in the oxide.

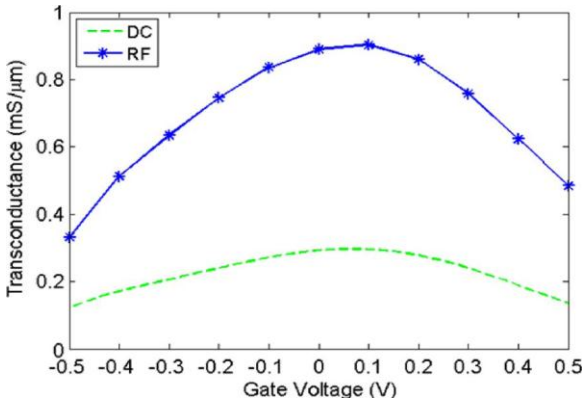

Fig. 5. Transconductance as a function of gate voltage for two different measurements on an InGaAs surface-channel MOSFET is plotted. The green dotted line shows the gm deduced from dc measurements, and the blue starred line shows the gm deduced from RF measurements. A drain voltage of VD = 0.55 V was used. The threshold voltage is Vt= −0.5 V

Aging is particularly pronounced for these devices as no passivation is used and the gate oxide is directly exposed to air, which could cause damages such as an increased number of traps in the oxide. Fig. 6 shows the frequency dependence of *gm* for the vertical InAs NW MOSFET and InGaAs surface-channel MOSFETmeasured in the 1 Hz–67 GHz-frequency range. For low frequencies (below 100 MHz), *gm* increases at a rate of about 0.009 MS/μm per decade and 0.006 mS/μm per decade for the NW and surface-channel Sdevices, respectively, which result inroughly a doubling of *gm.*from dc up to 100 MHz These high rates in the two DUTs distinctly indicate high densities of deep border traps in both devices.

Advantages And Challenges Of III-V Mosfet

Compound semiconductors have the potential for low-power and high-speed logic because their high-mobilityand low energy-delay productcharacteristics. Current III-V FETs like HEMTs have already shown higher unity gain cutoff frequency (fT) and less active power than silicon NMOS of the same scaling dimension[6]. However, Ion/Ioff ratio is limited by the schottky gate leakage. To get high performance devices, III-V compatible gate dielectric needs to be applied on the material systems. The major difficulty is the lack of a low density of interface states. For CMOS logic applications, high hole mobility channeldevices are needed as well. But current III-V materials show hole mobility just comparable to Si. The challenge includes improving hole-mobility in III-Vs or utilizing novel materials such as Ge.

Conclusion and Future Work

As III-V MOSFET has High Electron Mobility, High-low Field Drift Velocity, Good for Low Power Logic Applications, Tight Carrier Confinement in Quantum Well, Wide range of Band Gaps III-V MOSFET is preferred as a advanced low dimensional transistor.

Future work includes Finding Optimum Fabrication Parameters of III-V MOSFET through Process Simulation, Performance Analysis through Device Simulation and Circuit Implementation with Fundamental Logic Gates using SILVACO Tool.

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