IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 4, Issue 1, Ver. I (Jan. 2014), PP 10-15
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

A Novel CMOS Model Design for 2.4 GHz Narrowband LNA input matching using inductive Degenerated Topology

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Abstract: *2.5 GHz narrow band inductive degenerated (LNA) low noise amplifier implemented in a 0.18 µm RF CMOS process which is used in particularly telecommand system for satellite and also for WSN (Wireless sensor networks. The amplifier provides a forward gain (S_{21}) of > 16 db with a noise figure of S_{11} < 2db. While drawing of 10 mw from 1.8v Supply by using inductive coupled degenerated LNA.*
General Terms: *LNA, Noise figure, gain, linearity.*
Keywords*:RF CMOS, VLSI Design, Wireless Communications*

I. Introduction

Present days the wireless design suffers from face noise,matching and signal detection.This is a new challenge for RFIC designers[1][2] .Among the many blocks of the wireless design the crucial block is the low noise amplifier. The purpose of this block is to match the antenna input with remaining circuitry .To implement the different topologies of the multi standard transmissions are recognised [9].

Due to low economy higher integration scaling technology the CMOS the competitor for the implementation of radio transceiver for variouswireless communication system.one of the primary advantage of using the CMOs is ease of integration with digital section on the single chip. The design of the low noise amplifier for the satellite is used in wireless telemetry communication system. It is divided into many subsystems of number of sensors and actuators. One of the subsystems is the master transponder which is facing earth and then it communicates with the earth station.Remaining subsystems are accessed by this master unit. By telemetry unit(TMMASTER)the gathered information from the different subsystem are relayed to earth station(TCMASTER).[9]

Telecommand unit is one which ,the earth station sends the command to control the various subsystem.However the takes place through respective master unit.dve to the advantage like less weight of satellites the communication must be through wireless. It is based on IEEE standard.

The first block of receiver is low noise amplifier(LNA).Depending on noise figure and gain the overall performance of receiver is sustained. The design of low noise amplifier is such that it must present minimum noise figure and then gain with sufficient linearity.To terminate the unknown length of the transmission line that deliver the signal from antenna to amplifier.IIP3 provides the 50Ωinput noise amplifier even a good input match is more sensitive to the quality of the point of terminating impedances .The main reason of the design of low noise amplifier which is aimed at low power consumption because the standard that is used for implementation of communication system is at low rate.[9]

1.1 LNA Requirements:

1. Gain (10-20 db) to amplify the received signal and to reduce the input referred noise of the subsequent stages.
2.Good linearity: Handling large undesired signals without much distortion.
3. Low noise for high sensitivity
4. Maximum power gain 50 Ω termination for proper operation and can route the LNA to the antenna which is located an unknown distance away without worrying about the length of the transmission line [12].

1.2 Basic Topologies

1. Wide band LNA input matching topologies (a) Resistive termination (b) common gate (c) resistive shunt feedback.
2. Narrow band LNA input matching topologies (a) inductive degenerated (b) resistive terminated [12].

1.3 Inductive degenerated LNA:

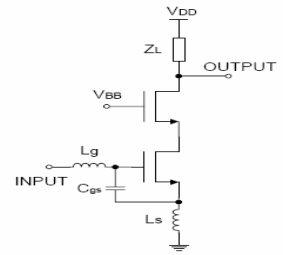


Fig1: Inductive degenerated low noise amplifier

From Figure1 we can say that Input impedance behaves like a series RLC circuit, due to the addition of L_g in the circuit[13][5].

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{ga}} + \frac{g_m L_s}{C_{gs}} \text{ .....(1)}$$

matching occurs when:

$$Z_{in}(j\omega_o) = R_s, \omega_o^2 = \frac{1}{(L_g + L_s)C_{gs}} \text{ and } R_s = \frac{g_m L_s}{C_{gs}} = \omega_T L_s$$

Ls can be selected by: $L_s = \frac{R_s}{\omega_T}$ if this value is too small to be practical, a capacitor can be inserted in shunt with Cgs to artificially reduce $\omega_{T]}$[13][5]

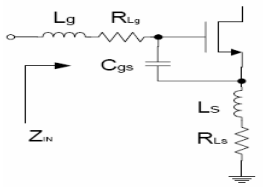


Fig2non-idealites of input impedence.

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \omega_T L_s + \frac{1}{s\frac{1}{\omega_T R_{Ls}}} + R_{Lg} + R_g + R_{Ls} + R_{g,NQS} \quad (1)$$

$$R_s = \frac{R_{poly,sh} W}{12n^2 L}$$

$$R_{g,NQS} = \frac{1}{5g_m}$$

$$Z_{in}(j\omega_0) = \omega_T L_s + R_{Lg} + R_g + R_{Ls} + R_{g,NQS} \quad (2)$$

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)(C_{gs} // \frac{1}{\omega_T R_{L_s}})}}$$

inductance loss R_{Lg}:offsetZ_{in};R_{LS}: offset Z_{in} and ω_0;Gate resistance Rg:offsetZ_{in};NQS gate resistance R_g;NQS:offsetZ_{in}; Q-boosting [5]:

at resonance we get Q boosting effect:

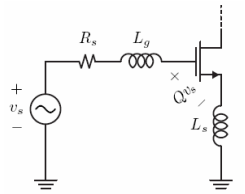


Fig.3. Q-Boosting

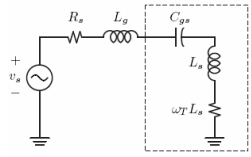


Fig.4.equalent circuit for Amplifier input ignoring C_gD

at resonance we get Q boosting effect:

$$Q = \frac{1}{(R_s + L_s\omega_T)C_{gs}\omega_0} = \frac{1}{2R_sC_{gs}\omega_0} \quad (3)$$

$V_{gs}=QxV_s$

$I_d=g_mv_s=\underbrace{Qg_m}_{G_m}v_s$

$$\underbrace{\frac{1}{2R_s}\left(\frac{\omega_T}{\omega_0}\right)}_{G_m}v_s$$

Need to watch out for linearity as vgs is Q times larger than the input signal. Short channel devices operating in velocity saturation regime (i.e., large overdrive voltage) are more forgiving as their gm is relatively constant.[13]

Equivalentinput network:
From the source, the amplifier input (ignoring C_{gd}) is equivalent to:
At resonance, the complete circuit is as fig4:

Noise Analysis: from fig5, The output noise current due to R_s and R_g is simply calculated by multiplying the voltage noise sources by G_m.[13]

The calculation of output noise current due to drain noise is more involved:i^2_d flows partly into the source of the device, it activates the g_m. Output Noise current i^2_d Output noise current: [8]

$$\overline{i_{no}^2} = G_m^2\left[\overline{v_{Rs}^2} + \overline{v_{Rg}^2}\right] + \overline{i_{d,out}^2} \quad (4)$$

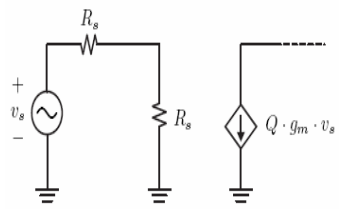


Fig.5. Complete circuit at Resonance

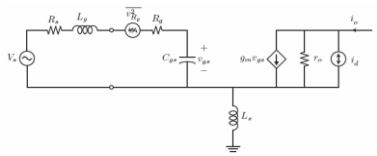


Fig.6. Q-Boosting Noise Analysis

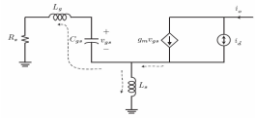


Fig.7. Q-Boosting Noise Analysis-Drain Noise

$$G_m = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_o}\right)$$

Drain Noise: The noise component flowing into the source is given by the current divider:

$$\upsilon_{gs} = -\frac{(g_m\upsilon_{gs} + i_d)\, X\, j\omega L_s}{j\omega L_s + \frac{1}{j\omega C_{gs}} + j\omega L_g + R_s X \frac{1}{j\omega C_{gs}}} = -g_m j\omega L_s \quad (5)$$

$$-\left(g_m\upsilon_{gs} + i_d\right) X \frac{1}{j\omega C_{gs}} (at\ resonance)\, X\ \frac{j\omega L_s}{R_s}$$

$$g_m\upsilon_s = -\frac{i_d}{2} \quad (6)$$

here we are not including R_g in the small signal model.

Total Output Noise: Let's first ignore the correlation of the gate noise and drain current noise. Notice only one forth of the drain noise flows to output.

$$\overline{i_{no}^2} = G_m^2 \left(\overline{V_{Rs}^2} + \overline{V_{Rg}^2}\right) + \frac{1}{4}\overline{i_d^2} \quad (7)$$

$$G_m = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_o}\right)$$

$$F = \frac{\overline{i_{no}^2}}{G_m^2 \overline{V_{Rs}^2}} = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} g_m R_s \left(\frac{\omega_o}{\omega_T}\right)^2 \quad (8)$$

Note that the Noise figure at resonance is the same as CS amplifier w/o inductive degeneration. Inductive degeneration did not raise $F_m$in but matched the input.If we consider the correlation of the gate noise and drain current noise then one can show.

$$F = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\chi g_m R_s \left(\frac{\omega_o}{\omega_T}\right)^2 \quad (9)$$

$$\chi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L^2) \quad (10)$$

$$Q_L = Q_{C_{gs}} = \frac{1}{\omega_0 R_s C_{gs}} = \frac{\omega_0(L_g + L_s)}{R_s} \quad (11)$$

Optimal Noise figure happens for a particular Q_L. Possible to obtain a noise and power match.[14]

OptimalQ_L : If we try to optimize the noise figure while power dissipation is kept constant then:

i.$Q_{L,opt}$ will be independent from the frequency and around 4.5

ii. $F_m$in is not too sensitive to Q_L and only changes by less than 0.1dB for Q_L between 3.5 and 5.5

iii. Smaller Q_L results in larger bandwidth and smaller inductors, while a larger Q_L results in narrower bandwidth and larger inductors.

Linearity: Linearity of a MOS transistor in saturation region:[13][14][5]

$$V_{IIP3,strongMOS} = \frac{4}{3}\frac{V_{eff}}{\theta}\left(2 + \theta V_{eff}\right)\left(1 + \theta V_{eff}\right) > \frac{8}{3}\frac{V_{eff}}{\theta} \quad (12)$$

$$V_{eff} = V_{gs} - V_{th} \qquad \theta = \frac{1}{E_{sat}L}$$

$$E_{sat} \approx 1V/\mu m$$

$$\text{for } L \approx 0.35\mu m - 0.18\mu m$$

IIP3 is independent of W

$$V^2_{IIP3,LNA}\left(V^2\right) = \frac{16}{3}\frac{P_D^2}{P_o^2\theta^2}(2 + \rho)\left(1 + \frac{1}{\rho}\right)^3 \quad (13)$$

$$\rho = \theta V_{eff} \qquad P_o = \frac{3}{2}\frac{V_{sat}E_{sat}}{\omega_o R_s}V_{DD}$$

Effect of R_L o**n input match:** We ignored the effect of load impedance on input impedance in previous derivations. It can be shown that[13]

$$Z_{IN} = \frac{1}{jC_{GS}\omega} + jL_S\omega + \frac{r_o}{r_o + R_L + jL_S\omega}[L_S\omega_S + \frac{(L_S\omega)'}{r_o}] \quad (14)$$
$$\approx \frac{1}{jC_{GS}\omega} + jL_S\omega + \frac{r_o}{r_o + R_L}[L_S w_r]$$

R_L can be large and it can drop the real part of the input impedance when we use resonators at output. Notice that the output impedance influenced the input impedance even in the absence of C_gd

Design Recipe for Inductive degenerated of LNA:
Step1: Choose Q_L for optimal[13]

$$NF \Rightarrow C_{gs} \Rightarrow Width(W)$$

$$\left(Q_L = \frac{1}{\omega_O R_S C_{GS}} \right)$$

Step2: Determine the current I_d from power budget.
Step3: From W & $I_d \Rightarrow$Width(W)
Step4: From g_m and $V_{eff} \Rightarrow \omega_T$ andF_{min}
Step5: Select L_s and L_g for the input network

$$L_s = \frac{R_S}{\omega_T} L_g = \left(\frac{1}{\omega_0^2 C_{gs}} \right) - L_s$$

Design Recipe Iterations: If NF is not low enough, increase ω_T by increasing I_d(with fixed device size) and for a fixed current density, increasing Q will reduce device size thus reduce total power and hence NF will increase. If the Linearity does not meet, reduce Q, burn more current and apply proper linearization techniques. If we need to increase gain, choose larger Q_L,Larger g_m and larger Load (Z_L) [13][2].

II. Simulation Result Analysis

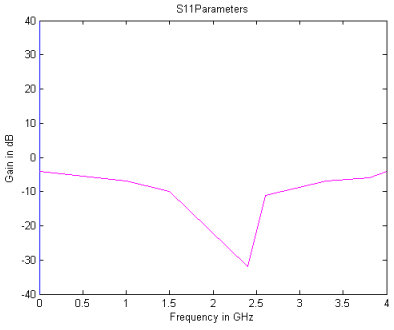
	Calculated	Simulated
M_1	110 μm/0.18	110 μm/0.18
M_2	110 μm/0.18	110 μm/0.18
L_g	31nH	20nH
L_s	0.14nH	0.28nH
I_d	9mA	8.6mA
Z_L	2.4 ω	26 ω

TABLE-1. PARAMETERS

	Specs	Simulation
Frequency	2.4Ghz	2.4Ghz
S_{11}	-10dB	- 32 dB
S_{21}	16 dB	15.7dB
NF	2dB	≈ 0.62dB
IIP3	10dBm	-6.85dBm
Current	10mA	8.6mA
Supply	1.8V	1.8V

TABLE-2. PERFORMANCE

The design was simulated using the ADS and also cadence tools provided for the 18μmRF CMOS process. The following graphs shows S21,S11, noise figure, IIP3, stability factor of inductive degenerated LNA



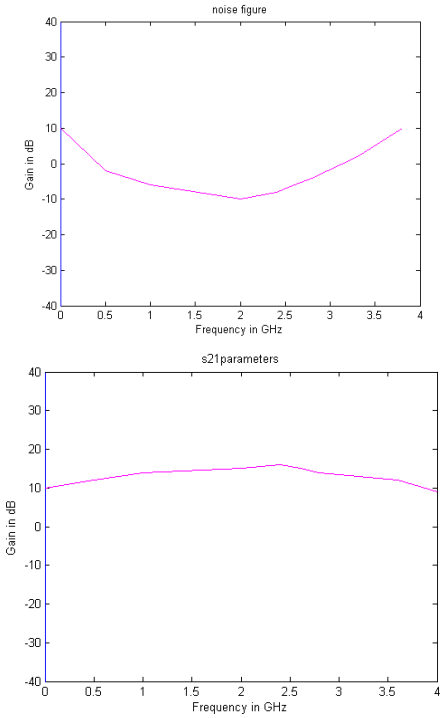


Fig 8(a)S11 parameters(b)noise figure and (c)S21 parameters.

III. Conclusion

The design of receiver supporting 4G wireless applications in all bands presents many challenges. Some of the characteristics of the receivers are multi band multi standard operation, MIMO support, low power and low cost. By applying mathematical descriptions for key performance parameters of LNA is required 4G front ends. This paper has presented the design of gain S21 16dB with a noise figure 2dB while drawing 10mW power from 1.8 volts supply by using inductive coupled degenerated LNA topology. A lesson learned in this design is the importance of intuitive understanding of resonance and circuit theory when designing LNAs using wireless telemetry telecommand system and also for wireless sensor network.

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