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Low Voltage Low Power SRAM design based on Schmitt Trigger technique

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Abstract: *Nowadays Electronic devices are portable which requires low power/low voltage requirement to maximize the battery lifetime. We propose Schmitt Trigger based SRAM bitcell that can operate on low supply voltages. The proposed Schmitt trigger SRAM bitcell resolves the fundamental conflicting design requirement of read versus write operation of conventional 6T bitcell and it gives better read-stability as well as better write ability compared to the other bitcell. This work is executed under the Mentor Graphics EDA tools in 350nm, 250nm CMOS technology. ST-2 cell consumes less power than ST-1 cell.*
Keywords*: low voltage SRAM, Schmitt Trigger (ST), voltage scaling*

I. Introduction

Aggressive scaling of transistor dimensions with each technology generation has resulted in increased integration density and improved device performance. Leakage current increases with the scaling of the device dimensions. Increased integration density along with increased leakage necessities ultralow-power operation in the present power constrained design environment. The power requirement for the battery-operated devices such as cell phones and media devices is even more stringent. Reducing supply voltage reduces the dynamic power quadratically and leakage power linearly to the first order. Hence, supply voltage scaling has remained the major focus of low power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor [1]. With the scaling of MOSFET dimensions, microscopic variations in number and location of dopant atoms in the region of the device induce increasingly limiting electrical deviations in device characteristics [2]. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations. Interdie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell resulting in asymmetrical characteristics. The combined effect of lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold failure, write-failure and access-time failure [3].

Moreover, it is predicted that embedded cache memories, which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling [4].In a given process technology, the maximum supply voltage for the transistor operation is determined by the process constraints such as gate-oxide reliability limits. Vmax is reducing with the technology scaling due to scaling of gate-oxide thickness. The minimum SRAM supply voltage, for a given performance requirement (Vmin), is limited by increased process variations and the increased sensitivity of circuit parameters at lower supply voltage. With the technology scaling, Vmin is increasing, and this closes the gap between Vmax and Vmin. Hence, to enable SRAM bitcell operation across a wide voltage range, Vmin has to be further lowered. Several design solutions such as read-write assist techniques and bitcell configurations have been explored [5]. Primary goal of this paper is to reduce the total power dissipation.

II. Past Sram Bitcell Research

Several SRAM bitcells have been proposed with different design goals such as bit density, bitcell area, low voltage operation and architectural timing specifications. Fig.1 lists the different bitcells SRAM configurations.

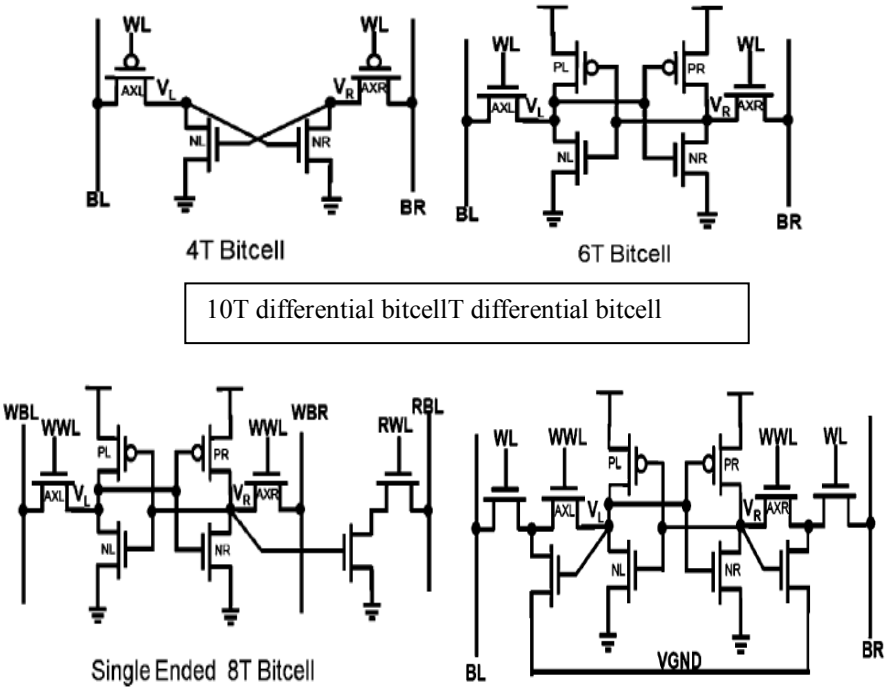


Fig.1 different bitcell configurations

In the four transistor (4T) loadless bitcell, PMOS devices act as access transistors[st-6].The design requirements in such that pMOS off state current should be more than the pull-down nMOS transistor leakage current for maintaining data "1" reliably. With increasing process variations and exponential dependence of the subthreshold current on the threshold voltage, satisfying this design requirement across different process, voltage, and temperature (PVT) conditions may be challenging.

A 6T bitcell comprises of two cross-coupled CMOS inverters, the contents of which can be accessed by two nMOS access transistors. The 6T bitcell is the "de facto" memory bitcell used in the present SRAM designs [6]. Successful write operation necessitates skewed inverter sizing, resulting in asymmetrical noise margins. In a single-ended 8T bitcell, extra transistors are added to the conventional 6T bitcell to separate read and write operation [7] [8] [9] [10]. Recently, differential 8T bitcells utilizing RWL/WWL cross-point array and data-dependent VCC have also been reported [11] [12]. Single-ended 10T bitcells are similar to the single-ended 8T bitcell except for the read port configurations. Additional transistors are used to control the read bit line leakage [13] [14]. A similar 10T cell with column-assist technique is also reported [15]. However, series-connected write access transistors degrade the write-ability of the bitcell and needs write-assist circuits such as word-line boosting for a successful write operation.

In all of the previously reported bitcells, the basic element for the data storage is a cross-coupled inverter pair. Extra transistors are added to decouple the read and write operations. None of the past reported bitcells incorporate process variation tolerance for improving the stability of the cross coupled inverter pair of an SRAM bitcell operating at ultralow supply voltage. Traditionally, device sizing has been adopted to mitigate the effect of process variations. However, device sizing is not effective in improving the bitcell stability at very low supply voltage [16].

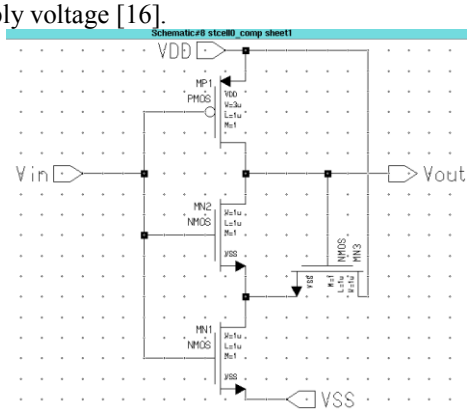


Fig2. Basic Schmitt trigger bitcell

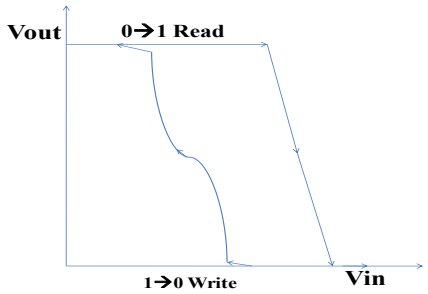


Fig3.Input transition dependant characteristics

Hence we need a different design approach for successful low voltage SRAM design in nanoscaled technologies. In this work we propose Schmitt Trigger based SRAM bitcell having built-in feedback mechanism that exhibits the process variation tolerance. This robust process tolerance can be an essential attribute SRAM scaling into future nanoscaled technology nodes.

III. Sram Bitcells With Schmitt Trigger Technique

In order to resolve the conflicting read versus write design requirements in the conventional 6T bitcell, we apply the ST principle for the cross-coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition [17]. In the proposed ST SRAM bitcells, the feedback mechanism is used only in the pull-down path, as shown in Fig.2. During 0→1 input transition, the feedback transistor (NF) tries to preserve the logic "1" at the output (Vout) node by raising in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initialed by a 0→1 input transition for the inverter storing logic "1", higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation.

For the 1→0 input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bitcell. Two novel bitcell design are proposed. The first ST-based SRAM bitcell has been presented in paper [18]. Another ST based SRAM bitcell which further improves the bitcell stability has been reported in [19]. To maintain the clarity of the discussion, the ST bitcell in [18] is named the "ST-1" bitcell while other ST bitcell in [19] is named the "ST-2" bitcell.

1. SCHMITT TRIGGER BITCELL-1(ST-1)

Fig.4 shows the schematic of the ST-1 bitcell. The ST-1 bitcell utilizes differential sensing with ten transistors, one word-line (WL), and two bitlines (BL/BR). Transistors PL-NL1-NL2-NFL forms one ST inverter while PR-NR1-NR2-NFR forms another ST inverter. Feedback transistors NFL/NFR raise the switching threshold of the inverter during the 0→1 input transition giving the ST action. Detailed operation of the ST-1 bitcell can be found in [18].

2. SCHMITT TRIGGER BITCELL 2(ST-2)

Fig .5 shows the schematics of the ST-2 bitcell utilizing differential sensing with ten transistors, two word lines (WL/WWL), and two bitlines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL Signal is asserted during the write operation.

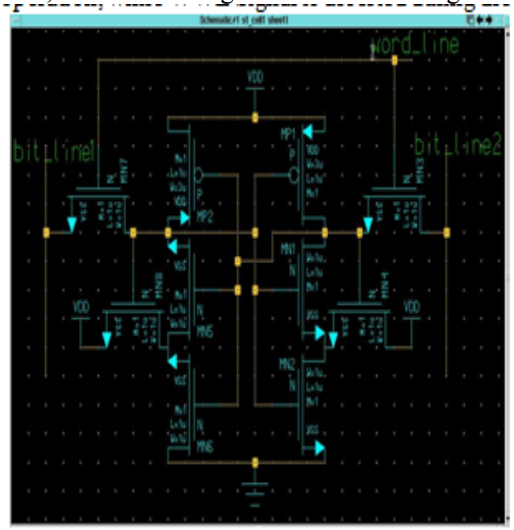


Fig. 4 ST-1 Bitcell schematic

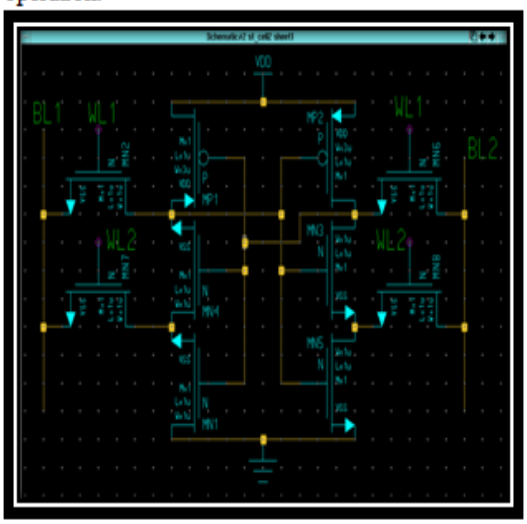


Fig. 5 ST-2 Bitcell schematic

OPERATION	WL	WWL
READ MODE	1	0
WRITE MODE	1	1
HOLD MODE	0	0

IV. Vmin ANALYSIS OF SRAM CELLS & RESULTS

1. **AREA** The Schmitt trigger bitcells consumes approximately 2x area compared with the 6T min cell [18] [19]. Hence in order to estimate the minimum supply voltage Vmin, it is only fair to compare the bit cells under iso-area condition. Fig.6 shows the thin cell illustrative of the 6T min cell and the proposed ST-1, ST-2 bitcell shown in Fig.7, 8. In thin cell approach, the vertical dimension is determined by the poly pitch while lateral dimension is determined by the device sizing. In this work we use 6T mincell device widths of 500nm, 500nm, and 1000nm for pull-up/access/pull-down transistors, respectively.

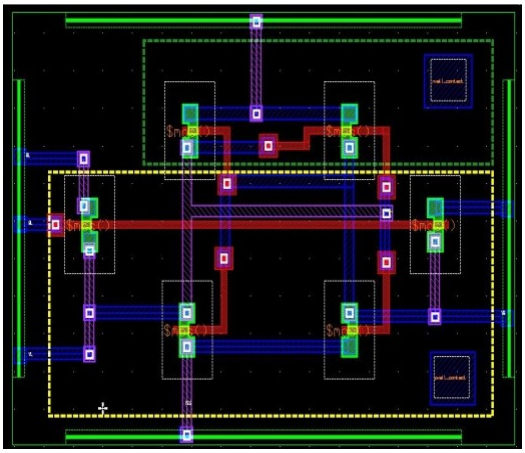


Fig.6 Conventional 6T Bitcell

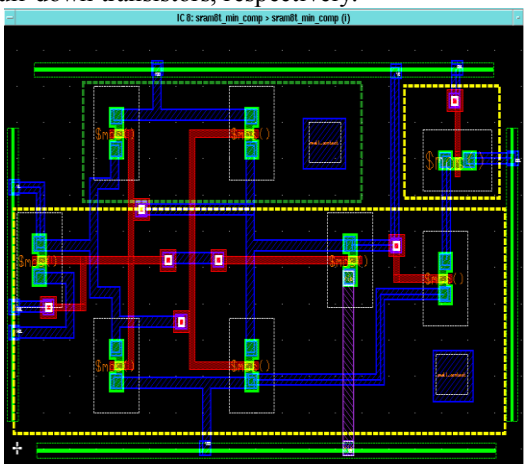


Fig.7 8T bitcell layout

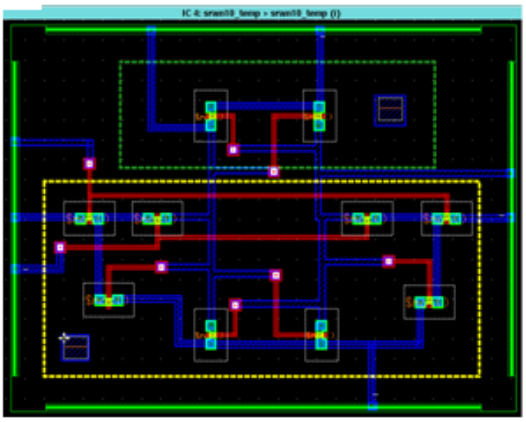


Fig.8 10T bitcell layout

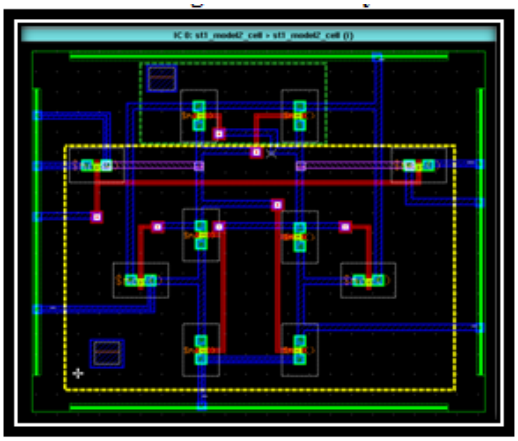


Fig.9 ST-1 Bitcell layout

Table: Area analysis

S.NO	BITCELL	AREA(um)
1	6T SRAM	116X170
2	8T SRAM	110X192
3	10T SRAM	195X260
4	ST-1 SRAM	180X215
5	ST-2 SRAM	162X217

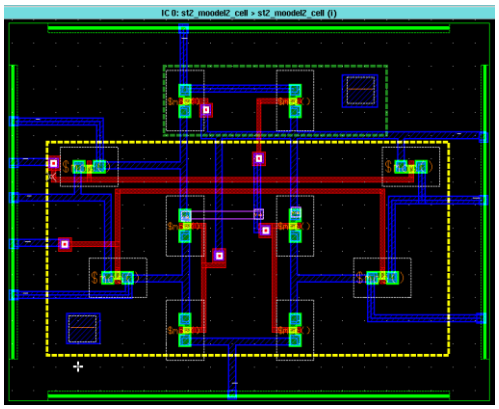


Fig.10 ST-2 Bitcell layout

2. **8T Bitcell:**8T (ST) bitcell area is 30% (100%) larger than 6T mincell [7] [8] [9] [10] [18] [19]. Table 1 shows the split-up of the total subarray area containing 6T/8T/10T/ST1/ST2 bitcells. Bitcell areas are normalized to 6T mincell area.
3. **10T Bitcell:**A 10T bitcell with additional read ports utilize differential sensing without disturbing the bitcell nodes during a read operation [20]. The differential 10T bitcell with two separate read ports consumes ~1.66X larger area compared with the 6T mincell. Table 2, lists device sizing for various bitcell topologies used for Vmin analysis.

Table.2 Comparison of various bitcell Vmin

S.NO	BITCELL TOPOLOGY	Vmin(V)
1	6T SRAM	1.5
2	8T SRAM	2
3	10T SRAM	3.3
4	ST-1 SRAM	0.9
5	ST-2 SRAM	0.8

Table.3 Device sizing for various bitcell topologies (device sizes in nm)

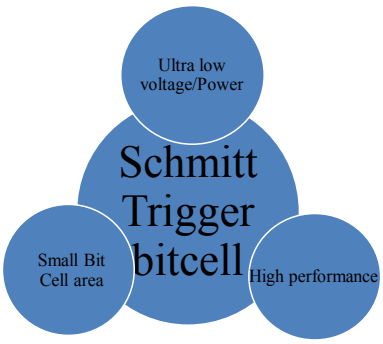
S.NO	Bitcell topology	NL1/NR1	NL2/NR2	PL/PR	AXL/AXR	NFL/NFR	N1/N2	N3/N4
1	6T mincell(1xarea)	1000	-	500	500	-	-	-
2	8T mincell	1000	-	500	500	-	500	-
3	10 mincell	1000	-	500	1000	-	500	500
4	ST-1 bitcell	2000	1000	1000	2000	1000	-	-
5	ST-2 bitcell	2000	1000	1000	2000	1000	-	-

4. **POWER ANALYSIS:**From the all configurations we can conclude that the ST-2 bitcell consumes less power than all other topologies.

Table.4 Comparison of Power dissipation

S.NO	DIFFERENT TOPOLOGIES	TOTAL POWER DISSIPATION(W)
1	6T SRAM	541.62P
2	8T SRAM	1.26N
3	10T SRAM	1.89N
4	ST-1 SRAM	1.71N
5	ST-2 SRAM	0.98N

5. Die Photograph



V. Conclusion

In this work, we proposed a robust Schmitt trigger based SRAM suitable for low voltage applications. Built in feedback mechanism can be effective for process tolerant, low voltage SRAM operation in future nanoscaled technologies. Lowering supply voltage is an effective way to achieve low power operation. Simulations in Mentor Graphics EDA Tools with TSMC-250nm, TSMC-350nm technology.

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