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Design of Low Power Negative Pulse-Triggered Flip-Flop with Enhanced Latch

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Abstract: *In this paper, a new low power pulse-triggered Flip-Flop is designed with enhanced latch where the pulse-generation circuit is constructed using one pmos transistor and Data is transferred through two nmos transistors and a inverter, when compared with the conventional pulse-triggered flip-flops, it consumes only 0.373µw of power to activate the circuit and occupies only less area on chip i.e. 5 transistors and two inverters. The simulation results are done based on CMOS 50 nm technology.*

Keywords: *Flip-Flop, Low power, Pulse-triggered*

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power [6]. Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave-based FF in the applications of high-speed operations [2]-[5]. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses are sufficiently wide to trigger the data capturing of the latch. Explicit-type P-FF designs face a similar pulse width control issue, but the problem is further complicated in the presence of a large capacitive load, e.g. when one pulse generator is shared among several latches. In this paper, we will present a novel low-power implicit-type Negative Pulse Triggered P-FF design which occupies only less area on chip and attains competitive power performance with low amount of delay

II. Proposed Implicit-Type P-Ff

A. Conventional Implicit-Type P-FF Designs

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed .A state-of-the-art P-FF design, named ip-DCO, is given in Fig. 1 [4].

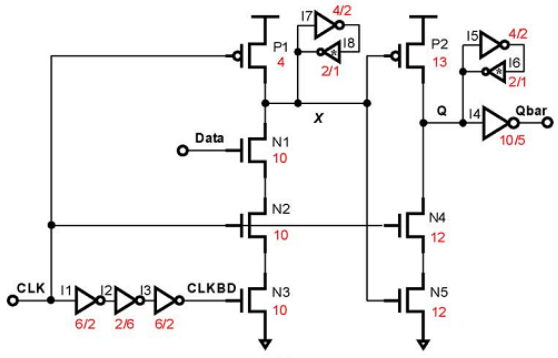


Fig. 1(IP-DCO)

It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node will be discharged on every rising edge of the clock. The other problem is that node controls two larger MOS transistors (P2 and N5).Fig.2 shows an improved P-FF design, named MHLLF, by employing a static latch structure presented in. Node is no longer precharged periodically by the clock signal. A weak pull-up transistorP1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero. This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node is not pre-discharged.

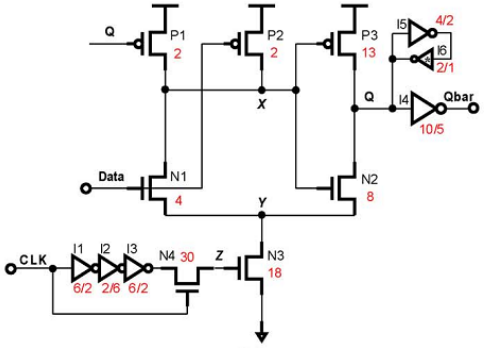


Fig. 2 (MHLFF)

Another drawback of this design is that node becomes floating when output Q and input Data both equal to "1".Fig. 3 shows a refined low power P-FF design named SCCER using a conditional discharged technique. The discharge path contains nMOS transistors N2 and N1 connected in series. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high.

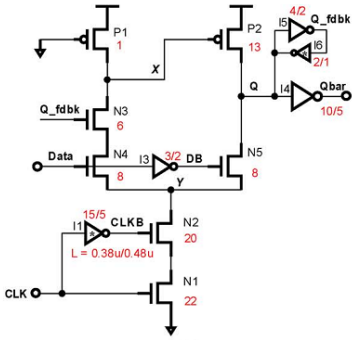


Fig.3 (SCCER)

The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series, i.e., N1 through N4. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

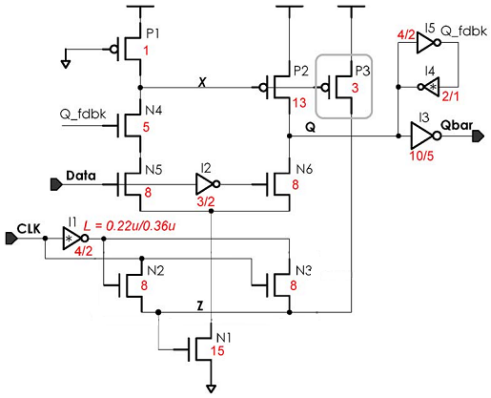


Fig.4 (Pulse-Enhancement FF Design)

The Pulse-Enhancement FF design, as shown in Fig.4 [1]. In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, transistor P3 is added [1]. Transistor P3 is normally turned off because node is pulled high most of the time. The generated pulse is taller, which enhances the pull-down strength of transistor N1.With the intervention of P3, the width of the generated discharging pulse is stretched out. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output is subject to a data change from 0 to 1[1].But due to more number of transistors for the latch and pulse generation circuitry, the power consumption still more, so this is a major drawback and in order to overcome that Negative Low-power pulse-triggered Flip-Flop is designed

B. Proposed P-FF Design

Fig.5 shows the proposed low-power Negative Pulse-Triggered Flip-Flop, which is constructed using 5 transistors(2 nmos transistors and 3 pmos transistors) and two inverters, outputs are indicated using Led's. In this design, clock is applied to P2 (pmos transistor) so whenever the clock is at low state, then pmos p2 turns on and provides short circuit path to the upper circuit. At the input stage, if Data is 1, the pmos P1 which is always on, sends strong 1 to the circuit, and the N1 is turned on which provides discharging path from P3 to P2,it resembles providing logic 0 to P3(pmos transistor),so P3 is turned on and vdd flows from P3 to output, means logic 1.Here as input is given to Inverter I1, the Nmos N2 is turned off.

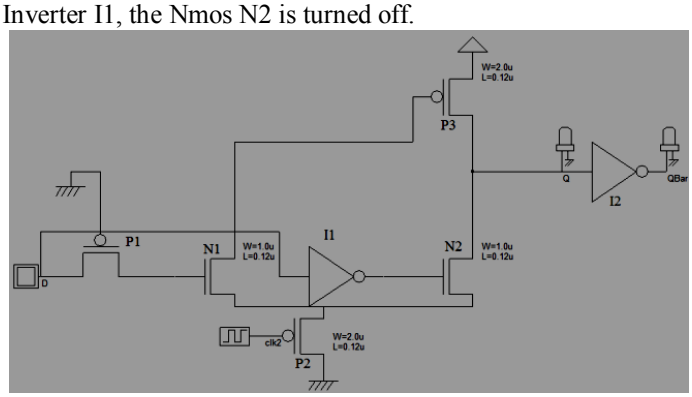


Fig.5 PROPOSED FLIP-FLOP DESIGN

Now take Data input as 0, and even if clock is at low state, as N1 transistor is turned off, there will be no discharging path from P3 to P2 and the input to the inverter I1 is 0, so N2 is turned on, there will be discharging path from output Q to P2, through N2, providing Output Q as 0(zero), Circuit reflects the following conditions

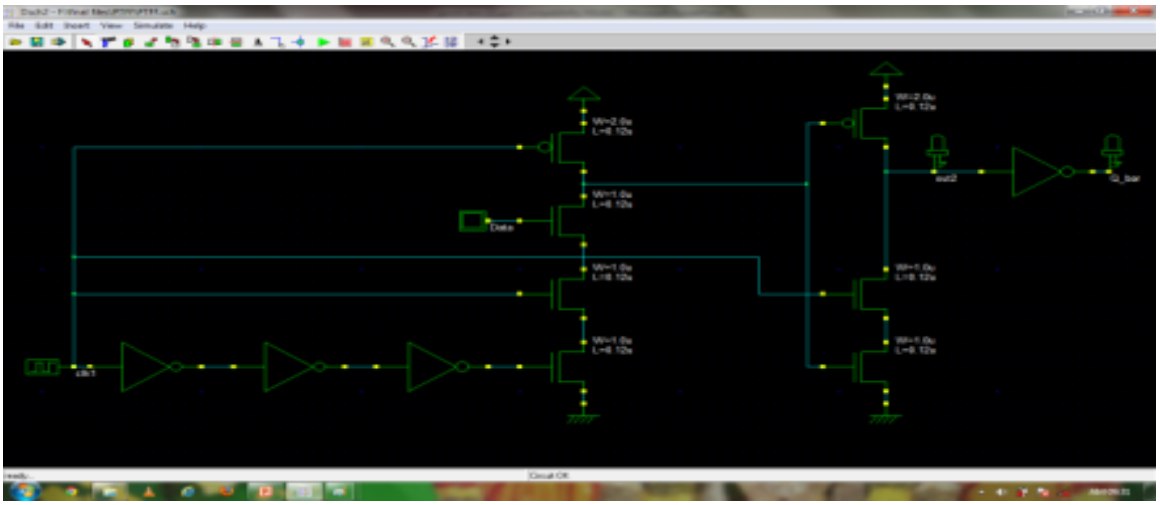
If D is 1, then Q will be 1, when clock is at low state

If D is 0, then Q will be 0, when clock is at low state

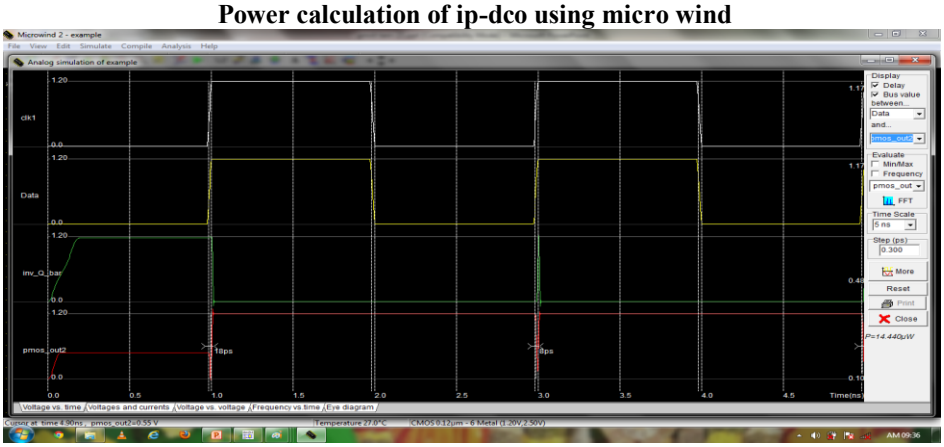
III. SIMULATION RESULTS

Using Dsch and Micro wind, the pulse-triggered Flip-flops are analyzed; Timing Diagrams and power calculations are shown below

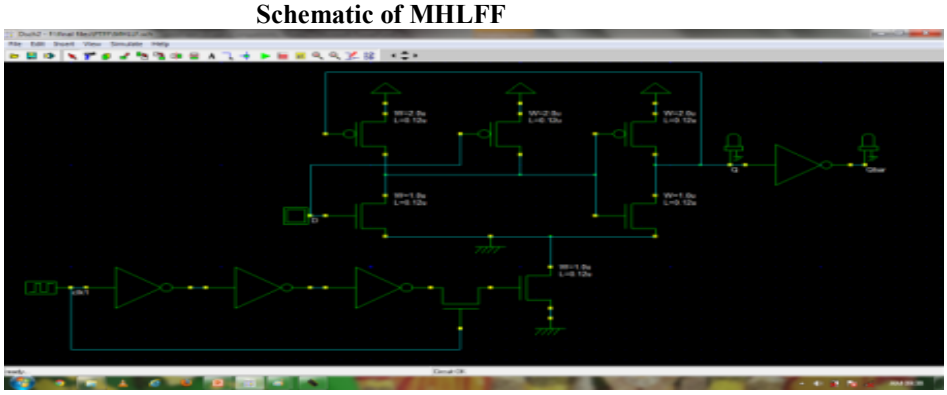
Schematic of IP-DCO



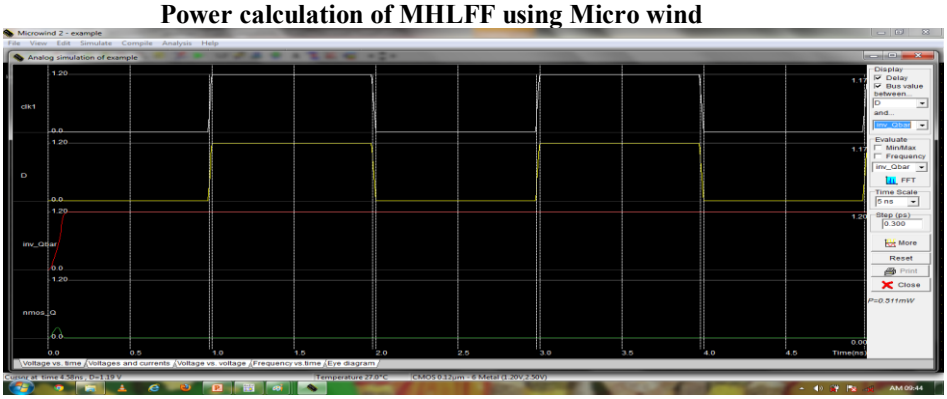
Power calculation of ip-dco using micro wind



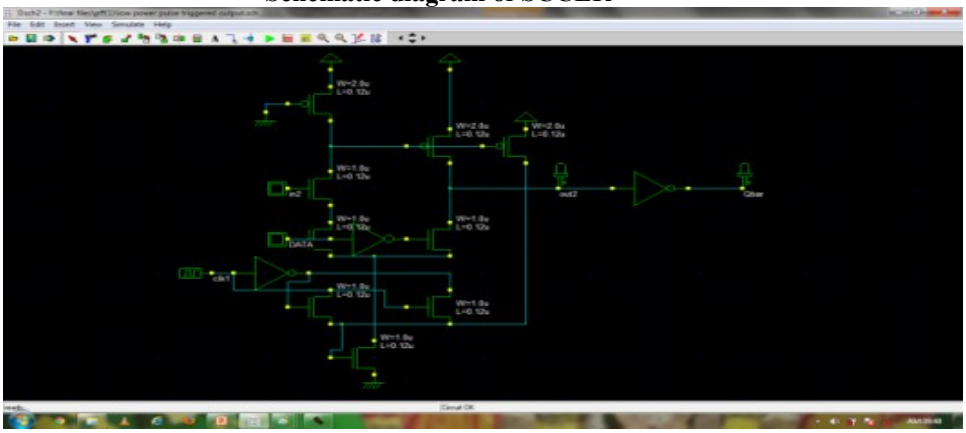
Schematic of MHLFF



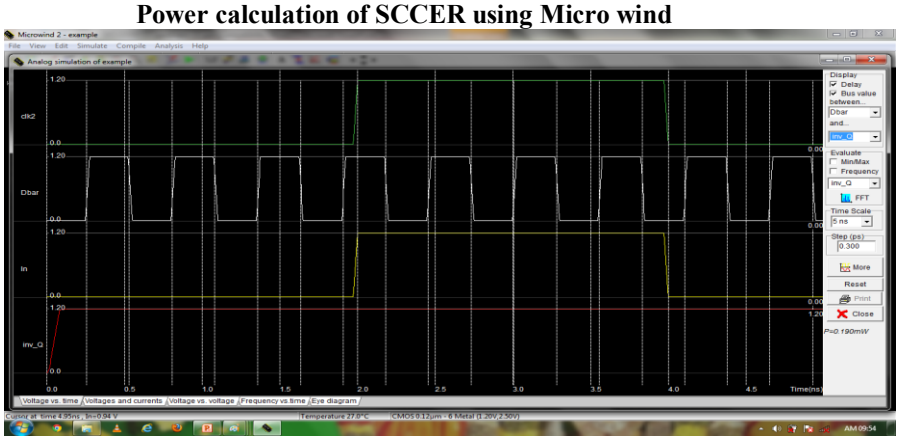
Power calculation of MHLFF using Micro wind



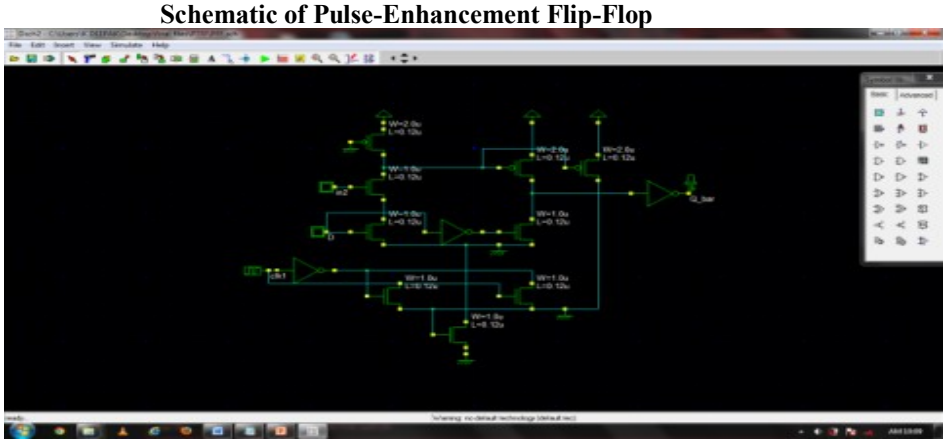
Schematic diagram of SCCER



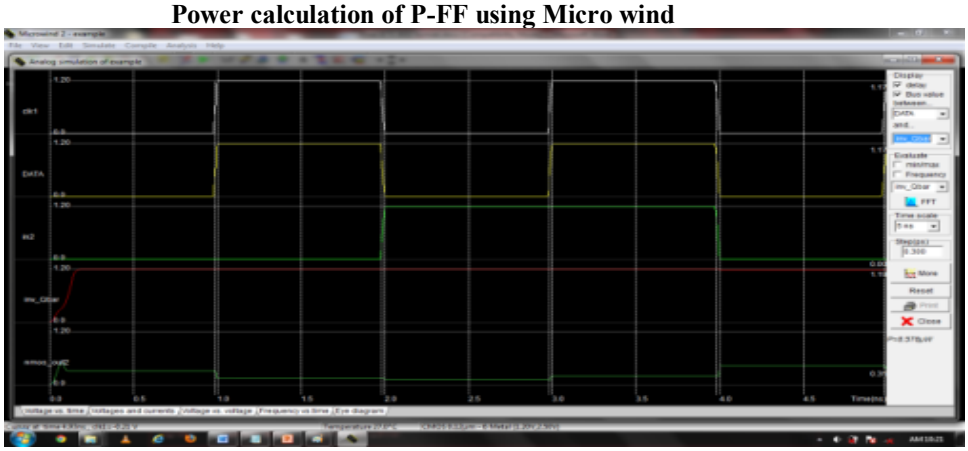
Power calculation of SCCER using Micro wind



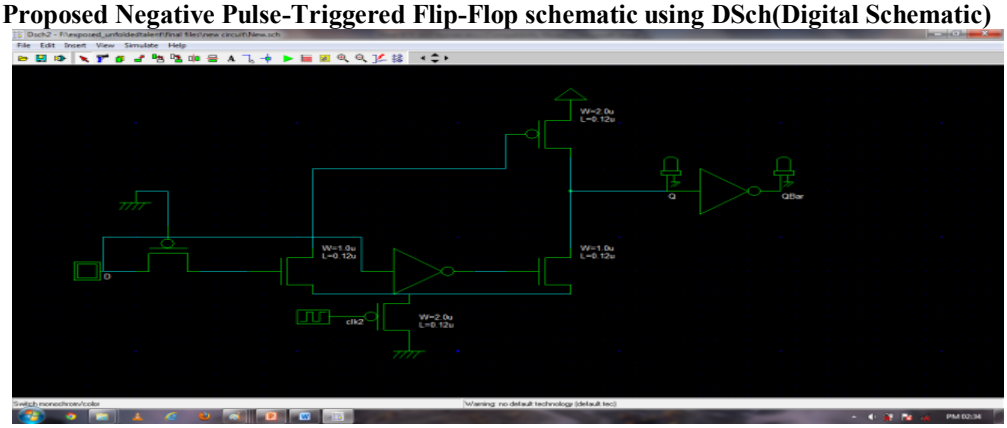
Schematic of Pulse-Enhancement Flip-Flop



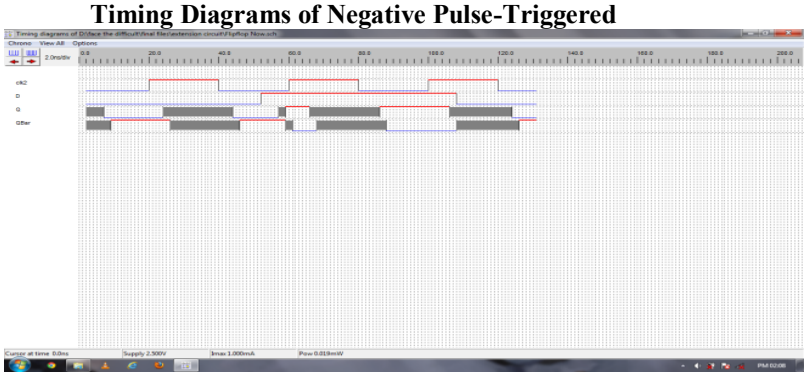
Power calculation of P-FF using Micro wind



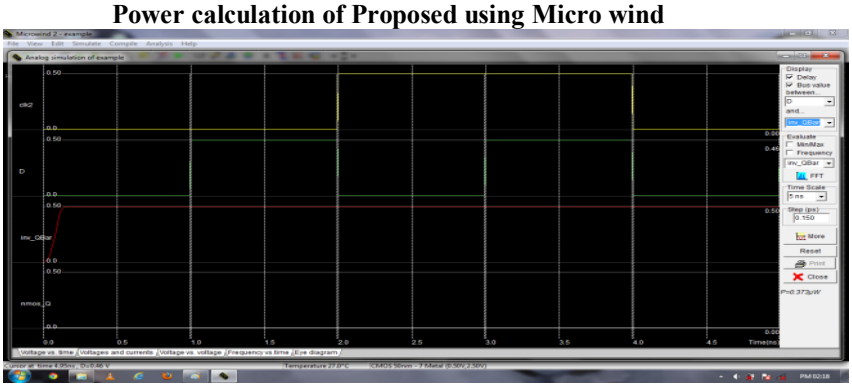
Proposed Negative Pulse-Triggered Flip-Flop schematic using DSch(Digital Schematic)



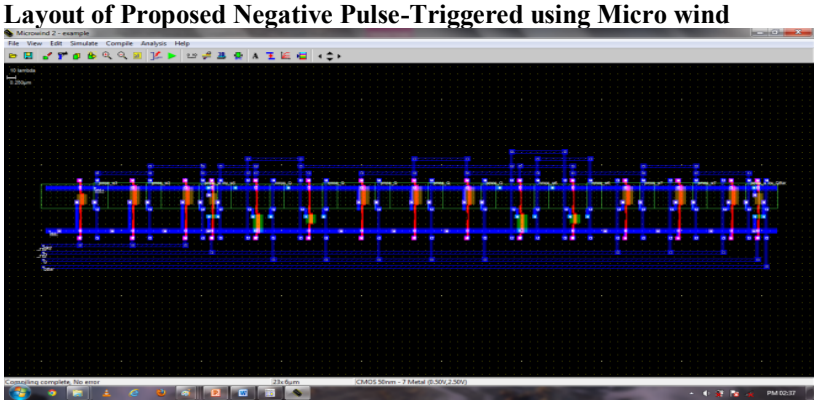
Timing Diagrams of Negative Pulse-Triggered



Power calculation of Proposed using Micro wind



Layout of Proposed Negative Pulse-Triggered using Micro wind



From the analysis, we achieved the following results

FLIP-FLOP	POWER CONSUMPTION
IP-DCO	14.4µw
MHLFF	0.51mw
SCCER	0.19mw
PULSE-ENHANCEMENT FLIP-FLOP	8.57µw
PROPOSED NEGATIVE PULSE-TRIGGERED FLIP-FLOP	0.373µw

IV. CONCLUSION

Hence when compared with conventional implicit type pulse triggered flip-flops, the proposed pulse-triggered flip-flop achieves the best power consumption circuit of power 0.373µw and number of transistors reduced to minimum quantity(5 transistors) excluding inverters. Hence this design can be treated as best flip-flop design in terms of power, area constraints

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