Comparative Analysis of CMOS ADC Topologies with Different Performance Parameters

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Abstract : *Analog to Digital Converters (ADCs) which are having importance in interface between analog and digital world are key design blocks and are currently adopted in many application fields to improve digital systems, which achieve superior performances with respect to analog solutions. This paper presents the comparative analysis of ADCs based on different performance parameters i.e. speed, technology used, power consumption, signal to noise ratio, bandwidth and dynamic & static characteristics. Various examples of ADC applications can be found in data acquisition systems, measurement systems and digital communication systems also imaging, instrumentation systems. The main aim of this paper is to provide comparison between different performance parameters for all ADCs & analyzing the better results & performance in future.*

Keywords: *Analog to Digital Converter, Flash, Sigma-Delta (∑ -Δ), Pipeline, Quantization, Sampling.*

1.   INTRODUCTION

An ADC produce a digital output that corresponds to the value of signal applied to its input relative to a reference voltage finite numbers of discrete values are 2n (where n is number of bits) resulting quantization uncertainty [4]. An ADC acts as a bridge between the analog and digital worlds. It is a necessary component whenever data from the analog domain, through sensors or transducers, should be digitally processed or when transmitting data between chips through either long-range wireless radio links or high-speed transmission between chips on the same printed circuit board [27].

The trend of achieving higher data throughput in both wires and wireless digital communication systems is continuous; this results in more and more demanding specifications on ADCs in terms of sampling rate and conversion accuracy. The challenge here is to achieve a high sampling rate and high conversion accuracy at the same time with low power dissipation in the presence of component mismatch, nonlinearity, and thermal noise. Component mismatch and nonlinearity are not fundamental limitations, and can be therefore overcome in a power efficient way by digital calibration at a cost of additional design complexity and extra power for the calibration circuits Furthermore, these digital calibration circuit benefits from CMOS scaling. In contrast to mismatch and nonlinearity, thermal noise is a fundamental limitation; as the circuit's fidelity relies on the relative contrast of the signal strength to that of thermal noise, measured by the signal-to-noise ratio (SNR), there is a strong trade-off between power dissipation and SNR if thermal noise is the main limitation Improving the voltage efficiency is then an effective way to improve the power efficiency for high-speed and high-resolution ADCs in advanced CMOS technology. Enabling the ADC to process a large input signal range allows reducing the capacitor size that determines the thermal noise. The reduction of the capacitors brings benefits such as smaller area, lower power dissipation, higher and width, and easier to drive. However, processing a large signal swing is normally constrained by the linearity of the input sampling stage, the amplifier's output stage, and further by the reference voltage [29].

This paper includes section 2 as history of ADC, which contains subsection 2.1 as architecture & working principle of basic ADC, subsection 2.2 as classification of ADC, 2.3 as parameters of ADC. Section 3 of the paper has comparative analysis of all ADC topologies with performance parameters in a tabulated form & then section 4 includes conclusion & future scope. And lastly the description of the paper references is given.

II.   HISTORY OF ADC

In Flash, successive approximation (SAR) & integrating converters are the three most widely used circuit topologies in the past, but in the last decade ADC architecture have progressed gradually. These devices have been replaced with the new ones, having reduced size, cost, and power consumption & also thousand times high conversion rate. From these improvements in the conversion rate characteristics, resolution, power, speed & cost of ADCs, provide more comfort ability in today's electronics systems. From the past usage in digital microprocessor system, they progressed from sampling rates of a few kHz up to several GHz, the resolution factor have reached to 24 bits [2].

1.1 Architecture of ADC

Fig. 1 [4] shows a block diagram of a general ADC. It consists of prefilter, sample and hold, quantizer and encoder blocks. A prefilter, called an antialisaing is necessary to avoid the aliasing of the higher frequency signals back into baseband of the ADC, which is followed by a sample-and-hold circuit that maintains the input analog signal to the ADC constant during the time this signal is converted to an equivalent output digital code [4] & [27].
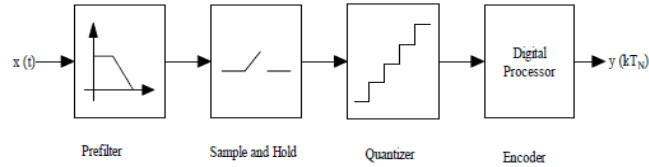

Fig. 1 Block diagram of General ADC [4]

$$\text{Digital Output Code} = \frac{\text{Analog Input}}{\text{Reference Input}} \times (2^n - 1) \qquad (1)$$

Sampling: Frequency which represents the continuous time domain signal at discrete & uniform time intervals. The maximum bandwidth of sampled ADC or reconstructed DAC signal from Nyquist frequency i.e. half of the sample exceeds the highest frequency of the sampled frequency [1] & [4].

Quantization: The process in which the analog sampled signal having an infinite resolution with digital finite resolution. It belongs a range of conversion (ΔVr), the number of bit combinations that convert output in possible states i.e. $N=2^n$, where n is the number of bits [1] & [4].

$$\text{Resolution Factor } (Q) = \frac{\Delta Vr}{N} \qquad (2)$$

The quantizer divides the reference into sub-ranges. Generally, there are 2N sub- ranges, where N is the number of bits of the digital output data. The quantization block finds the sub-range that corresponds to the sampled analog input. Consequently, the encoder i.e., digital processor in the block diagram encodes the corresponding digital bits. Within the conversion time, a sampled analog input signal is converted to an equivalent digital output code [4] & [27].The Nyquist frequency or rate which states that, sampling frequency must be at twice the bandwidth of the signal in order for the signal to be recovered from the samples. Fig.2 [1] shows the basic ADC with external references [1].
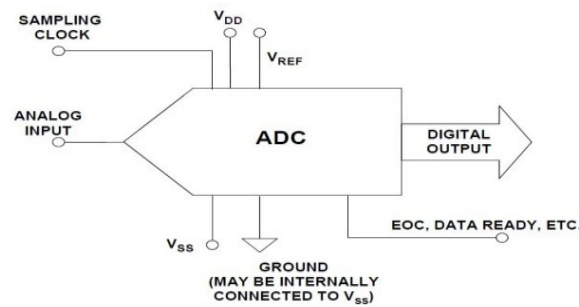

Fig.2 Basic ADC with external references

1.2 Classification of ADC

ADCs have a wide range of classification. The main converter topologies are in different fields: Flash, Pipeline, Sigma-Delta, & SAR as:

2.2.1 Pipeline ADC

A Pipeline ADC consists of a cascade of stages, each of which contains a low resolution ADC, DAC and amplifier, S&H. The sample and hold circuit basically samples the values and then holds the value at which further operations on the data is done. High-speed and medium-resolution ADCs are the vital elements in a wide variety of commercial applications including high-speed data conversion in communication systems, image signal processing and ultrasound front ends. In such applications, the reduction of power consumption associated with high-speed sampling and quantization is one key design issue in enhancing portability and battery operation. Among various ADC architectures, the pipeline converter is most suitable for high-speed and medium-resolution applications. A front-end track-and-hold amplifier (THA) prevents the multiplying digital-to-analog converter (MDAC) and stage ADC in the first pipeline stage from operating on different analog inputs due to skew; hence, significantly minimizing errors in the output's most significant bit for high-bandwidth

inputs. Proposed modified two-stage operational transconductance amplifier (OTA) is selected as basic building analog block for the functional blocks like THA and MDAC sections which reduces the power consumption of these functional blocks [15]. The block diagram of pipeline ADC is shown below in Fig.3 [2].
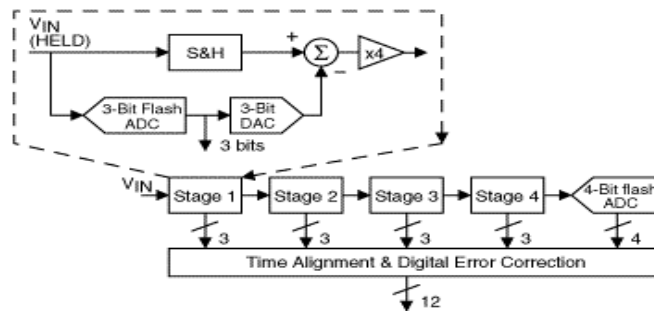

Fig.3 Block diagram of Pipelined ADC

2.2.2 Sigma-Delta (∑ -Δ) ADC

Sigma - delta converters are more commonly called as oversampling converters or charge balancing ADCs. ∑ - Δ ADC differ from other ADC approaches by sampling the input signals at a much higher rate than the maximum input frequency [27]. These converters are classified as ADC topology that provides highest resolution while still achieving high speed on the order of 24 bits at 1.5MHz. Oversampling & Noise shaping are the two key techniques employed in these ADCs [4].

Oversampling is the process of sampling a signal with a sampling frequency significantly higher than twice the bandwidth or highest frequency of the signal being sampled. Oversampling helps avoid aliasing, improves resolution and reduces noise. The sigma delta ADC oversamples the desired signal by a large factor & filters the desired signal band. Unlike the Nyquist rate converters, in oversampled converters each output is obtained from a sequence of coarsely quantized input samples [4].

Oversampling Ratio (OSR): The ratio of the sampling rate and the Nyquist rate is called the oversampling ratio. This oversampling can vary from 8 to 256. The resolution of the oversampling ADC is directly proportional to oversampling ratio. The bandwidth of input signal is inversely proportional to the oversampling ratio [4]. The block diagram of ∑ -Δ ADC is shown below in Fig.4 [27].
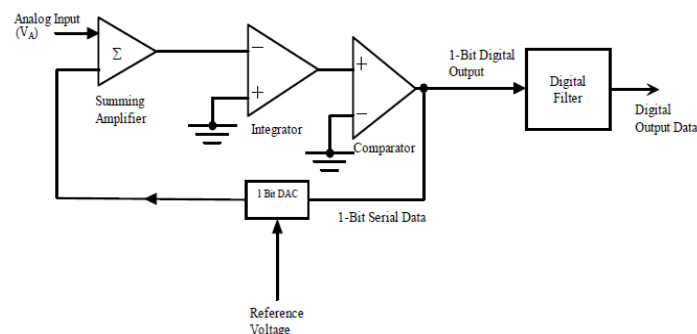

Fig. 4 Block diagram of oversampled Sigma Delta ADC

The oversampling interface requires some extra signal-processing steps: the analog signal is first converted to a high-speed, low-resolution digital signal, and then filtered and down sampled to a low-speed, high-resolution format. In oversampling converters, the output data depends on all previous samples, so they give a different result depending on the past history of the input signal. The oversampling converters are not memory less. A limitation of this architecture is its latency, which is substantially greater than that of the other types [27] – [28].

Delta - Sigma (Δ-Σ) modulation is a relatively simple means of performing data conversion. ΣΔ is the mathematical symbol for the summation of delta pulses and is read sigma-delta. Delta Modulation requires two integrators for modulation and demodulation as we seen in the Fig.5 [27]. Since integration is a linear operation, the second integrator can be moved before the modulator without altering the input and output characteristics. Now, the two integrators can be combined into a single integrator by the linear operation property. This arrangement is called Sigma-Delta Modulation [27] – [28].
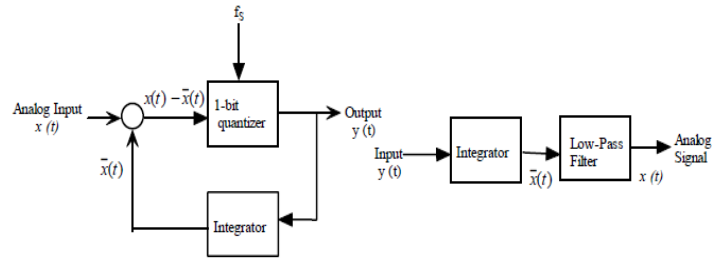
Fig. 5 Delta modulation & demodulation

2.2.3   Flash ADC

The highest speed of any type of ADC is parallel or flash converters. As shown in figure 4. Flash ADC uses one comparator per quantization level (2^N-1) and 2^N resistors. The reference voltage is divided into 2^N values, each of which is fed into comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators. A thermometer code exhibits all zeros for each resistor level if the value of VIN is less than the value on the resistor string, and ones if VIN greater than or equal to voltage on the resistor string. A simple 2^N-1: N digital thermometer decoder circuit converts the compared data into an N-bit digital word [26]. Why flash is needed in ADC because of high speed, resolution factor, dynamic performance and low power consumption. Flash can be implemented in silicon based BJT and CMOS rarely used in III-IV technologies. Recently for cost performance ratio flash using 50K channels in 12bit [4]. As shown below in Fig.4 [26].
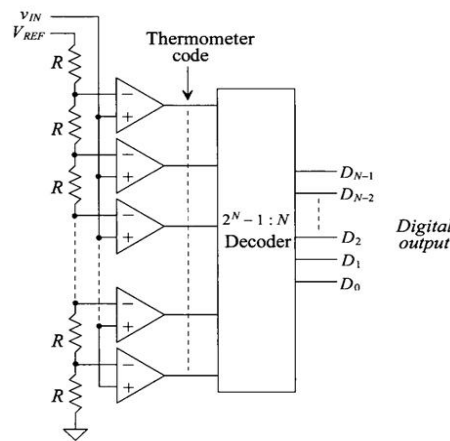

Fig.4 Block diagram of Flash ADC

The comparators, as the name suggests compares an analog signal with another analog signal and outputs a binary signal based on the comparison. The comparator can be thought of as a decision-making circuit. The comparator is widely used in the process of converting analog signals to digital signals. Since comparators are generally used in open loop mode, they can have very high open-loop gain. Comparators are generally classified as open-loop comparators and regenerative comparators. Open-loop comparators are basically operational amplifiers without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals [5]. Comparators using hysteresis it is the quality in which the input threshold changes as a input or output level [4], it is the difference between the input signal levels at which a comparator turns off and turns on. A small amount of hysteresis can be useful in a comparator circuit because it reduces the circuit's sensitivity to noise, and helps reduce multiple transitions at the output when changing state. There are many ways to introduce hysteresis in a comparator. All of them use some type of positive feedback. [5].

2.2.4   SAR ADC

The method of addressing the digital ramp ADC's shortcomings is the so-called successive approximation ADC. The only change in this design is a very special counter circuit known as a successive-approximation register (SAR). The approximation is stored in a successive approximation registers. SAR converter performs basically a binary search through all possible quantization levels before converging on the final digital answer [26]. SAR converters provide good resolution such as 16bits at 120MHz and speed characteristics without any trade off from latency or post processing. SAR is applicable for real time operation ADC that uses a comparator to successively narrow range that contains the input voltage at each successive step

the converter compares the input voltage to the output of the internal DAC which might represent the midpoint of a selected voltage range at each step in this process [3] - [4]. SAR ADC is the most suitable architecture for applications where reasonably high speed, low power consumption, low complexity and high resolution are needed. As shown below in Fig.5 [26].
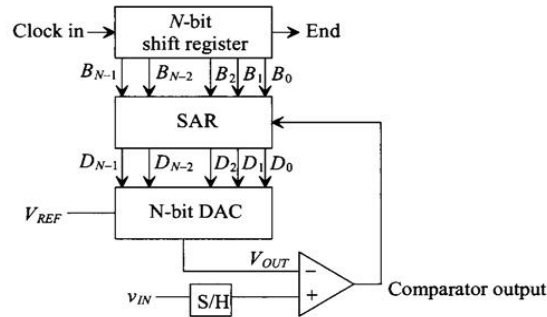

Fig.6 Block diagram of SAR ADC

1.3 Parameter of ADC

The parameters of an ADC can be broadly classified into static performance parameters and dynamic performance parameters. Static performance parameters are those parameters that are not related to ADCs input signal. Conversely, dynamic performance parameters are related to ADCs input signal and their effects are significant with higher frequencies .Major static parameters include gain error, offset error, full scale error and linearity errors whereas some important dynamic parameters include signal-to-noise ratio (SNR), total harmonic distortion (THD), signals to noise and distortion (SINAD) and effective number of bits (ENOB) [2] - [4].

1.3.1   DNL

Differential nonlinearity (DNL) is a measure of the separation between adjacent levels measured at each vertical jump. DNL measures bit-to-bit deviation from ideal output steps, rather than along the entire output range [1] & [4]. As shown below in Fig.7 [4].

2.3.2   INL

Integral nonlinearity (INL) is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically. INL can be expressed the percentage of the full scale range or in term of the LSB. The maximum +INL is 1.5 LSB and the maximum – INL is -1.0LSB [1] & [4].As shown below Fig.7 [4].
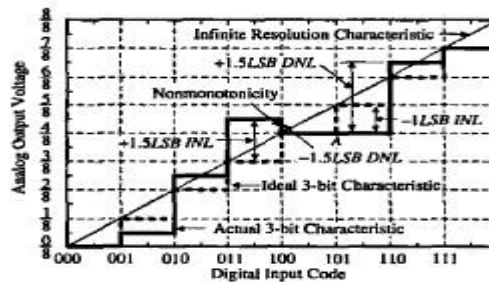

Fig.7 Characteristics of DNL & INL

2.3.3   SNR

Signal to Noise Ratio (SNR) is defined as the ratio of the full scale value to the rms value of the quantization noise. The rms value of the quantization noise can be found by taking the root mean square of the quantization noise. It does not include signal harmonics [4]. It can be given as:

$$SNR = \frac{vOUTrms}{FSR \, / 2^N \sqrt{12}}$$

(3)

Where, FSR is Full Scale Range [4].

2.3.4   OFFSET ERROR

It is a static conversion error in which a constant difference between the actual finite resolution characteristic and the finite resolution characteristic measured at any vertical jump, illustrated in below Fig.8 (a) [4].

2.3.5 GAIN ERROR

The gain error is the difference between the actual finite resolution and an infinite resolution characteristic measured at the rightmost vertical jump. Gain error is proportional to the magnitude of the DAC output voltage. This error is illustrated in below Fig.8 (b) [4].
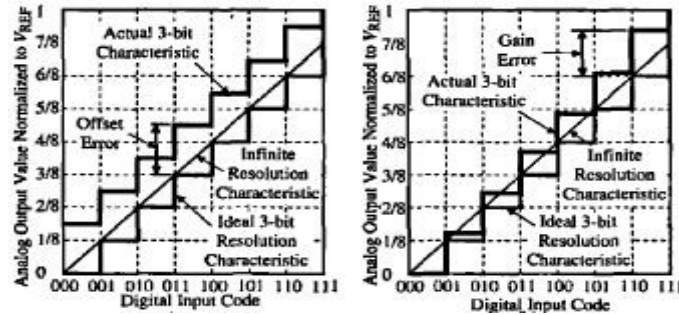

Fig.8 (a) Offset Error   (b) Gain Error

2.3.6 ENOB (Effective Number of Bits)

The effective number of bits can be defined as [4]:

$$ENOB = \frac{SNR_{actual} - 1.76dB}{6.02}$$

(4)

2.3.7 Dynamic Range (DR)

The ratio between the maximum signal amplitude that can be resolved without saturating the converter, and the minimum signal amplitude that can be resolved without being mistaken for noise [4].

2.3.8 SNDR

Signal-to-Noise-and-Distortion Ratio *(SINAD)*. The ratio of the rms signal amplitude (set 1 dB below full-scale to prevent overdrive) to the rms value of the sum of all other spectral components, including harmonics but excluding dc. SNDR is a measurement of the purity of a signal. It is given as [1].

$$SNDR = \frac{P_{signal}}{P_{quantization\ error} + P_{random\ noise} + P_{distortion}}$$

(5)

2.3.9 SFDR

Spurious-Free Dynamic Range (SFDR) is the parameter measures the difference between the power of the desired signal and the power of its highest harmonic or intermodulation products [28].

III. COMPARATIVE ANALYSIS

All the specified architectures of ADCs have some specialty in their own. Following is some survey data in tabulated form showing all types of ADCs considered above, having various performance parameters calculated by various authors for different applications:

TABLE 1: COMPARATIVE PARAMETERS OF FLASH ADC

References	Resolution/ Bandwidth	Speed	CMOS Technology	Power Consumption/ Supply Voltage	DNL / INL	SNDR / SFDR	ENOB	Remark
Ref. [6]	5 bit / 1GHz	3.5 Gsps	20μm	227mW / 1.4V	-0.83-0.93 / -0.89-0.88LSB	23.6dB/-	-	Comparator is used to improve regeneration speed, pre-amplification
Ref. [7]	4,5,6bit/ -	1to2 Gsps	65 nm	6mW / 1.2V	0.36 / 0.28LSB	29.5dB/-	4.6	TIQ comparator, inverters as a comparator for high speed & low power consumption.
Ref. [8]	5,6 bit / -	1.056 Gsps	0.18 μm	36mW / 1.8V	0.32/0.56	-	4.2	Differential amplifier comparator is used
Ref. [9]	5 bit / 800MHz	1.6 Gsps	0.13μm	180mW /1.2V	0.60 / 0.65LSB	27.12 / 35.80	4.20	Pre-amplifier based comparator is used to
Ref. [10]	5bit/600 MHz	3.2 Gsps	0.13μm	120 mW/1.2V	0.24 /0.39 LSB	-	4.54	Pre-amplifier based comparator is used to

TABLE 2: COMPARATIVE PARAMETERS OF PIPELINE ADC

References	Resolution/ Bandwidth	Speed	CMOS Technology	Power Consumption/ Supply Voltage	DNL / INL	SNDR / SFDR	ENOB	Remark
Ref. [11]	12 bit	20 Msps	0.53μm	56.3mW / 3.3V	1.47 / 7.05 to 0.2LSB	41.3 & 52.1 to 72.5 / 84.4dB	11.8 bit	With Interpolation-Based Nonlinear Calibration
Ref. [12]	10 bit	100 Msps	90 nm	- / 1.2V	-	-	-	With *In Situ* Background Clock-Skew Calibration
Ref. [13]	10 bit	100 Msps	0.13 μm	32.4mW / 1.2V	0.64 / 1.03LSB	56dB / -	-	Using Dynamic Memory Effect Cancellation Technique
Ref. [14]	10 bit	60 Msps	0.18 μm	13mW / 5mV (A / D)	0.73 / 1.44LSB	56.6 / 64.8dB	-	With Split-Capacitor CDS Technique
Ref. [15]	10 bit	100 Msps	180 nm	52.6 mW / 1.8 V	+0.6167/- 0.3151LSB / +0.4271/- 0.4712LSB	58.72 & 57.57 dB / 65 / 62 dB	9.5 / 9.27 bit	Low power ADC with systematic design approach

TABLE 3: COMPARATIVE PARAMETERS OF SIGMA DELTA ADC

References	Resolution/ Dynamic Range	Speed	CMOS Technology	Power Consumption/ Supply Voltage	Bandwidth / Clock Frequency	SNDR / SFDR	SNR / OSR	Remark
Ref. [16]	14 bit / 85 dB	5 Msps	0.25μm	50 mW / 2.5 V	2.5 MHz / 60 MHz	80.5 / 98.4 dB	81 dB / 12	Continuous Time Δ - ∑ ADC
Ref. [17]	12 - 15 bit / -	1 Gsps	0.18μm	950 mW / 1.8 V	50 - 62.5 MHz / -	76 dB / 81.79 dB	- / 8	ADC with Residue Averaging Technique
Ref. [18]	16 bit / -	2.5 MHz	0.5μm	270 mW / 1.2 V	1.25 MHz / -	- / 102 dB	90 dB / 8	Cascaded multibit Δ - ∑ ADC for wire line communication & high speed instrumentation
Ref. [19]	≥15 bit / ≥95 dB	-	0.18μm	9 mW / 1.8 V	2 MHz / 64 MHz	82 dB / -	- / -	Low power highly digitized bandpass ∑ - Δ ADC
Ref. [20]	16 bit / 97 dB	2.5 Msps	0.65μm	295 mW / 5 V	- / 60 MHz	89 dB / -	95 dB / 24	High performance multibit ADC with Data Weighted Averaging

TABLE 4: COMPARATIVE PARAMETERS OF SAR ADC

| References	Resolution/ Bandwidth	Speed	CMOS Technology	Power Consumption/ Supply Voltage	DNL / INL	SNDR / SFDR	ENOB	Remark
Ref. [21]	10 bit / -	1 Ksps	0.13μm	53nW / -	0.54 / 0.45LSB	56.7 / 67.6dB	9.1 bit	For Medical Implant
Ref. [22]	8 bit / -	80 Ksps	0.18μm	- / 1V	0.70 / 1.5LSB	53.28 / 61.1dB	-	-
Ref. [23]	10 bit / -	40 Msps	65 nm	1.21mW / 1.1V	- / -	55.1 / 71.5dB	8.9 bit	-
Ref. [24]	12 bit / -	50 Msps	65 nm & 90 nm	- / -	- / -	66dB & 65.6dB / 78dB & 77dB	10.4 bit	SAR Assisted Two-Stage Pipeline ADC
Ref. [25]	10 bit / -	64 kHz	0.18μm	6.2 mW / 1.8 V	- / -	- / -	- / -	Using a offset biased auto zero comparator
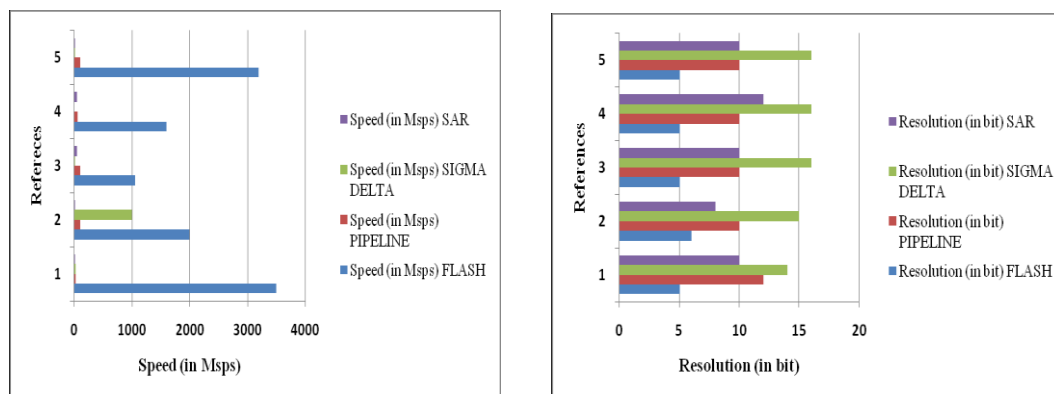
Fig.9 Comparative Analysis of ADCs (a) Speed of all ADCs   (b) Resolution of all ADCs
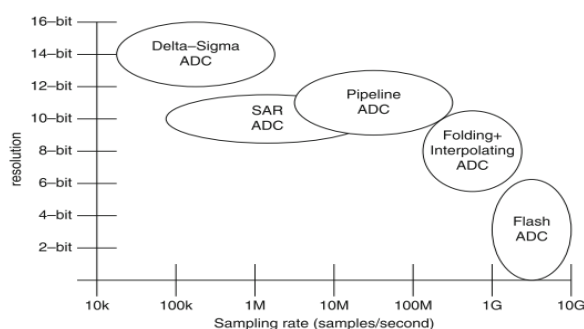
(c) Comparative Analysis of all ADCs [30]

The plots in Fig.9 (a) & (b) show the comparative analysis of speed (sampling rates) & resolution of all types of ADC topologies respectively & the combination of Fig.9 part (a) & (b) is the part (c), showing the speed Vs resolution graph for each ADC.

IV. CONCLUSION & FUTURE SCOPE

This comparative analysis of different ADC architectures is given considering many parameters. The comparison tables show that as the CMOS technology is reduced, the performance of the ADC will be better; for each type of ADC. Also it is clear from the table that for high speed applications Flash ADC is a perfect solution, which in turn gives lower resolution. While Σ-Δ ADC provides highest resolution among all ADCs but on lesser sampling rate. Also the SNDR is higher in Σ-Δ ADC. Pipeline ADC is very much useful for medium speed applications, also with medium resolution, though higher than Flash & SAR ADCs. On the basis of these conclusions the Fig. 9 (c) [30] shows the clear view of performance of all ADC topologies. This comparative analysis of different parameters teaches all the parameters needed to design a ADC. This data provides easy to work on any ADC topology. So, according to this gathered parameters it is more convenient to work on ADCs & helpful to implement much better performing ADCs in future.

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