IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 3, Issue 1 (Sep. – Oct. 2013), PP 29-35
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Low Power SAR-ADC in 0.18µm Mixed-Mode CMOS Process for Biomedical Applications

RVNR Suneel Krishna[1], Jyothirmayi[2]
M.Tech ,Embedded systems[1], Associate professor,Dept.of ECE[2]
Geethanjali College of Engineering and Technology, Rangareddy Dist, A.P, India-50130

***Abstract**: This paper presents an energy efficient successive-approximation-register (SAR) analog-to-digital converter (ADC) for biomedical applications.For low-power applications designer needs to come up with a compromise among speed, resolution and speed power.To reduce energy consumption, a charge redistribution technique is used along with auto zero technique for comparator offset cancellation.The power consumptions of the capacitive digital-to-analog converter (DAC), latch comparator, and digital control circuit of the proposed ADC are lower than those of a conventional SAR ADC.ADC is designed in 0.18µm CMOS technology in such a way that the total power is minimized while medium sampling rate and 8 bit resolution are achieved.*
***IndexTerms:** Analog-to-digital converters (ADCs), CMOS analog integrated circuits, low power, offset,autozero,low supply voltage, successive approximation.*

I. Introduction

In the last few years, there has been a growing interest in the design of wireless sensing device for portable, wearable or implantable biomedical applications. These sensing devices are generally used for detecting and monitoring biomedical signals such as electrocardiographic (ECG), electroencephalography (EEG), and electromyography (EMG), to name a few. Most biomedical signals are often very slow and exhibit limited dynamic range. A typical biomedical sensor interface consists of a band-pass filter, a low-noise amplifier and an analog-to-digital converter (ADC). The digitalization of the sensed biomedical signals is usually performed by ADCs with moderate resolution (8–12 bits) and sampling rate (1–1000kS/s). In such devices, energy efficiency and long battery life are paramount design goals. Particularly, ADCs for implanted medical devices need microwatt operation to run on a small battery for decades. Therefore, energy efficiency is a critical challenge for ADCs design.battery life are paramount design goals. Particularly, ADCs for implanted medical devices need microwatt operation to run on a small battery for decades.Therefore, energy efficiency is a critical challenge for ADCs design. Successive approximation register (SAR) ADC has the advantage of power efficiency compared with other ADC architectures (e.g., pipelined ADC). Furthermore, SAR ADC benefits from technology downscaling because of two major reasons:(1) SAR ADC mainly consists of digital circuits which get faster in deep sub-micron technologies; and (2) SAR ADC is an opamp-free architecture. In other words, SAR ADC does not require high gain and high bandwidth opamps to guarantee the linearity.A high-performance opamp consumes large power, and suffers from short channel effect and low supply voltage in advanced process nodes. These reasons arouse the interest of designers which is reflected in the number of recent publications.SAR ADCs are commonly used in biomedical acquisition systems due to their low power consumption and simplicity,particularly for simple analog sub-circuits.The comparator and sampling switches are the only two analog components..

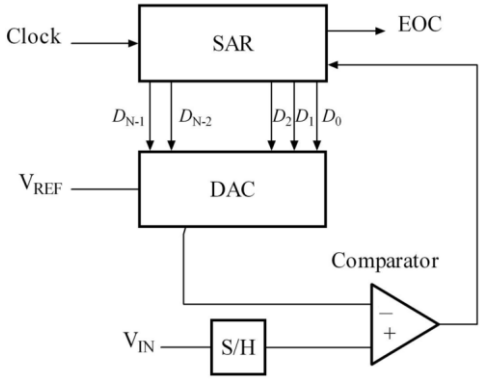

Fig. 1. Overall system Architecture of SAR-ADC

The overall system architecture is shown in "Fig.1". We designed and implemented all the blocks of SAR-ADC and results are validated using CADENCE Virtuoso Analog Design Environment IC 6.1.5 tool.

II. Converter Principle

Successive Approximation Converter based on a Charge Redistribution Principle is characterized in "Fig. 2". Binary weighted capacitors are used for the DAC. The switching point of the comparator is independent of the value of the input signal. During conversion, at the comparator input positive and negative voltages VC referred to analog ground occur, whose magnitude is continuously decreasing with the number of conversion steps performed within a complete conversion cycle. Consequently, at the end of the conversion cycle, i.e., when highest precision is demanded, both comparator inputs are operated near analog ground [1].

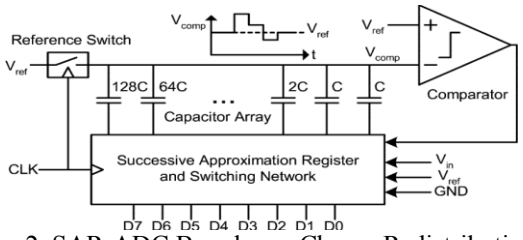

Fig. 2. SAR-ADC Based on a Charge Redistribution Principle

III. The Sample & Hold Circuit Design

The Sample & Hold circuit is completely passive. It contains just a sampling switch, a dummy switch, a sampling capacitor and two clock buffers "Fig. 3". The passive S/H circuit gives a simple solution to the requirements of both small offset and wide input bandwidth of the SA-ADC to be used in an ADC array [2].

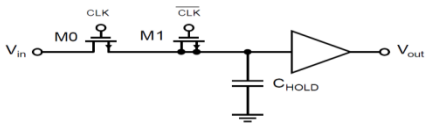

Fig. 3. Passive Sample & Hold Circuit

In this architecture "Fig.3", one dummy switch is used to minimize clock feed through error [3]. The theory behind this technique is that if the width of M1 is one half of M0 transistor, and clock wave form is fast enough then charge will cancel. The "Fig.4", shows the schematics of Sample and Hold circuit. The value of holding capacitor is 1pF. Where transistor M0 operating in linear region, the condition for operating in linear region is

$$V_{GS} > V_T \quad (1)$$

$$V_{DS} < V_{DSAT} = V_{GS} - V_{TH} \quad (2)$$

$$I_{DS} = K' \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) V_{DS} \quad (3)$$

Where,

$K' = \mu_N C_{OX}$, V_{GS}=Gate Source Voltage

$I_{DS} = K' \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) V_{DS}$ (3)

V_{DD}=Supply Voltage, V_T=Threshold voltage

$$g_m = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_{TH}) \quad (4)$$

The calculated value of W/L for M0 & M1 is given in
Table I the "Fig.5", shows the simulation result of S&H circuit "Fig.4".

Table I: Aspect Ratio Of Sample & Hold Circuit

Transistor	W	L
M0	2u	0.5u
M1	1u	0.5u

III. Capacitor Array Dac

The Binary weighted Capacitor DAC or Charge scaling DAC architecture is as shown in "Fig.6".In this architecture, a parallel array of the binary weighted capacitors is connected [3],[8]. The voltage output, VOUT, can be expressed as relation (6)

$$V_{OUT} = KV_{REF}D \qquad (6)$$

Where, VOUT is the analog voltage output, VREF is the reference voltage, K is a scaling factor and the digital word D is given by relation (7)

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N} \qquad (7)$$

N is the total number of bits of the digital word, and bi is the ith coefficient and is either 0 or 1. The relation (8) gives the value of VOUT for any digital word.

$$V_{out} = \frac{C_{eq}}{(2C - C_{eq}) + C_{eq}} \times V_{ref} \qquad (8)$$

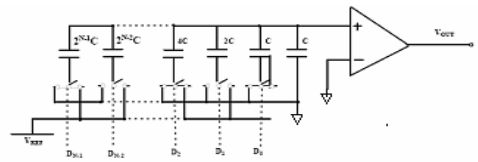

Fig. 6 Architecture of Charge Scaling DAC

We have implemented the architecture shown in "Fig.6" using CMOS capacitors and transistor switches as shown in
"Fig.7", which is simulated using CADENCE Analog Design Environment.The values of capacitors CMSB……..CLSB are used as a multiple of unit capacitor of 20fF. Here we are assuming the unit capacitance is 20fF.
The calculated values of all capacitors are given in Table II.

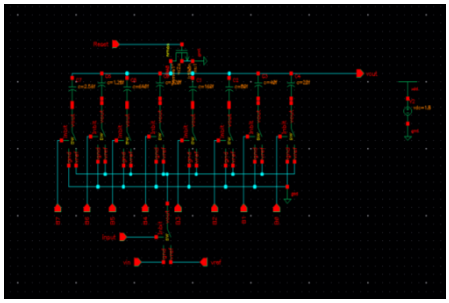

Fig. 7. Schematic of Charge scaling DAC

IV. Dac Switch Design

This design is used to reduce charge injection and clock feed through errors by complimentary PMOS and NMOS switches shown in "Fig.8". All MOS transistors are operating in linear region [4], [5].The "Fig. 8" shows a unit capacitor connecting to VREF when bit-1 is set (High).

TABLE II
Dac Switches Sizes And On Resistances

For 0.18µm Technology								
capacitor	C7(MSB)	C6	C5	C4	C3	C2	C1	C0(LSB)
capacitor value	2.56pF	1.28pF	640fF	320fF	160fF	80fF	40fF	20fF
NMOS/PMOS Switch in um	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18	0.27/0.18
RON (NMOS)	2.04K	2.04K	2.04K	2.04K	2.04K	2.04K	2.04K	2.04K
RON (PMOS)	2.96K	2.96K	2.96K	2.96K	2.96K	2.96K	2.96K	2.96K

Switch-1 PMOS, NMOS combination goes ON and connects to VREF.

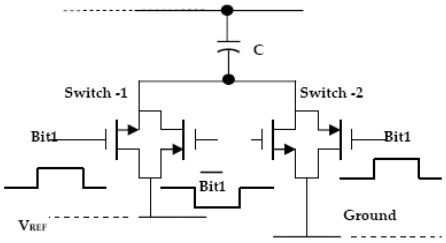

Fig. 8. DAC Switch architecture

Switch-2 PMOS, NMOS combination goes ON and connects to ground when bit-1 is reset [4], [6]. We have calculated the W/L of switch transistors and is given in Table II.

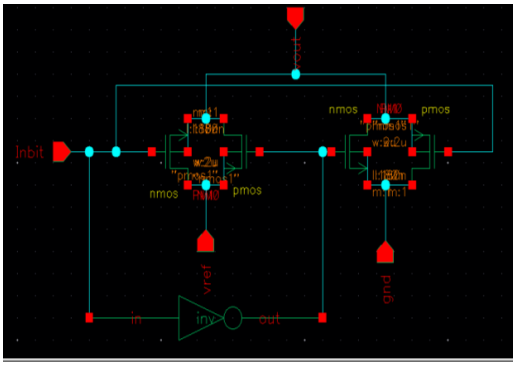

Fig. 9. Schematic of DAC switches

The "Fig. 9" shows implementation of DAC switch. The
RON resistance of PMOS and NMOS transistor can be calculated using relation (9).

$$R_{ON} = \left[K` \frac{W}{L}(V_{GS} - V_T)\right]^{-1} \qquad (9)$$

The Charge Scaling DAC is simulated in 0.18um CMOS process. The threshold voltages are 0.327 V for the nMOS and -0.4064V for the pMOS device. It is observed that a value of DNL is ±0.7*LSB* and INL is ±0.8*LSB* respectively.

V. Comparator

The comparator is designed as a simple regenerative resettable circuit "Fig. 12", [1], [8] followed by inverters for signal level recovery. This type of comparator is use positive feed back bi-stable element to compare two signals. The advantage of this circuit is that there is no steady state power consumption. The only current will be the one required by bias circuit. The design approach is based on slew rate and optimum propagation delay constraints. Apart from offset related issues, the comparator is working as expected. The bias current can be controlled by the bias transistor is as shown in "Fig.13", both transistor M2 and M3 is operating in saturation region and drain current of M2 and M3 can be given by equation (10)

$$I_{DS} = \frac{K^{'}W}{2\ L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \qquad (4)$$

We have assumed 2uA bias current to calculate the W/L ratio of the transistor M2 & M3.The aspect ratios of transistor M2 & M3 given in Table III. The complete schematic of comparator is as shown in "Fig.12".

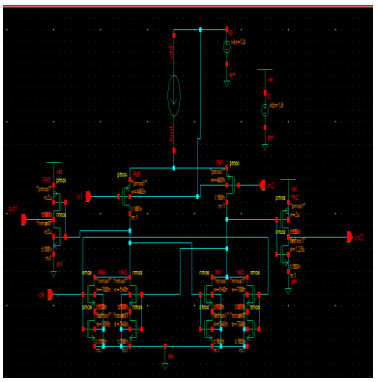

Fig. 12. Schematic of Regenerative Comparator

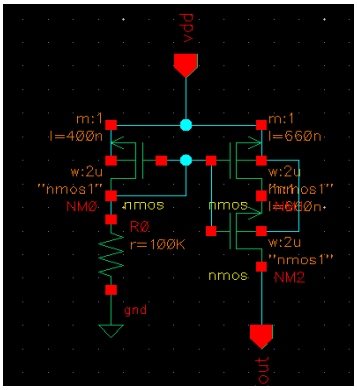

Fig. 13 Schematic of biasing current source

The current ID or bias current split in to ID1 and ID2 which flows through M4 and M5 respectively in differential pair transistor. This two current are depends on Vin1 and Vin2 which can be expressed as relation (11).

$$I_D = 0.5I_D + 0.25K \cdot \frac{W}{L} - \Delta V^2 \qquad (11)$$

Where $\Delta V = V_{in1} - V_{in2}$

TABLE III

TRANSISTOR SIZE

Circuit	MOS	W	L
Bias Current Source	M2	2u	0.4u
	M3	0.33u	0.4u
Differential Pair	M4	0.4u	0.18u
	M5	0.4u	0.18u
Switches	M6.M7	0.35u	0.18u
	M8,M9	0.27u	0.18u
Inverter	PMOS	3u	0.18u
	NMOS	0.23u	0.18u

The Auto zero technique

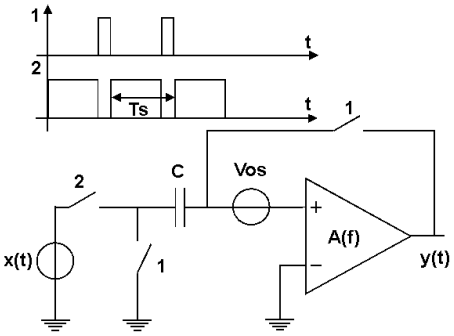

Fig.14: The auto zero technique

The auto zero technique reduces the offset and low frequency noise based on sampling methods [9]. This method has been extensively used in the past for offset reduction in comparators and amplifiers [4]. Most of the nowadays A/D converters with offset cancellation make use of auto-zeroed comparators. Fig.14 illustrates the principle of an auto zero amplifier. In the phase 1 of the clock, the sampling phase, the offset and the flicker noise of the amplifier configured as a buffer is sampled on the capacitor C. The output y(t) is actually the offset voltage V_{OS} as long as the open loop gain of the amplifier A_{OL} is large:

$$y(t) = -\frac{1}{1-\frac{1}{A_{ot}}} V_{os} \qquad (12)$$

$$y(t) \cong A_{OL}\left[x(t) - \frac{V_{OS}}{A_{OL}}\right] \qquad (13)$$

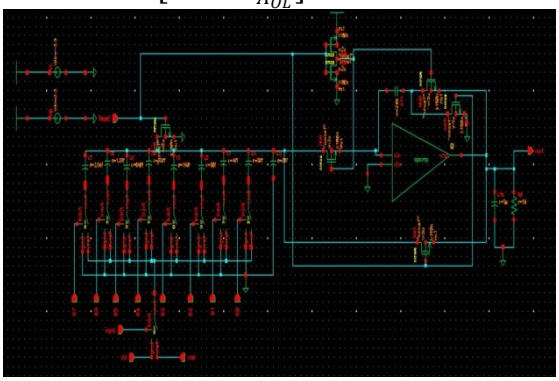

Fig.15: Implementing auto zero technique

VI. Sar Logic Design

A successive approximation register (SAR) is a digital control circuit, which is implemented using D flip-flop. We have designed D flip-flop using Verilog-A code. It has a parallel world output, which is connected to the input of an nbit D/A converter. The input of the SAR is a one bit digital signal, which is taken from the output of the comparator. To start the conversion, MSB in the SAR is set to 1 and all the other bit are set to 0. If the input is higher than the output of DAC then MSB of the SAR is set to d0=1 other wise d0=0.The content of SAR is changed to [d0 1 0…….0] in the second step, and [d0 d1 1 0….0] in the third step. The procedure of the successive approximation is continued until the desired accuracy is reached. The classic SAR algorithm flow chart is as shown in "Fig. 17" and the logic diagram of successive approximation register is shown in "Fig.16".

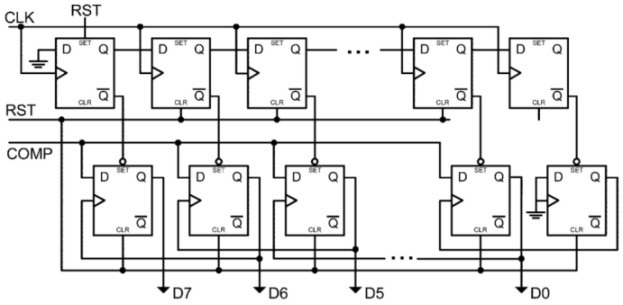

Fig. 16. Logic diagram of successive approximation register

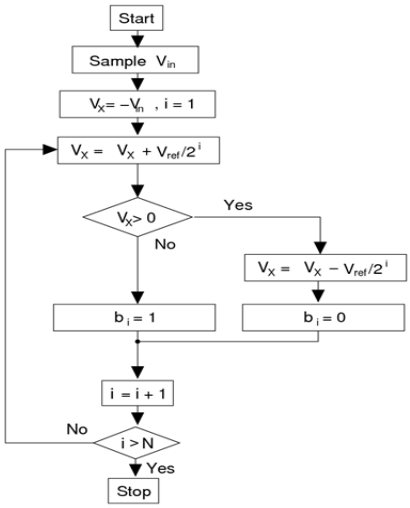

Fig. 17. SAR algorithm flow chart

VII. Conclusion

A successive approximation converter suitable for operation at low supply voltage is designed in a standard 0.18um MOS technology. We design all the building blocks of SAR-ADC using transistors with threshold voltages of approximately 0.327V for NMOS and – 0.4064 for PMOS. The simulation results indicate that the circuit achieves 8-bit monotonic conversion at high speed with differential nonlinearity less than 1 LSB. This device is suitable for standard CMOS technology VLSI implementation. These results are validated using CADENCE mixed signal Virtuoso Analog Design Environment IC (6.1.4/6.1.5) tool.

References

[1] Jens Sauerbrey, Doris Schmitt-Landsiedel, Roland Thewes, "A 0.5V, 1µW Successive Approximation ADC", *IEEE Journal of Solid State Circuit, IEEE 2002.*
[2] Jiren Yuan and Christer Svensson," A 10-bit 5-MS/s Successive Approximation ADC Cell Used in a 70-MS/s ADC Array in 1.2-pm CMOS", *Ieee Journal Of Solid-State Circuits, Vol. 29, No. 8, August 1994.*
[3] David A. Johns and Ken Martin ,"*Analog Integrated Circuit Design*"2nd Ed. 2002 John Wiley & Sons(ASIA) Pvt. Ltd. Singapore.
[4] P. E. Allen, Holberg, *CMOS Analog Circuit Design* (New York Oxford Uni. Press.2004)
[5] Jens Sauerbrey, Doris Schmitt-Landsiedel, Roland Thewes, "A 0.5V, 1µW Successive Approximation ADC", *IEEE Journal of Solid State Circuit, IEEE 2002.*
[6] National Semiconductor Article – ABC's of ADC's by Nicholas Gray, November 24 2003.
[7] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900mV 40µW Switched Opamp ΔΣ Modulator with 77dB Dynamic Range", *ISSCC Digest of Technical Papers*, pp. 68-69, p. 414, 1998
[8] R. J. Baker, Li H. W., D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation* (IEEE Press)
[9] F. Maloberti: "Data Converters"; Springer-Verlag, 2007, ISBN 9780387324852.

Biography

RVNR Suneel Krishna was born in Vijayawada, A.P, India. He received B.Tech in Electronics and Communication Engineering from Vivekananda Institute of Engineering and technology, *Rangareddy Dist, A.P*, India. Perusing M.Tech in Embedded Systems at Geethanjali College of Engineering and technology A.P, India.

S.Jyothirmaye was born in Warangal district, A.P, India. She is working as an Associate Professor in Electronics and Communication Engineering in Geethanjali College of Engineering & Technology, A.P, India. She received her Masters Degree in Embedded Systems from Holy Mary Institute of Technology and Sciences, under JNTUH, A.P, India. She completed her B.E. in Electronics and Communication Engineering from MIT, Manipal under MAHE University, India. He has 08 years of Teaching Experience and her interesting fields are low power VLSI Signal Processing, Communications and Signal Processing.