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Design a Low Power Half-Subtractor Using .90µm CMOS Technology

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Abstract: *In this paper we are presenting a Half-Subtractor using Adaptive Voltage Level (AVL) technique consuming less power than the conventional one .The main objective is to design that half subtractor using either of the two adaptive voltage level(AVL) techniques to reduce the sub threshold leakage current which plays a very important role in the reduction of power dissipation. We can bring down the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology in which the ground potential is increased and AVLS (adaptive voltage level at supply) in which supply potential is raised. Also the reduced transistor count add to the further lowering of power consumption of the realized Half-Subtractor circuit which is optimized at .90 micron technology using AVL technique. The AVL technique based Half-Subtractor compared to conventional one based on power consumption, speed, layout area and propagation delay is more preferred. The circuit is simulated on microwind and DSCH in .90 micron CMOS technology.*
Keywords*- Half-Subtractor, AVL techniques, DSCH, microwind simulator, VLSI circuit and low power*

I. Subtractor

Basically a subtractor is a digital circuit that performs subtraction of numbers or one could possibly say that it performs one of the four basic binary operations. In many computers and other kinds of device processors, subtractors are used not only for the arithmetic calculations, but are also frequently used in other parts of the processor, where there is a requirement of calculating addresses, table indices, and similar operations. And most importantly, many a times may also be used as an Attenuator.

Although subtractors can be constructed for many binary code representations, such as excess-3 or gray code or even binary-coded decimal, the most common subtractors operate on binary numbers. While performing subtraction between the two given numbers, two's complement or ones' complement is very commonly used to represent the negative numbers. Also due to the ease with which calculations are performed, many a times modifying an adder into an adder–subtraction is considered comparatively important. Other signed number representations require a more complex subtractor.

Depending upon the application of the device or upon the purpose of the application to be performed, the inputs to the circuit device may vary from two to three. We could possibly use an Half-Subtractor if we have two inputs while for three inputs, a Full-Subtractor can be used.

If we look at the working of the Full-Subtractor, the subtraction of the two given binary numbers may be carried out by taking the complement of the subtrahend and then adding it to the minuhend. By this method, the subtraction operation may also be converted to an addition operation requiring full adders for its machine implementation. Now in an another method of subtracting the numbers in which the subtraction on the logic circuits is performed in a direct manner, each subtrahend bit of the number is subtracted from its corresponding significant minuhend bit to form a different bit. If the minuhend bit is smaller than the subtrahend bit, a 1 is borrowed from the next more significant position.

Therefore if we can describe the whole process as follows: the Full-Subtractor basically performs subtraction process on two bits, a minuend and a subtrahend, and also takes into consideration whether a '1' has been borrowed by the previous adjacent lower minuend bit or not. As a result, there are three bits to be handled at the input of a Full-Subtractor, namely the two bits to be subtracted and a borrow bit designated as B_{in}. There are two outputs, namely the Difference output D and the Borrow output B_o. The Borrow output bit tells whether the minuend bit needs to borrow a '1' from the next possible higher minuend bit.

The Boolean expression for the two output variables are given by the equations

$D = A'B'B_{in} + A'BB_{in}' + AB'B_{in}' + ABB_{in}$

$B_o = A'B'B_{in} + A'BB_{in}' + A'BB_{in} + ABB_{in}$

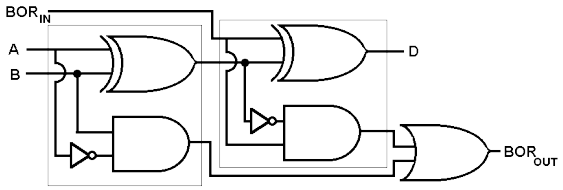

Figure 1 – Logic Symbol of Full-Subtractor

	Inputs			Outputs	
Line	Minuend (*A*)	Subtrahend (*B*)	Borrow in (*Bin*)	Difference	Borrow out (*Bo*)
1	0	0	0	0	0
2	0	0	1	1	1
3	0	1	0	1	1
4	0	1	1	0	1
5	1	0	0	1	0
6	1	0	1	0	0
7	1	1	0	0	0
8	1	1	1	1	1
	A – B – Bin			*Di*	*Bo*

Table 1 – Truth Table of Full-Subtractor

II. Conventional Half-Subtractor Circuit

A conventional Half-subtractor circuit is a combinational circuit that can be used to subtract one binary digit from another to produce a Difference output and a Borrow output. The Borrow output here specifies whether a '1' has been borrowed to perform the subtraction. The Half-Subtractor at the gate-level can be shown as follows in Figure 2 while the Table 2 gives us the truth table of the Half-Subtractor which is obtained from the binary arithmetic operations.

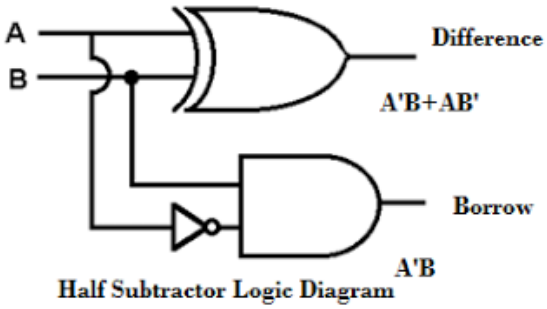

Figure 2 – Logic Symbol of Half-Subtractor

Inputs		Outputs	
Minuend *A*	Subtrahend *B*	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0
A – B		*Di*	*Bo*

Table 2 – Truth Table of Half-Subtractor

The Boolean expression for the two output variables are given by the equations

$D = A'B + AB'$
$B_o = A'B$

III. Transistor Level Half-Subtractor

The same conventional Half-subtractor can be formed using CMOS transistors and the whole transistor circuit consist of 16T (Transistor) in which 8TPMOS (Positive channel Metal Oxide Semiconductor) and

8TNMOS (Negative channel Metal Oxide Semiconductor) are used. The Half-subtractor at the transistor level can be shown in Figure 3 where we have two inputs Minuend bit (A) and Subtrahend Bit (B) and two outputs Difference Bit (D) and Borrow Bit (B_O).

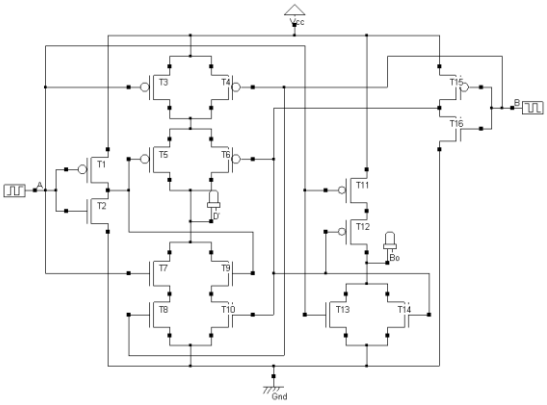

Figure 3 – Transistor level Half-Subtractor Circuit

In Conventional Half-Subtractor, when we design the circuit in the Microwind software, we obtain the value of power consumption of about 18.539µW which is a very large value and may lead to heating of the system. To reduce the heating, the power consumption has to be reduced and this can be achieved by either of the two schemes. One is AVLS (Adaptive Voltage Level at Supply) in which the supply voltage is reduced and the other one is AVLG (Adaptive Voltage Level at Ground) in which the ground potential is increased.

IV. Half-Subtractor Using Adaptive Voltage Level (Avl) Control Circuit

An adaptive voltage level control circuit can be used either at the upper end of the cell to bring down the supply voltage value (AVLS scheme) or at the lower end of the cell to lift the potential of the ground node (AVLG scheme). The effect of these two techniques on the power consumption is described in the following section.

A. Power Control using AVLG

A Half-Subtractor incorporating AVLG scheme is shown in Figure 4. The full switch provides 0 Volt at the ground node during the active mode while 1 Volt during the inactive mode at the ground node. An increase in virtual ground voltage reduces the gate-source and gate-drain voltage of transistor T8 and also the gate-drain voltage of transistor T10, which results in reduction of the power consumption on a whole, though not much improvement is observed in gate-source and gate-drain voltage of transistor T7 and T9.

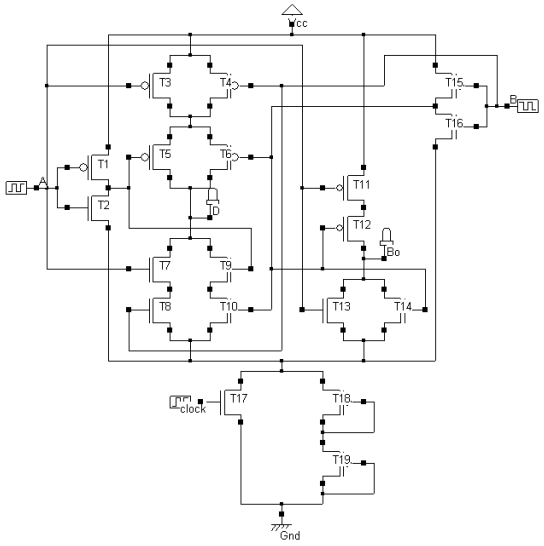

Figure 4 – Half-Subtractor using AVLG Technique

Incorporation of AVL Technique allows the decrease in power consumption through an added gate T17 in the AVL switch. The gate T17 is n-mos in nature. Therefore, this approach is useful in lowering the final value of the power consumption.

Table 3 gives us the truth table of the Half-Subtractor in AVLG Technique and Figure 5 gives us the logic symbol of the resultant Half-Subtractor.

A	B	D	Bo
0	0	X	X
0	1	1	1
1	0	X	X
1	1	0	0

Table 3 - Truth Table of the Half-Subtractor in AVLG Technique

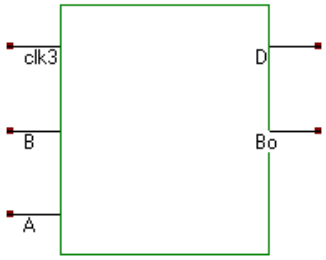

Figure 5 – Logic Symbol of the Half-Subtractor using AVLG Technique

B. Power Control using AVLS

Figure 6 shows the schematic of a Half-Subtractor in which AVLS scheme is applied. In this scheme, a full supply voltage of V_{cc} is applied to Half-Subtractor in Active mode while a Lowered or reduced supply voltage of V_{cc} is applied in Active Mode. Now the transistors T1, T3, T4, T11, T15 are at V_{cc} and in ON state. A decrease in gate-source voltage and gate-drain voltage is observed in transistors T3, T4 which is the major source of reduction in power consumption of the whole circuit. Furthermore an additional loss in power consumption of the circuit is observed due to the reduction observed in drain voltages in transistors T2, T3, T6. Hence, this approach is more successful in lowering the value of the total power usage involved in the Half-subtractor circuit than the AVLG approach. Table 4 gives us the truth table of the Half-Subtractor in AVLG Technique and Figure 7 gives us the logic symbol of the Half-Subtractor with an AVLS switch.

A	B	D	Bo
0	0	0	0
0	1	X	X
1	0	1	0
1	1	0	0

Table 4 – Truth Table of the resultant Half-Subtractor

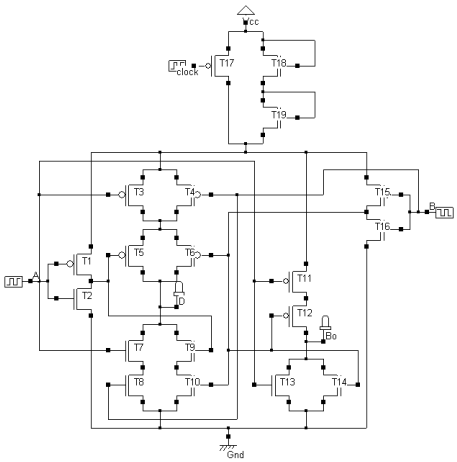

Figure 6 – Half Subtractor using AVLS Technique

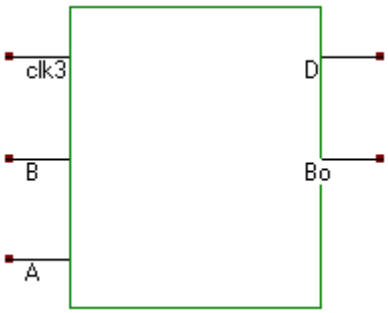

Figure 7 – Logic Symbol of the Half-Subtractor using AVLS Technique

V. Simulation Results

A binary Half-Subtractor subtracts two input bits and gives two output bits with one of them determining the difference (D) of the two input bits while the other giving the borrow bit (B_o). We design a Transistor level Half-Subtractor Circuit using the Dsch software and on obtaining its verilog file through the same software, we compile the obtained circuit design in the microwind software where then on compiling the circuit we may run its simulation hence obtaining the required appropriate results. On applying either of the two techniques on the conventional Half-Subtractor using 90 nanometre technology, we obtain low resultant power consumption value. We observe drop in power values which can be easily portrayed in the form of waveforms.

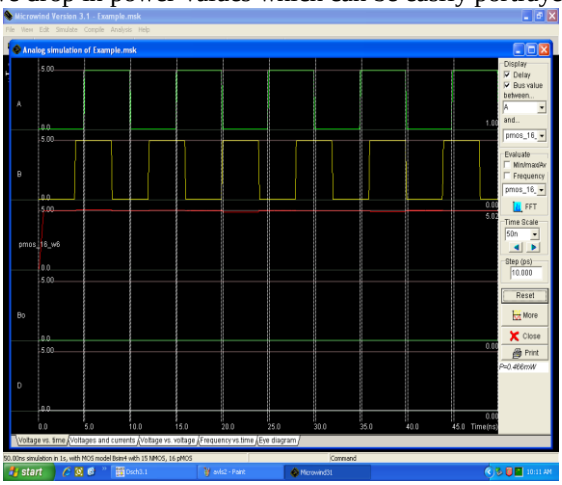

Figure 8 – Waveform of conventional Half-Subtractor

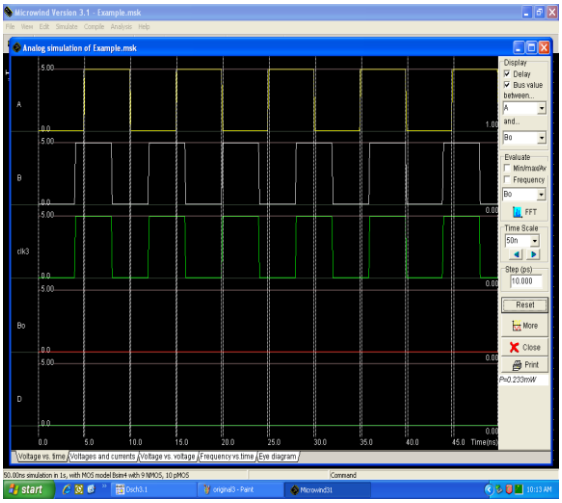

Figure 9 – Waveform of Half-Subtractor using AVLG Technique

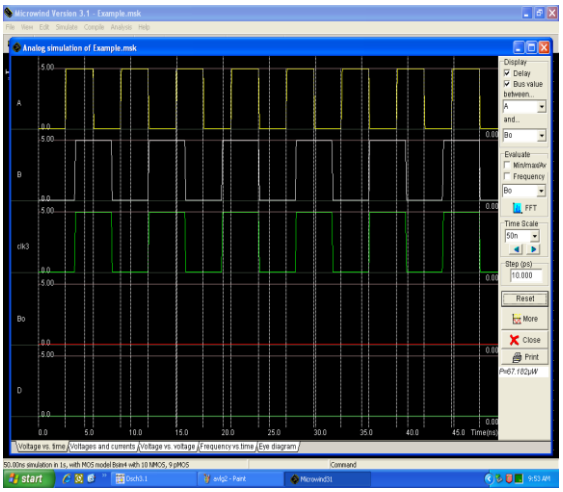

Figure 10 – Waveform of Half-Subtractor using AVLS Technique

VI. Conclusion

Simulation results clearly demonstrated the reduction in the power consumption by using AVL Technique which is either AVLG or AVLS Technique.

Comparison of the conventional Half-Subtractor with the Half-Subtractor incorporated with AVLG and AVLS techniques:

S. No.	***Parameters***	***Conventional***	***AVLG***	***AVLS***
1.	Power Consumption	0.466 mW	0.233 mW	67.182 µW
2.	Routed Wires	31	41	13
3.	Compiled Cells	16/16	19/19	19/19
4.	Layout Area	55,002 μm^2	84,357 μm^2	180,492 μm^2
5.	Propagation Delay	50 ps	35 ps	21 ps
6.	No. of p-mos and n-mos transistors	8 , 8	10 , 9	9 , 10

The comparison results clearly show us that the Half-Subtractor circuit implemented using AVLS technique gives us the appropriate dimensions of various parameters helping in obtaining a near optimum Half-Subtractor circuit. On designing AVLS technique based Half-Subtractor using 90 nanometre technology, we obtain a low power consumption circuit and also with lesser number of routed wires as compared to the conventional Half-Subtractor circuit.

SUMMARY

In this paper, we compare the simple CMOS technology and the AVL technology. The AVL technology has a reduced power consumption and shorter propagation delay in comparison with the simple CMOS technology.

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