Design and Analysis of Conventional and Ratioed Cmos Logic Circuit

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Abstract*: This paper compares the ratioed logic circuits and conventional CMOS design. This comparison performed on efficient CMOS circuit realizations and the ratioed logic circuits and it is resulted in to superiority of ratioed circuit over the conventional CMOS in some cases with respect to area, input capacitance. In this paper, 4-input NAND gate is designed using the conventional CMOS design and pseudo-NMOS logic design, which is the most common form of CMOS ratioed logic and the results are compared using Microwind and DSCH2 CMOS layout tools.*
Keywords *- CMOS, DSCH2 , PSEUDO-NMOS, NAND Gate , Microwind*

I. Introduction

Today's integrated circuits have a growing need for speed,area, and power. Despite many advantages, CMOS suffers from increased area, more power dissipation and correspondingly increased capacitance and delay, as the logic gates become more complex. Ratioed circuits use weak pull-up devices and stronger pull-down devices. They reduce the input capacitance and hence improve logical effort by eliminating large pMOS transistors loading the inputs, but depend on the correct ratio of pull-up to pull-down strength. Ratioed circuits also dissipate static power while the output is low, so they must be used in a limited fashion where they provide significant benefits[1,2].

In this paper, we have designed 4-input NAND gate using conventional CMOS and pseudo-NMOS logic gate, which is the most common form of CMOS ratioed logic on MICROWIND/DSCH2.Number of transistors is less in pseudo-NMOS than in CMOS and hardware requirement is also low, other parameters are delays, low input capacitance, area and various parameters are compared for corresponding circuit. Various parameters of 4-input NAND gate are studied on the basis of CMOS and pseudo-NMOS logic. We have studied the circuit on the basis of Microwind and DSCH2 tools .Section II give a brief description of conventional CMOS design,section III describes the pseudo-NMOS logic design. In section IV conventional CMOS is compared with pseudo-NMOS logic design by the help of Microwind DSCH2 tool. Section V concludes the paper.

II. Conventional Cmos Logic Design

The logic is used in the circuits basically effect the speed ,area, capacitance and delays and complexity of the circuit. Two important characteristics of CMOS are high noise immunity and static low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states.fig.1 shows the schematic circuit diagram of 4-input NAND gate using conventional CMOS logic design. This circuit uses the 8-MOS transistor to perform the operation of NAND gate. In this circuit there is 4-pull up pMOS transistor and 4-pull down NMOS transistor is used. In case of 4-input NAND gate, when all inputs are high, then all the NMOS transistors (bottom half of the diagram) will conduct, neither of the pMOS transistors (top half) will conduct, and a conductive path will be established between the output and V_{ss} (ground) , bringing the output low. If either of the input is low, one of the NMOS transistors will not conduct, one of the PMOS transistor will, and a conductive path will be established between the output and V_{dd} (voltage source),bringing the output high.
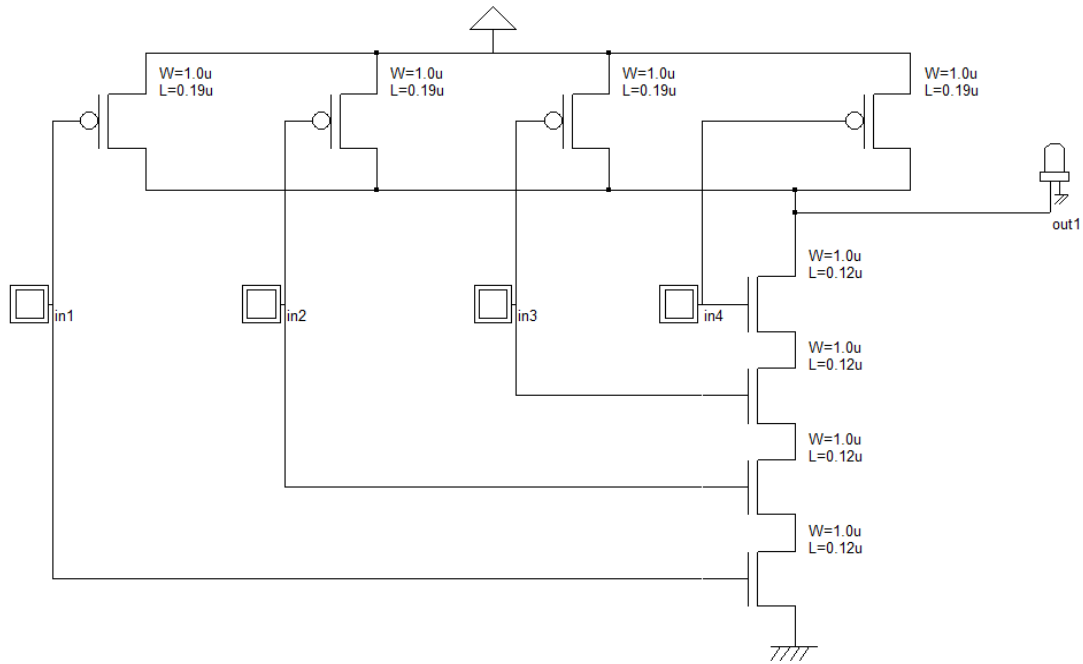
Fig. 1 Schematic of 4-input NAND gate

Fig. 2 shows the timing operation performed on 4-input NAND gate using conventional CMOS design,the rise delay and fall delay has calculated is 0.003ns and 0.002ns respectively.
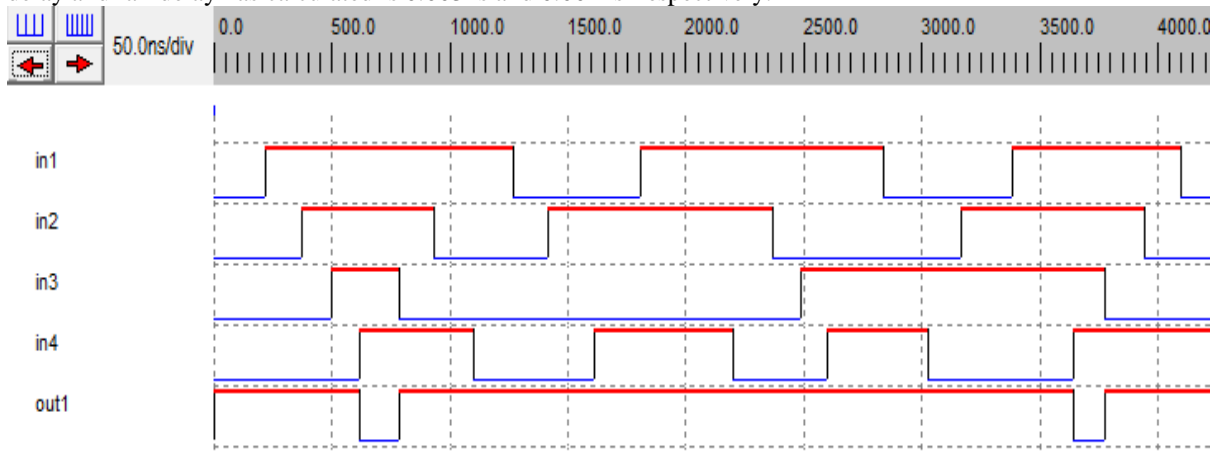

Fig. 2 Timing diagram of 4-input NAND gate

After simulation of the circuit, the above circuit is implemented using Microwind 2[4] CMOS layout tool. Microwind accelerate the design cycle and reduces the design complexities, and simulate the circuit then verify the logic of the circuit. The layout of the circuit is implemented in 0.12μm technology. Fig. 3 shows the layout of 4-input NAND gate using conventional CMOS logic design. The width of layout is 12.6μm(210 lambda),height is 7.9μm(132 lambda) and the surface area is 99.5μm^2 .
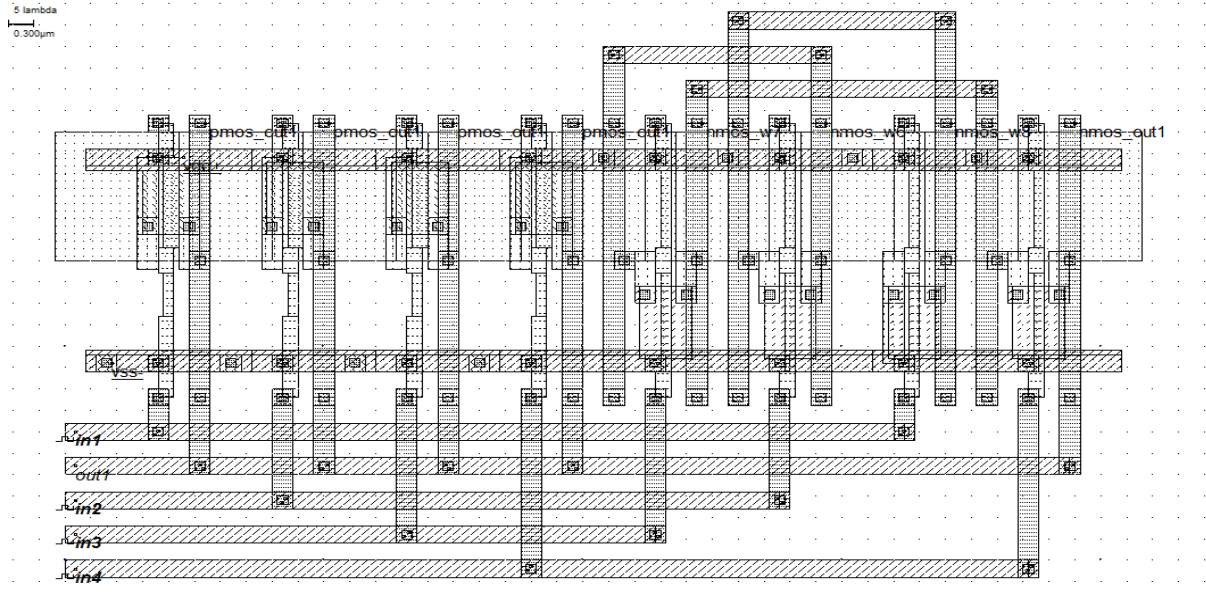
Fig. 3 Layout of 4-input NAND gate

III. Ratioed Logic Circuit

Ratioed MOS circuits have been known for many years, and were used widely in the past despite their high power dissipation because they are fast static circuits[3]. Ratioed circuits use weak pull-up devices and stronger pull-down devices. They reduce the input capacitance and hence improve logical effort by eliminating large PMOS transistors loading the inputs. Fig.4 shows the schematic circuit diagram of 4-input NAND gate using pseudo-NMOS logic gates, which are the most common form of CMOS ratioed logic. The pull-down network is like that of a static gate,but the pull-up network has been replaced with a single pMOS transistor that is grounded so it is always ON[1]. The main advantage of 4 -input pseudo NMOS logic gate is that there is 1-pMOS and 4-NMOS transistors is used, so the number of components has reduced and area also reduced. It also reduces the complexities of the circuit. Because of less hardware used so the capacitance become reduced.
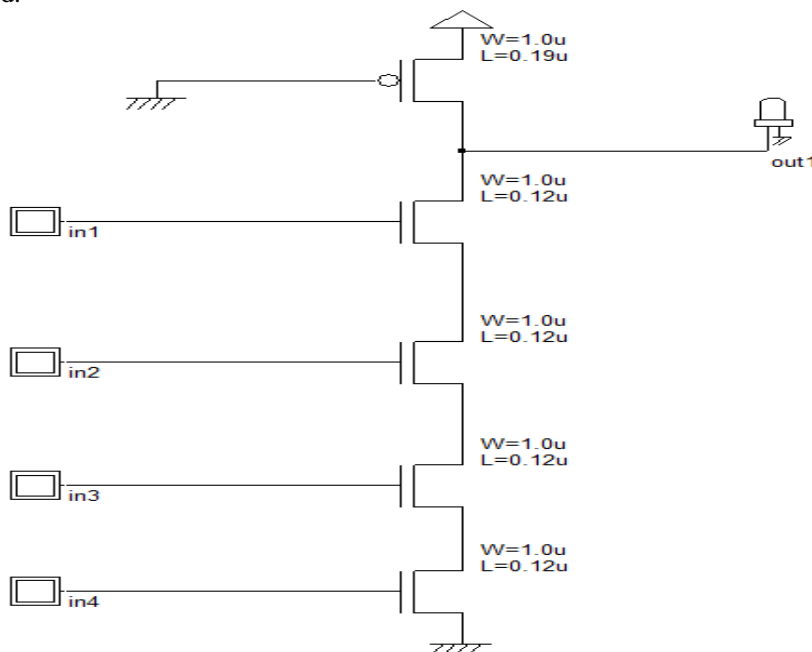

Fig. 4 Schematic of 4-input NAND gate using ratioed logic

In fig.5 shows the timing operation performed on 4-input NAND gate using ratioed logic design, the rise delay and fall delay calculated is 0.005 ns and 0.001ns respectively.
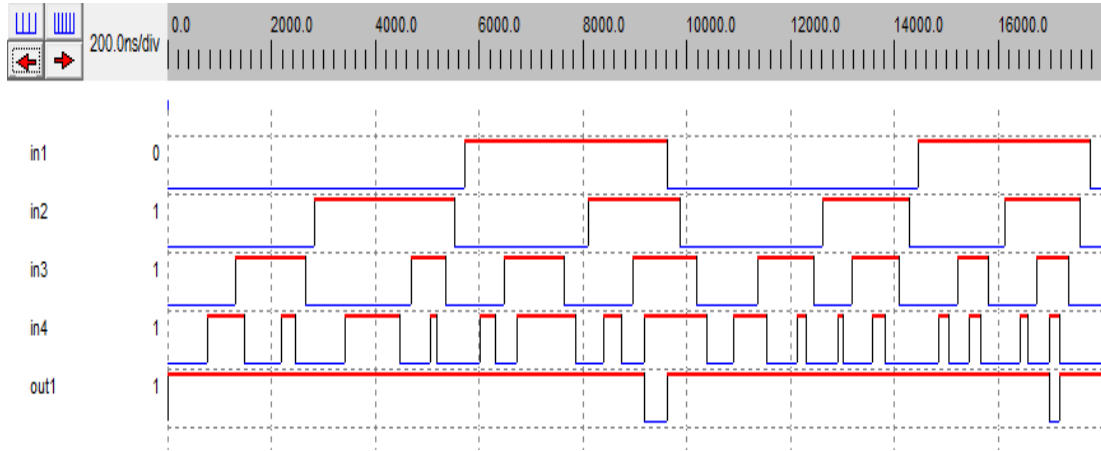

Fig. 5 Timing diagram of 4-input NAND gate using ratioed logic

Fig.6 shows the circuit layout of 4-input NAND gate using ratioed logic design. The width of layout is 8.3 μm(138 lambda) and height is 7.4 μm(124 lambda) and surface area is 61.4μm^2 (0.0mm^2).
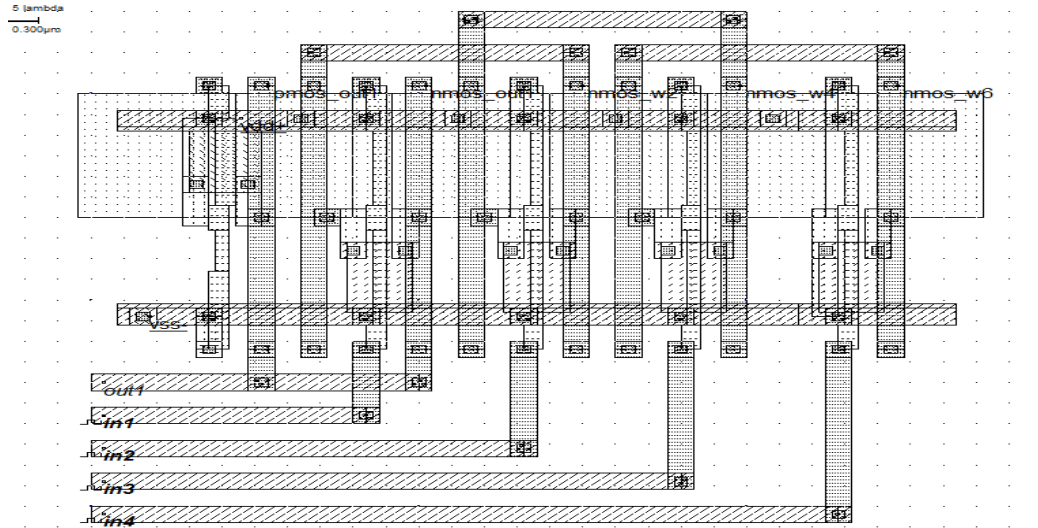

Fig.6 Layout of 4-input NAND gate using ratioed logic

IV. Result And Comparison

The comparison of 4-input NAND gate using CMOS and 4-input NAND gate using ratioed logic is shown in Table 1.

TABLE 1- PARAMETRIC ANALYSIS

S.NO	PARAMETERS	4-INPUT NAND GATE USING CMOS	4-INPUT NAND GATE USING RATIOED LOGIC
1	Width of layout	12.6μm(210 lambda)	8.3 μm(138 lambda)
2	Height of layout	7.9μm(132 lambda)	7.4 μm(124 lambda)
3	Surface area	99.5μm^2	61.4μm^2
4	Input Capacitance	At input1=4.26 fF	At input1=1.83 fF
		At input2=4.56 fF	At input2=1.90 fF
		At input3=4.56 fF	At input3=1.97 fF
		At input4=4.76 fF	At input4=2.05 fF
5	Output Capacitance	3.03 fF	1.12 fF
6	Number of transistor required	8	5
7	Rise delay	0.003 ns	0.002ns
8	Fall delay	0.005 ns	0.001 ns
9	Power dissipation	0.827μW	25.589 μW

V . Conclusion

In this paper, we represented 4-input NAND gate using pseudo -NMOS logic gates, which is the most common form of the ratioed logic circuit and shows that such type of designing can lead to decrease the area and input capacitance and number of components has also reduced, but its power dissipation is more and delays are also more as compared to conventional CMOS, so therefore ratioed circuit can be used in the areas where our requirement is of less area ,low input capacitance, because we cannot use this circuit anywhere as compared to conventional CMOS circuit, so therefore ratioed circuit can be use in the areas where our requirement is of less area ,low input capacitance.

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