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Design of High Gain CMOS Comparator with Slew Rate Of 10V/µS

D.Nageshwar Rao[1,] M.S.Sameera[2,] Fouzia Nasir[3,] M.A.Muqeet[4]
Assoc.Prof., Asst.Prof.,[1,2,3,4] (ECE DEPARTMMENT, Nizam Institute Of Engineering & Technology, JNTUH),India.

Abstract: *In present days mixed signal design is very important in many of system applications like Analog to digital convertors, switching circuits and communication blocks. In ADC architecture comparator is the main functional block. Main purpose of the comparator is to compare a signal with a reference signal and produce an output depending on whether the input is greater or smaller than applied references. Settling time is important in analog signal processing in order to avoid the errors in the accuracy of processing analog signal and to have fast settling time. To get the fast settling time the circuit must be with high slew rate. A longer settling time implies that the rate of processing analog signals must be reduced. In this paper presented design of CMOS comparator of high gain in order of 10^3 with slew rate of 10v/µs. This architecture is operates at 3V power supply and design is simulated using LT-SPICE tool. Transient response, ac analysis and slew rate results also shown and discussed in this paper.*

I. Introduction

Comparator is widely used in the process of converting analog signals to digital signals. Low power and high speed ADCs are the main building blocks in the front-end of a radio-frequency receiver in most of the modern telecommunication systems. As the comparator is one of the block which limits the speed of the converter. In the A/D conversion process, it is necessary to first sample the input and then comparator compares the voltages that appear at their inputs and outputs a voltage representing the sign of the net difference between them [1]. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +, VP, the input of the comparator is at a greater potential than the -, VN, input, the output of the comparator is a logic 1 and vice versa.

Basic comparator symbol along with conditions are shown in Fig 1.1.

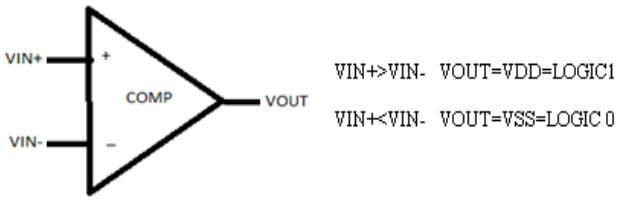

Fig 1.1: Comparator Symbol with conditions.

Input-output characteristic of an ideal and practical comparator is shown in Fig 1.2.

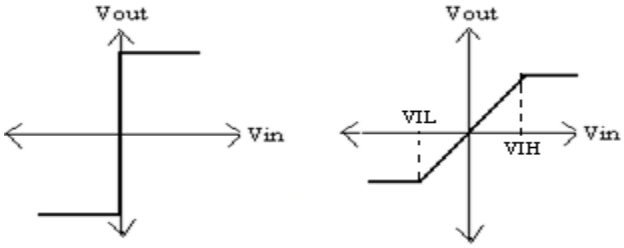

Fig 1.2: Ideal and Practical Comparator.

II. Characteristics Of Comparator

2.1 Minimum input slew rate: Slew rate is a large-signal behavior that sets the maxi-mum rate of output change. It is limited by the output driving capability of the comparator. It improves in sensitivity and speed performance of comparator.

2.2 Propagation delay: It gives the difference between input V+ crossing the reference voltages V- and output changes its logic states. Delay of the comparator can be reduced by cascading the gain stages i.e delay of single high gain stage is far greater than the delay of several low gain stages. The propagation delay is inversely proportional to the input voltage applied. This means that applying a larger input voltage will improve the propagation delay, up to the limits set by the slew rate [3].The most important dynamic parameters that determine the speed of a comparator are the propagation delay and the settling time. If the propagation delay time is determined by the slew rate of the comparator, then this time can be calculated as [4]:

$$\mathbf{T_P = \Delta T = \frac{\Delta V}{SR} = \frac{VOH - VOL}{2SR}}$$

where, T*p(*or)*ΔT* = propagation delay
ΔV = Change of the output voltage.
SR = Slew rate.
VOH = Upper limit of the comparator.
VOL = Lower limit of the comparator

2.3 Comparator offset: Due to the mismatch between input transistors, the circuit exhibits a DC offset of different values. This value of DC offset depends on the mismatch of input and output voltages. The Fig 1.2 shows a differential pair with perfect symmetry of input and output nodes, i.e. Vin =0 as well as Vout=0, Hence the circuit has no offset error. The input-referred offset voltage can be defined as the input level which forces the output voltage to go to zero [5]. The offset can limit the performance of comparator and it can make the system nonlinear.

III. Circuit Diagram And Its Design Steps

In this Section comparator architecture and its design steps are discussed.

3.1 Circuit Diagram: The following Fig3.1 shows the implementation of CMOS Comparator with NMOS input drivers.

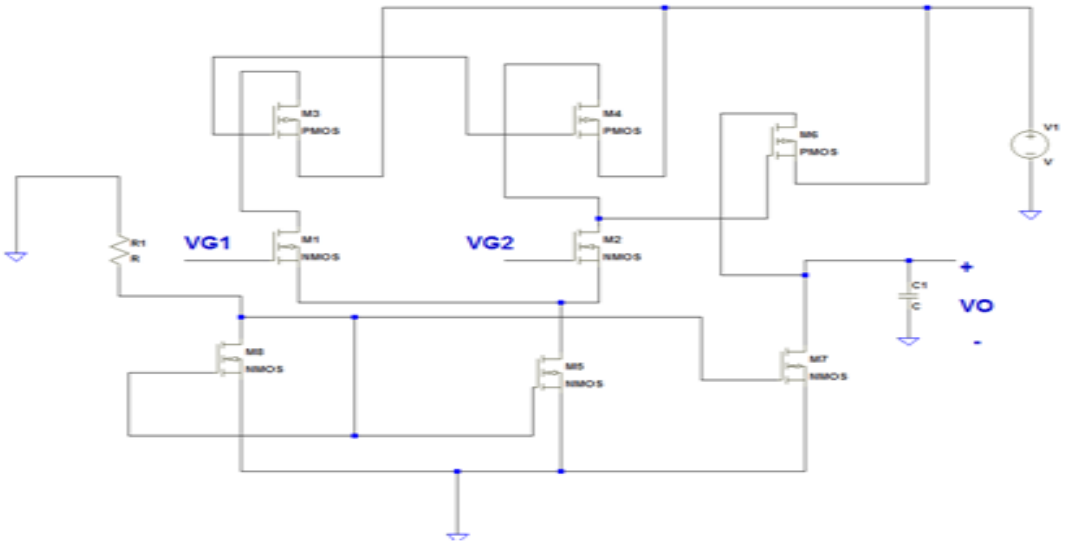

Fig 3.1: CMOS Comparator with NMOS input drivers.

3.2 Design Steps: The following specifications will be used in designing the comparator in NMOS processes are VDD=3V, VSS=-3V, AV>10000, -3<CMR<3, -3.5<Vo<3.5, SR=10V/us.

Step1: Determine the current drive requirement of M7 to satisfy the SR specification. $I_{D7} = C_L \left(\frac{dv}{dt}\right) = C_L$ (SR)….(1)

Step2: Determine the size of M6 and M7 to satisfy the output-voltage swing requirement.

$$V_{D7(SAT)} = V_{O(MIN)} - V_{SS} = \sqrt{\frac{2I_{DS7}}{\beta_7}} = \sqrt{\frac{2I_{DS7}}{K_N (W/L)_7}} \quad .....(2)$$

$$\left(\frac{W}{L}\right)_7 = \frac{2I_{DS7}}{K_N (V_{DS7(SAT)})^2}$$

Similarly**,**

$V_{SD\,6(SAT)} = V_{DD} - V_{O\,(MAX)}$ …..(3)

$$\left(\frac{W}{L}\right)_6 = \frac{2I_{SD6}}{K_P(V_{SD6(SAT)})^2} \text{.....(4)}$$

Step3: Calculate the gain of the second stage

$$A_{V2} = -\left(\frac{g_{m6}}{g_{ds6}+g_{ds7}}\right) = \frac{\sqrt{2K_P I_{SD6}\left(\frac{W}{L}\right)_6}}{I_{SD6}(\lambda_P + \lambda_N)} \text{.....(5)}$$

Step4: Calculate the gain of the first stage to satisfy the overall gain.

Step5: Determine the first stage biasing current using the minimum allowable size of (W/L)=1, and minimum output offset.

(a) Consider M4 and M6.

Using the minimum size for M4, determine the current I_{SD4} that mirror with M6. i.e, $I_{SD4}=$ $\left(\frac{(W/L)_4}{(W/L)_6}\right) I_{SD6}$

(b) Consider M5 and M7. Using the minimum size for M5, determine the current I_{DS5} that mirror with M7.

That is, $I_{DS5}=\left(\frac{(W/L)_5}{(W/L)_7}\right) I_{DS7}$ & $I_{SD4=}\, I_{DS5}/2=I_{SD3}$

$$I_{DS1}=I_{DS2}=I_{DS5}\left(\frac{W}{L}\right)_1 = \frac{(A_{V1})(I_{DS1})(\lambda_N+\lambda_P)^2}{2K_N I_{DS1}} \text{.....(6)}$$

(c) Select the larger of the two I_{SD4} and adjust the size of M4 such that $\left(\frac{W}{L}\right)_4 = \frac{I_{SD4}}{I_{SD6}}\left(\frac{W}{L}\right)_6$

Step6: Determine the size of M1 to satisfy the gain requirement.

$$A_{V1} = -\left(\frac{g_{m1}}{g_{ds2}+g_{ds4}}\right) = \frac{\sqrt{2K_N I_{DS1}\left(\frac{W}{L}\right)_1}}{I_{DS1}(\lambda_P+\lambda_N)} \text{.....(7)}$$

$$\left(\frac{W}{L}\right)_1 = \frac{(A_{V1})(I_{DS1})(\lambda_N+\lambda_P)^2}{2K_N I_{DS1}} \text{.....(8)}$$

Step7: The minimum size of M5 (=1) in step 5(b) can be adjusted to satisfy the negative input CMR of –3V.

$$V_{G1(MIN)} = V_{SS} + V_{DS5(SAT)} + \sqrt{\frac{2I_{DS1}}{K_N\left(\frac{W}{L}\right)_1}} + V_{T1} \text{.....(9)}$$

$$V_{DS5(SAT)} = \sqrt{\frac{2I_{DS5}}{K_N\left(\frac{W}{L}\right)_5}}$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{DS5}}{K_N(V_{DS(SAT)})^2} \text{.....(10)}$$

Select the larger of the two, $(W/L)_5$=1. No adjustment needed, since this is the value used earlier in the calculation.

Step8: The minimum size of M3(=1) in step 5(a) can be adjusted to meet the positive input CMR of 3V.

$$V_{G1(MAX)} = V_{DD} - \frac{\sqrt{2I_{DS3}}}{K_P\left(\frac{W}{L}\right)_3} - V_{T3} + V_{T1}$$

$$\left(\frac{W}{L}\right)_3 = \frac{2I_{SD3}}{K_P(V_{DD} - V_{G1(MAX)} - V_{T3} + V_{T1})^2} \text{.....(11)}$$

Select the larger of the two, $(W/L)_3$=1. No further adjustment needed.

Step9: Determine the size of M8 to provide as the main current mirror for the comparator.

For V_{DS5}=0.5V and V_{DS7}=0.5V, this voltage corresponds to the value of V_{G8}=-3.5V or V_{GS8}=1.5V.

Let I_{SD8}=20uA and $\left(\frac{W}{L}\right)_8 = \frac{2I_{DS8}}{K_N(V_{GS8} - V_{TN})^2}$ .....(12)

The external resistor R_B connected between V_{G8} and ground must be chosen to provide the required current for M8 of 20uA.

According to the above equations all transistors aspect ratio are calculated which are shown in Table1

Table1: Transistors aspect ratios

PARAMETERS	M1	M2	M3	M4	M5	M6	M7	M8
I(µA)	2.5	2.5	2.5	2.5	5	20	20	20
T	N	N	P	P	N	P	N	N
(W/L)	1	1	1.33	1.33	1	10.66	4	4
W(µ)	5.4	5.4	7.2	7.2	5.4	59.4	22.2	22.2
L(µ)	6.6	6.6	6.6	6.6	6.6	6.6	6.6	6.6

Step10: Select the width of each transistor.

IV. Simulation Results

Comparator designed and simulated using LT-Spice software. Output of the comparator is shown below. The designed circuit operates at 3V power supply. Simulated comparator output presented between -3V (low) and +3V (high) without offset voltage as shown in Figure4.1 as well as Comparator Transient response slew rate as shown in Figure 4.2 with pulse input.

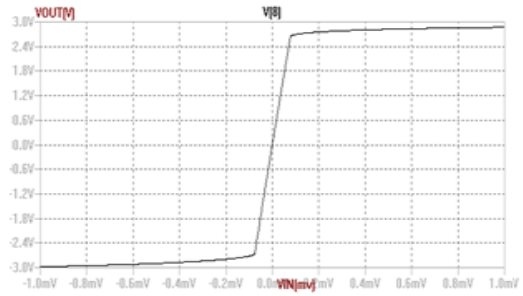

Fig 4.1: Comparator output without offset voltage.

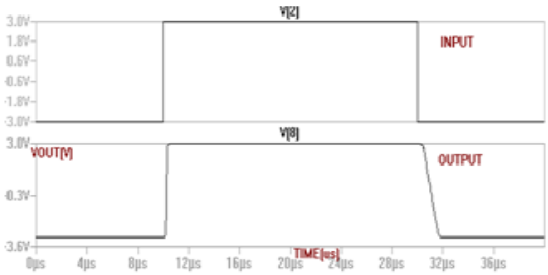

Fig4.2: Comparator Transient Response Slew Rate.

Comparator gain and phase margins also determined. This is the main characteristics in many applications. Approximately gain of the comparator is 90db and phase of 30 degree as shown in Figure4.3 and Comparator Transient Response Settling time as shown in Figure4.4 with pulse input.

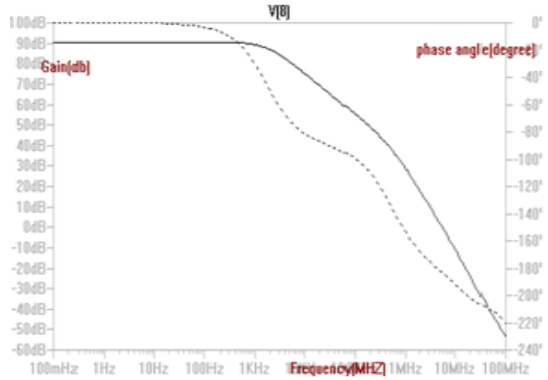

Fig4.3: Comparator gain and phase margin.

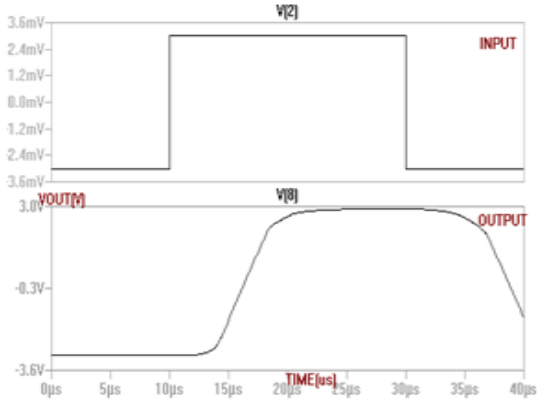

Fig 4.4: Comparator Transient Response Settling time

V. Conclusion

The CMOS Comparator with NMOS input designed and simulated in LT-Spice. The simulation results shows that delay is 0.09532ns and slew rate of 10v/us. Transient response, Comparator gain and phase response are discussed.

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