IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 2, Issue 1 (Mar. – Apr. 2013), PP 45-50
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design of Low Power and High Speed CMOS Buffer Amplifier with Enhanced Deriving Capability

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Abstract: *A high driving capability CMOS buffer amplifier with a novel concept of telescope-cascaded differential stages has been designed in present paper. The circuit describes here the capacitive load behaviour with reduced distortion at output node. A high slew rate of 36.54 v/µs is achieved with minimizing the quiescent current in the present circuit. A uniform voltage gain of 12.11 is obtained by varying the capacitive load [1nf to 5nf].The circuit has been fabricated using 180 nm technology. With 5nf load capacitor is efficiently used for charging capability in a ±1.8 v power supply. In a designed circuit, we attained overall power consumption 70.5 µW and improved tranconductance 3.561µs/µm.*

Keywords - *Buffer amplifier, slew rate, cascaded stages, source driver.*

I. Introduction

A buffer with complementary differential pair is capable to deliver stronger current and thus have better driving capability. As mentioned in [1], [2]. In order to achieve higher driving capability with low static power and low offset voltage, we design a newly developed telescope-cascade based buffer amplifier complementary differential input stages for low power and high resolution application in electronic display devices. As we know display resolution increases, load capacitance of buffer amplifier is increases, large number of buffer amplifier on a single chip creates power dissipation problem. Consequently, a high driving capability buffer amplifier with low static power consumption is requisite [1].

There are many works on LCD-TFT drivers [1-5], as mentioned in [1], [3-5]. In this paper a high performance, high speed CMOS buffer amplifier with low noise and rail to rail output swing is presented as mentioned in reference [6]. The power amplifier seems to be leading to configurations which take advantage of a common source type output stage in order to achieve higher load current capability along with a higher output swing as mentioned in reference [7], [8].The voltage buffer should improve while the buffer dissipates small quiescent current in the static state as mentioned in reference [9], [10]. In the designing of buffer amplifier circuit, large gate capacitance of power transistor degrades the loop gain bandwidth of transistor and the slew rate at the gate drive of low power condition [11], [12].In the recent developments amplifier compensation techniques are used to improve the amplifier's ability to reduce noise on the main power supply [13]. In order to achieve high performance, high speed buffer, important parameters such as slew rate, tranconductance, voltage gain, total power consumption, leakage current and static power should be based on the process technology used in the design [15], [16]. The experimental results are listed below along with comparison values formed in a table.

II. Proposed Circuit And Operation

1.1 BLOCK DIAGRAM

The designed buffer amplifier with two complementary differential input amplifiers is shown in Fig.1 below:

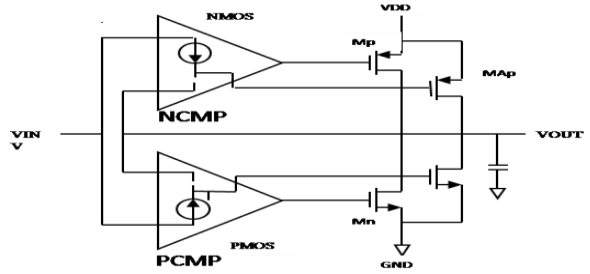

Figure1. Block diagram of CMOS buffer amplifier

The circuit was formed by a common source push-pull stages. Two auxiliary driving transistors are used for good swing characteristics. This technology is used to increase the driving capability of the whole circuit two transistors MAp and MAn are introduced in the given circuit. The two transistors MAp and MAn are used to control by two comparator NCMP and PCMP. NCMP are introduced as an N MOS transistor comparator circuit and PCMP are introduced as a P MOS transistor comparator circuit in the given circuit. The comparator circuit are mostly used to define how the circuit compares two voltages or current and switches it's output to indicate which is large they are commonly used in device such as analog to digital convertor(ADCs). The basic comparator will swing its output to $\pm V_{CC}$ at the lightest difference between its inputs but there are many variation where the output is designed to switch between two other voltage values also. The input may be tailored to make compares to an input voltage other than zero. The added comparators are used to reduce the power dissipation.

1.2 CIRCUIT DIAGRAM

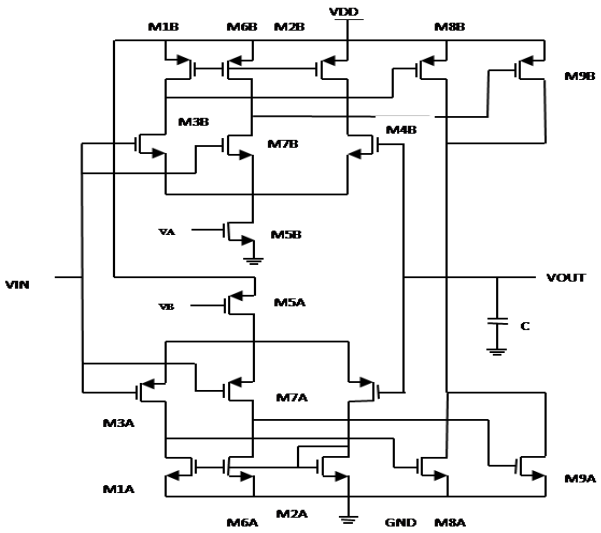

Figure2. Circuit diagram of CMOS buffer amplifier

Fig.2 Shown above shows the detailed circuits of the CMOS buffer amplifier in which two stage configuration are used in this design which consist of a high gain input stage and unity gain output stage. In the above designed circuit transistor M1A – M5A and transistor M1B – M5B form the complementary telescope – cascade differential stages. The two designed stages are connected parallel to make a common source push-pull stages. In the above shown fig. two transistors M5A and M5B forms the biasing current source. There are number of methods are used for biasing. There biasing currents are determined by VA and VB.The two stages are configured in parallel in the upper circuit transistor M6B – M7B and lower circuit the two transistor are used is M6A – M7A are connected to form two set of comparators. The two transistors M9A and M9B is the auxiliary driving amplifier without and with auxiliary power supply of 1.8 V is desired for proper working of the mentioned circuit diagram. Input voltage VIN is applied on two parallel transistors namely M3A and M3B.
The output response of the CMOS buffer amplifier can be expressed as

$$V_{out} = V_I + (V_F - V_I)[1 - \exp^{-t/\tau_p}) \quad (1)$$

Where VI and VF are the initial and final value of the output voltage respectively.
And

$$\tau_p = (R_{8B}||R_{9B}).C_L \quad (2)$$

Where C_L = Load capacitance
Defining R8A (B) and R9A (B) as the channel resistance of the output transistor M8A and M8B and the auxiliary driving transistor M9 (A) and M9 (B) respectively.
The positive slew rate of the CMOS buffer amplifier can be expressed by following equation:

$$dV_{out}/_{dt} = (V_F - V_I)/_{\tau_P} exp\frac{-t_1}{\tau_P} \quad (3)$$

Transistor M1A-M7A and M1B-M7B of the input differential pair are active when VIN reaches the centre of the supply voltage and biasing currents of the circuit are determined by VA and VB.
The current of M3A (B) and M7A (B) can be expressed as

$$I_{M7A(B)} = \tfrac{1}{2}\mu_{p(n)}C_{ox}\left(\frac{W}{L}\right)_7(V_{SG} - |V_T|)^2$$
$$1/2\mu_{p(n)}C_{ox}\left[\left(\frac{W}{L}\right)_3 - \Delta\frac{W}{L}\right](V_{SG} - |V_T|)^2$$
$$I_{M3A(B)}\left[1 - \Delta\frac{W}{L}\right] \quad (4)$$

The current through M7A and M7B is smaller than that through M3A and M3B that will derive M6A and M6B in the triode region and force VDS6A (B) close to 0 volt. The auxiliary driving transistor M9A and M9B will then stay off and consume no static power in that state. Hence, the aspect ratios of the auxiliary driving transistors can be designed with larger values to obtain higher driving capability without increasing power consumption.

For a given slew rate SR and load capacitor, we assume that

1. Transistor Mp and Mn both are in saturation region.
1. The channel length of transistor Mp and Mn is neglected. It can be demonstrated that the optimal size of the lower bound transistor Mp and Mn are given below

$$(W/L)_{L,M_p} = \frac{2.SR.C_L}{\mu_p C_{ox}(V_{DD} - V_{ov.Md5} - |V_{th,Mp}|)^2} \quad (5)$$

$$\left(W/L\right)_{L'M_P} = \frac{2.SR.C_l}{\mu_n C_{ox}\left(V_{DD} - |V_{ov.Md2}| - V_{th,M_n}\right)^2} \quad (6)$$

Equation (5) and equation (6) indicate to increase slew rate for a particular load capacitor of value 5nf.

We assume that ΔV=1.3v with V_{OL}=1.5v and V_{OH}=2.8v then $V_{OL} \leq V_o \leq V_{OH}$. Therefore, the upper bound transistor size is given below

$$(W/L)_{U,M_p} \leq \frac{0.1C_L b_{1.g_m}\delta V}{\mu_p C_{ox} V_1(|V_{th,M_p}| - |V_{ov,Md4}|)} \times \ln\left(\frac{V_{DD} - V_{OL}}{V_{DD} - V_{OL} - 0.9\Delta V}\left(1 + \frac{0.9\Delta V}{2V_1 + V_{OL} - V_{DD}}\right)\right) \quad (7)$$

The upper bound transistor size Mn is given below

$$\left(\frac{W}{L}\right)_{L,M_n} \leq \frac{0.2C_L b_{2g_m}\delta V}{\mu_n \% C_{ox} C_{p2} V_2 (V_{th,M_n} - V_{ov,Md6})} \times \left(\frac{V_{OH} - V_2}{V_2} + \frac{1}{2}\ln\left(\frac{2V_2}{V_{OL} + 0.1\Delta V} - 1\right)\right) \quad (8)$$

Then finally we arrange the transistors Mp and Mn within the range given below

$$(W/L)_{L,M_p} \leq (W/L)_{opt,M_p} \leq (W/L)_{U,M_p} \quad (9)$$

$$(W/L)_{L,M_n} \leq (W/L)_{opt,M_n} \leq (W/L)_{U,M_n} \quad (10)$$

We analyze the whole circuit through the pole and zero location of the input stage are given below

$$Z \approx \frac{-2g_{m6}g_{m8}g_{m11}}{C_{c1}g_{m6}g_{m11} + c_a g_{m8}g_{m12}} \quad (11)$$

$$P_1 \approx \frac{-1}{g_{m11}C_{c1}R_{o10}R_L} \quad (12)$$

$$P_2, P_3 = -\frac{g_{m8}(C_{c1} + C_L)}{2C_{c1}C_L} \pm j\left[\frac{g_{m8}g_{m11}}{C_L C_a} - \left(\frac{g_{m8}(C_{c1} + C_L)}{2C_{c1}C_L}\right)^2\right]^{1/2} \quad (13)$$

Where $C_a = C_{g8} + C_{ds8}$

The slewing period, $t_{slew,p}$ is determined by the time requirement to charge load capacitor is given below

$$t_{slew,p} = \int_{V_{OL}}^{0.9\Delta V + V_{OL}} \frac{2C_L dV_0}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{Mp}[2V_1(V_{DD} - V_0) - (V_{DD} - V_0)^2]} \quad (14)$$

$$\frac{C_L}{\mu_p C_{OX}\left(\frac{W}{L}\right)_{Mp} V_1} \times \ln\left(\frac{V_{DD} - V_{OL}}{V_{DD} - V_{OL} - 0.9\Delta V}\left(1 + \frac{0.9\Delta V}{2V_1 + V_{OL} - V_{DD}}\right)\right) \quad (15)$$

Where $V_1 = V_{DD} - V_{OV,Md5} - |V_{tp}|$

III. MODELLING AND SIMULATION RESULTS

Fig.3 show the output response curve of CMOS buffer amplifier simulated at 180 nm technology by virtuoso cadence tool

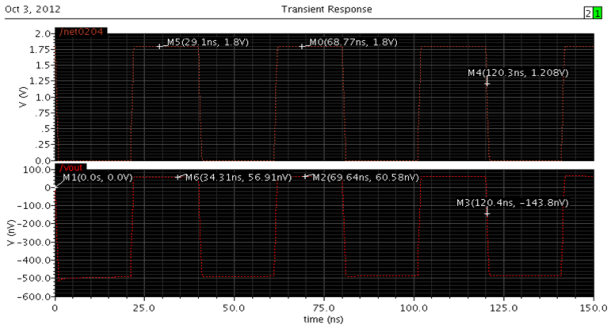

Figure3. Transient Response waveform

Fig.4 show the simulation result of overall power consumption has a threshold value is 844.1µw is marked below.

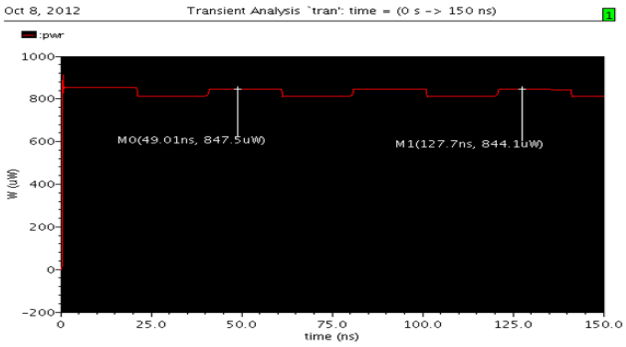

Figure4. Power Response Waveform

Fig.5 show the static power response curve of CMOS buffer amplifier has obtain value is 813µw.The curve is simulated at 180 nm technology by virtuoso cadence tool.

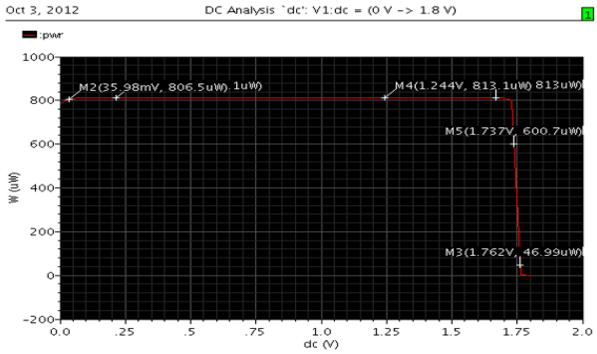

Figure5.Static Power response

Fig.6 shows leakage current waveform for which simulation result is -452.10µA is marked below. The waveform simulated at 180 nm technology by cadence virtuoso tool.

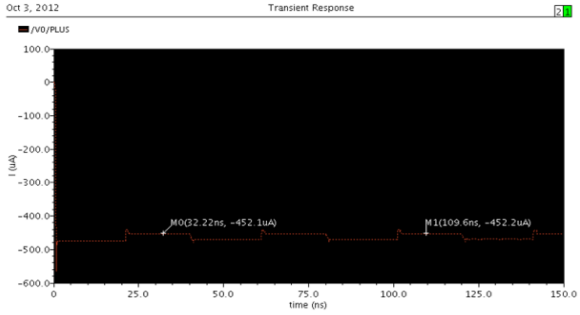

Figure6.Leakage Current waveform

Fig.7 shows the simulation result of slew rate whose threshold value is obtained 550.1v/µsec. A number of values are marked on the curve but we can observe peak threshold value

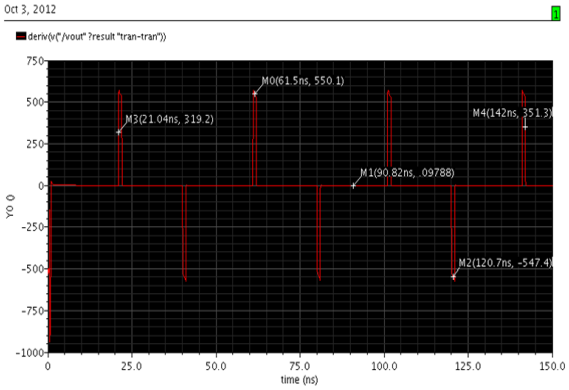

Figure7. Slew Rate waveform

Fig.8 show the simulation result of tranconductance at 180 nm technology obtained threshold value is 3.561 as marked belowby using cadence virtuoso tool.

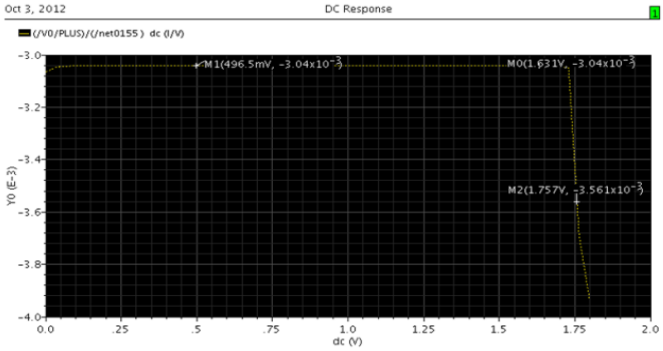

Figure8. Tranconductance waveform

Fig.9 show the simulation result of voltage gain value marked in curve below is 12.11. This value is simulated at 180 nm technology by cadence virtuoso tool.

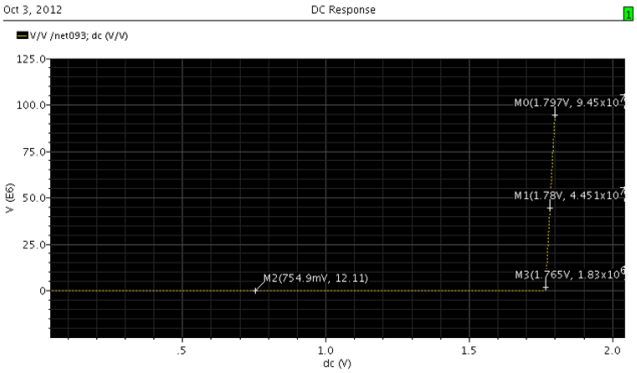

Figure9. Voltage Gain waveform

TABLE.1

Sr. No.	**Parameter**	**Technology Used**	**Power Supply**	**Output**
1.	Total power (µw)	180nm	1.8v	70.5...
2.	Average power (µw)	180nm	1.8v	470.0
3.	Leakage current (µA)	180nm	1.8v	452.16
4.	Slew rate (V/µ sec.)	180nm	1.8v	36.54

5.	Tranconductance (µs/µm)	180nm	1.8v	3.561
6.	Voltage gain(v/v)	180nm	1.8v	12.11

IV. CONCLUSION

This paper presents the design of a high speed and enhanced driving capability CMOS buffer amplifier with low static power which is suitable for the source driver of high resolution. As per the simulation result a high driving slew rate having value of 36.54 is achieved by keeping the voltage gain constant up to the value of 12.11. Its low power requirement 70.5µW, high slewing rate, high driving capability and accuracy makes the buffer amplifier more suitable for high resolution display viz. LCD and TFTs etc

ACKNOWLEDGEMENT

The authors would like to thank ITM Universe, Gwalior and Cadence Pvt. Ltd. Bangalore, India.

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