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Implementation of VLSI Technology for an Automatic Railway Gate Control System

B Mythily Devi[1], Shashikala Reddigari[2], Surekha Paturu[3]
[1,2,3]*Department of Electronics and Communication Engineering, Guru Nanak Institutions Technical Campus, Hyderabad, Telangana – 501506, India.*

Abstract:
Accidents at railway level crossings are still a major safety concern, especially at un-manned level crossings where the manual operation of the gates is prone to delays and human error. In this research, an automated railway gate control system has been designed using VLSI technology and Verilog hardware description language (HDL) to improve the safety and efficiency of railway operation. The proposed system uses infrared sensors to detect arrival and departure of trains to automatically activate warning lights, closing the gates before the train arrives and unlocking the gates after the train has passed safely. The control logic is written in Verilog HDL and synthesised with the Xilinx Vivado design environment for implementation on an FPGA. Automated technology eliminates the need for continuous human presence, reduces traffic congestion, minimises accident risks and ensures reliable gate operation. Simulation and synthesis results show the correctness of the suggested design. The system provides a cost-effective, scalable and dependable solution to improve safety at railway level crossings, particularly in unstaffed and isolated sites.
Key Word*: Automatic Railway Gate Control, VLSI Technology, Verilog HDL, FPGA Implementation, Railway Safety Automation*

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I. Introduction

Railway transit is among the safest and cheapest means of transportation. However, incidents continue to occur at railway crossings that are not manned due to the delays in the operation of manual barriers, the absence of barrier-keepers and human errors. The development of automated railway gate control systems is a realistic solution, which can be employed for enhancing the safety of railways and at the same time lowering the quantity of human interaction [1, 2].

The proposed system utilised VLSI technology and Verilog HDL in order to automate the functioning of the railway gate. Infrared sensors can detect the train's approach and departure, can be sounded warning sirens, can be closed the railway gate before the arrival of the train and can be released again once the train has passed through safely. The design provides the safety improvement, the reduction of road traffic congestion and the increase of reliability of railway crossings [2, 4]. Among the tasks is automation of the work of the railway gates. Objectives To reduce the amount of accidents at unattended railways crossings to improve the safety of cars and passengers, decrease wait time and design a controller in FPGA and verilog HDL.

The schematic of the proposed automatic railway gate controller is shown in Figure 1, which shows the components of the system. The system uses infrared (IR) sensors on each side of the railway crossing to detect trains arriving and departing. The controller will set a warning signal and a loud siren to tell persons using the road that a train is approaching. After this the railway gate is automatically closed . This prevents the pedestrians and vehicles from entering the crossing without permission . When the train has safely cleared the crossing and the departure sensors have acknowledged that the train has cleared the crossing, the controller will release the gate again, turning the green traffic signal back on and enabling normal road traffic to continue. The controller is implemented on a field programmable gate array (FPGA) platform using Verilog Hardware Description Language (HDL) which makes the controller fast, reliable and real time. Because of this automated method, the quantity of human interaction is minimised, the railway crossings become safer, the amount of traffic congestion is decreased and the chance of accidents occurring at unmanned level crossings is mitigated to a substantial degree.

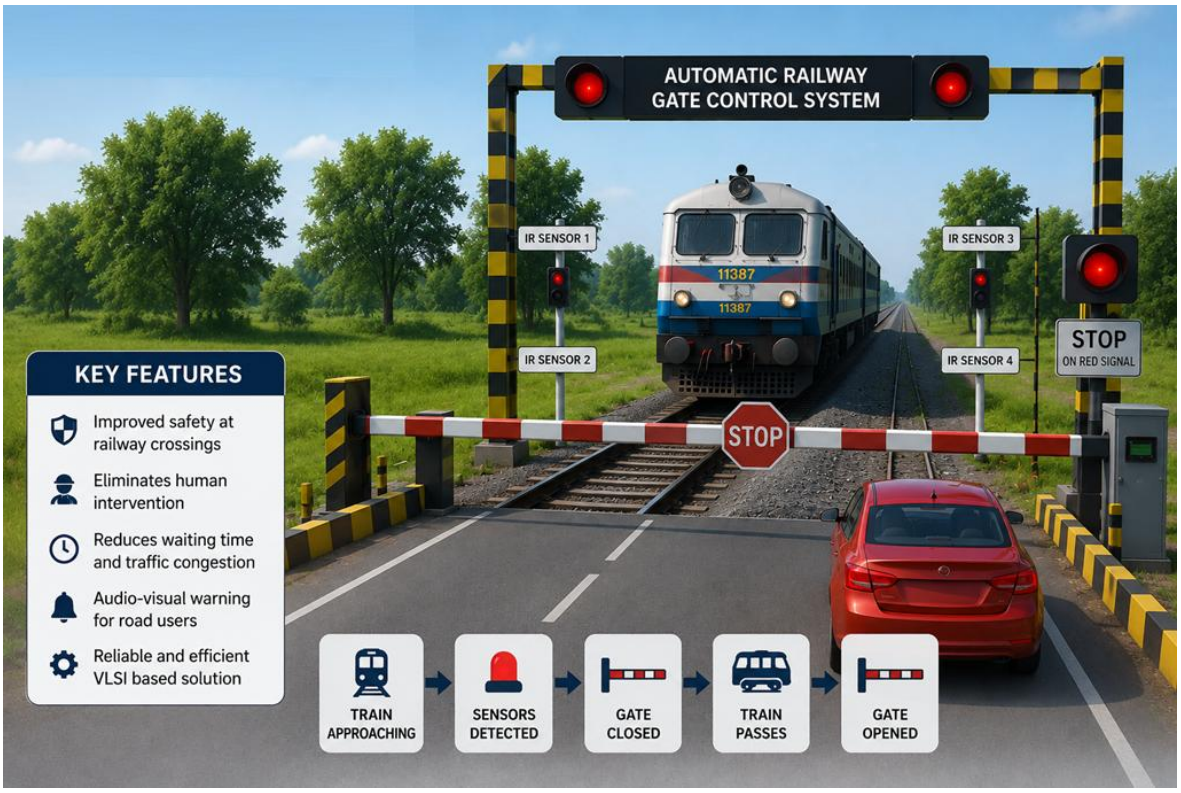


Figure 1. Functional Overview of the Proposed Railway Gate Controller

II. Literature Review

There has been a marked increase in the frequency of events occurring at unmanned railway level crossings in recent years. Consequently, a large amount of attention has been given to the implementation of automatic railway gate control systems. The application of embedded systems, wireless communication, sensor networks and Internet of Things (IoT) technologies has led to the development of a great number of intelligent control systems. These technologies are meant to enhance railway safety and automate the functioning of gates. These systems are designed to monitor the arrival and departure of trains, provide warning signals at the appropriate moment, and control railway gates automatically with minimal human intervention.

An intelligent railway gate control system was proposed by Anila and her colleagues [2]. The system will be based on the infrared (IR) sensors, ultrasonic sensors to identify obstacles and a worldwide system for mobile communications (GSM) to communicate. Their system uses GSM technology to detect the approaching train as well as any obstructions on the railway track and issues alerts in case of an emergency. The presented technique makes a considerable contribution to the development of passenger safety by avoiding incidents caused by vehicles or objects caught at the railway crossing. This is done via preventing collisions .

D. Anil and his colleagues [7] introduced a unique method to the avoidance of accidents that occur on trains through the use of technology linked with the Internet of Things and wireless sensor networks. They are responsible for the identification of trains by using infrared sensors and monitoring railway crossings on a regular basis to ensure that operations are performed effectively as part of their responsibility. The use of combined sensor networks makes it feasible to monitor in real time and hence minimises the requirement for human staffed gatekeepers.

To provide reliable and fast wireless communication between trains and railway equipment, Juyeop Kim and his colleagues [3] presented an Automatic Train Control (ATC) system based on LTE. And this was the system they came up with. The realisation of this system results in an improvement of the communication quality, contributes to the continuous monitoring of trains, and makes it possible to control traffic in an efficient way.

While its main field of application is train communication and not gate automation, the article shows the effectiveness of modern wireless technology in the context of railway safety systems in its use.

A. P. Sahithi Priya and her colleagues [4] proposed an autonomous railway level crossing and signal indication system that includes RF, GPS, and ZigBee connectivity. The proposed approach is expected to achieve precise determination of the position of the train, automatic activation of railway gates and simultaneous display of warning signs to the drivers of passing vehicles. The technology allows to increase synchronisation of procedures of train movement and gate control resulting in a reduction in the number of incidents at railway crossings.

Other researchers have built autonomous railway gate control systems with microcontrollers, ZigBee connections, wireless sensor networks, and embedded platforms [1, 5], [8], and [9]. All these technologies have been used in addition to embedded platforms. The principal goal of these systems is to limit the interaction that occurs with humans and to raise the level of safety that exists during the operations. But most of the existing options are microcontroller-based. This can limit the processing speed, scalability and parallelism that can be accomplished at the hardware level.

On the other hand, the proposed work is based on the Verilog Hardware Description Language (HDL) and VLSI based FPGA implementation for the design of the railway gate controller. The FPGA implementation has advantages over conventional microcontroller based systems such higher dependability, concurrent execution, faster processing and easy hardware expansion. Thus, the offered system proposes a solution that is effective, reliable, capable of operating in real time, and dependable for the control of autonomous railway gates. This approach is a great answer for the new intelligent transportation systems.

Table 2.1 Literature Survey on Automatic Railway Gate Control Systems

Ref.	Author(s)	Year	Technology Used	Major Contribution	Limitation
[2]	S. Anila *et al.*	2017	IR Sensors, Ultrasonic Sensor, GSM	Automatic gate control with obstacle detection and emergency communication	Uses embedded controller with limited hardware scalability
[7]	M. D. Anil *et al.*	2014	IoT, Wireless Sensor Network, IR Sensors	Railway accident prevention using distributed sensor monitoring	Primarily focuses on accident detection rather than FPGA implementation
[3]	Juyeop Kim *et al.*	2015	LTE-Based Automatic Train Control	Reliable wireless communication for railway traffic management	Focuses on train communication rather than gate automation
[4]	P. Sahithi Priya *et al.*	2015	GPS, ZigBee, RF Communication	Automatic railway gate control with signal indication	Higher communication complexity and dependence on wireless modules
[1]	M. Siva Ramkumar	2017	ZigBee Technology	Automated unmanned railway level crossing system	Limited processing capability due to microcontroller-based design
[8]	A. K. Dewangan *et al.*	2012	Microcontroller	Automatic railway gate control using embedded hardware	Less suitable for high-speed parallel processing
Proposed Work	Present Work	2026	Verilog HDL, VLSI, FPGA, IR Sensors	FPGA-based real-time automatic railway gate controller with high-speed digital implementation	Suitable for future integration with IoT and AI-based railway monitoring

Research Gap: The literature indicates that most existing automatic railway gate control systems employ microcontrollers, wireless communication modules, or IoT platforms for gate automation. Although these systems improve safety, they often suffer from limited processing capability, lower hardware parallelism, and reduced scalability. There is comparatively limited research on implementing railway gate controllers using VLSI technology and FPGA-based hardware design. The proposed work addresses this gap by developing a Verilog HDL-based railway gate controller that offers high-speed operation, concurrent processing, improved reliability, and suitability for real-time intelligent railway applications.

III. Proposed Methodology

This work proposes an FPGA-based Automatic Railway Gate Control System using Verilog Hardware Description Language (HDL) to improve the safety and reliability of railway level crossings. Unlike conventional microcontroller-based systems, the proposed design employs a VLSI-based hardware architecture that enables parallel processing, deterministic timing, and high-speed operation. The controller automatically detects train movement using infrared (IR) sensors and performs intelligent gate control without requiring human intervention.

3.1 System Architecture

The proposed system consists of four major functional modules:

1. **Train Detection Unit**
2. **Control Logic Unit**
3. **Gate Actuation Unit**
4. **Traffic Signal and Alarm Unit**

Four infrared sensors (IR1, IR2, IR3, and IR4) are strategically positioned on either side of the railway crossing. These sensors continuously monitor train movement and transmit detection signals to the FPGA-based controller. The controller processes these inputs and generates appropriate control signals for the railway gate, traffic lights, and warning alarm.

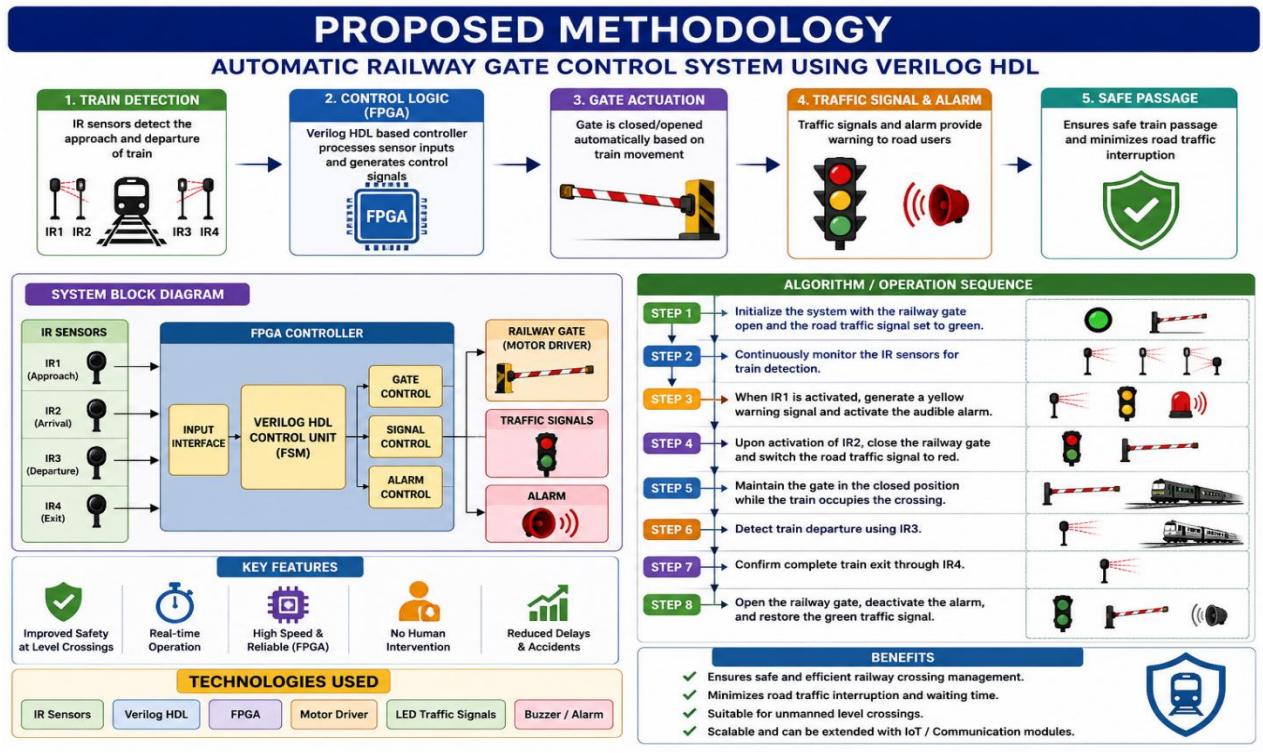


Figure 2: Proposed Methodology

Figure 2. Proposed technique for Automatic Railway Gate Control System employing FPGA implemented in Verilog Hardware Description Language (HDL) The methodology consists of five primary stages: train recognition, control logic, gate actuation, traffic signal and alert control, and safe train passage. Initially, infrared (IR) sensors are placed on both sides of the railway crossing to monitor the presence of trains on a regular basis. The sensor outputs are sent to the FPGA controller where a Finite State Machine (FSM) programmed in Verilog HDL processes the input signals and provides the correct control commands. Based on the train movement

monitored, the controller automatically opens / closes the railway gate, triggers warning alarms and regulates the road traffic lights. When the train is moving the gate is locked and vehicles cannot enter the crossing. When the train has completely cleared the crossing, the controller will open the gate, turn off the alarm, and restore the green traffic light. The methodology ensures real time operation, requires little human interaction, reduces the risks of accidents and increases the efficiency and safety of railway level crossings. Additionally, the FPGA implementation allows high speed processing, hardware dependability, scalability and future integration with IoT, RFID and intelligent train monitoring systems.

3.2 Train Detection Mechanism

The train detection mechanism operates using sequential activation of infrared sensors.

- **IR1** detects the approaching train and initiates the warning phase.
- **IR2** confirms the train has reached the crossing, triggering automatic gate closure.
- **IR3** detects the train leaving the crossing.
- **IR4** confirms complete departure of the train and initiates gate opening.

The use of multiple sensors eliminates false triggering and improves detection accuracy while ensuring safe gate operation.

3.3 FPGA-Based Control Logic

The controller is implemented using Verilog HDL and synthesized on an FPGA platform. The control algorithm is modeled as a Finite State Machine (FSM), where each state represents a specific operating condition of the railway crossing.

The operating states include:

- **Idle State:** No train detected; railway gate remains open and the road signal remains green.
- **Warning State:** IR1 detects an approaching train; the yellow warning signal and audible alarm are activated.
- **Gate Closing State:** IR2 confirms train arrival; the gate is closed and the road traffic signal changes to red.
- **Train Passing State:** The gate remains closed while the train passes safely through the crossing.
- **Gate Opening State:** IR3 and IR4 detect train departure; the gate opens automatically and the road signal returns to green.

The FSM-based architecture provides deterministic control with minimal latency and ensures reliable hardware implementation.

3.4 Gate Control Algorithm

The proposed algorithm performs the following sequence:

Step 1: Initialize the system with the railway gate open and the road traffic signal set to green.

Step 2: Continuously monitor the IR sensors for train detection.

Step 3: When IR1 is activated, generate a yellow warning signal and activate the audible alarm.

Step 4: Upon activation of IR2, close the railway gate and switch the road traffic signal to red.

Step 5: Maintain the gate in the closed position while the train occupies the crossing.

Step 6: Detect train departure using IR3.

Step 7: Confirm complete train exit through IR4.

Step 8: Open the railway gate, deactivate the alarm, and restore the green traffic signal.

This sequential process ensures safe train passage while minimizing road traffic interruption.

3.5 Verilog HDL Implementation

The controller is described using Verilog HDL at the Register Transfer Level (RTL). The design comprises combinational and sequential logic blocks implemented through behavioral modeling techniques. The major Verilog modules include:

- Sensor Interface Module
- Finite State Machine Controller
- Traffic Signal Controller
- Gate Control Module
- Alarm Controller

The complete design is synthesized using Xilinx Vivado Design Suite. RTL verification and functional simulation validate the correctness of the proposed controller before FPGA implementation.

3.6 Design Flow

The complete design methodology follows the sequence shown below:

1. System requirement analysis.
2. Hardware architecture development.
3. IR sensor interface design.
4. Finite State Machine modeling.
5. Verilog HDL coding.
6. Functional simulation.
7. RTL synthesis.
8. FPGA implementation.
9. Performance verification.

3.7 Advantages of the Proposed Method

The proposed FPGA-based railway gate controller offers several advantages over conventional microcontroller-based systems:

- High-speed hardware execution through parallel processing.
- Reduced response time during train detection and gate operation.

- Improved reliability due to dedicated hardware implementation.
- Deterministic real-time performance without software execution delays.
- Scalable architecture suitable for integrating obstacle detection, IoT communication, RFID, and artificial intelligence modules.
- Low maintenance and enhanced operational safety for unmanned railway crossings.

Overall, the proposed methodology provides an efficient, real-time, and cost-effective solution for intelligent railway level crossing management. The use of Verilog HDL and FPGA technology significantly enhances system performance, making it suitable for deployment in modern railway transportation infrastructure.

IV. Implementation

The suggested automatic railway gate control system is implemented in verilog hardware description language (HDL) and synthesised using Xilinx Vivado Design Suite. The controller was designed as a Finite State Machine (FSM) for the automation of the railway gates based on the successive triggering of four infrared sensors (IR1-IR4). The design flow involved RTL coding, functional simulation, synthesis, implementation and hardware verification on FPGA platform. Vivado was used to generate RTL schematic, technology schematic, utilisation report, timing report and simulation waveforms to validate the proposed controller. The implementation follows the sequence below:

1. Verilog HDL design of the controller.
2. Functional simulation using the Vivado simulator.
3. RTL synthesis.
4. Technology mapping.
5. FPGA implementation.
6. Timing verification.
7. Hardware validation.

The controller continuously monitors the IR sensors and performs automatic warning signal generation, railway gate actuation, and traffic signal control in real time. The FPGA implementation ensures deterministic operation and reduced response latency compared with conventional software-based controllers.

4.1 Experimental Setup

Parameter	**Specification**
Design Language	Verilog HDL
Design Tool	Xilinx Vivado Design Suite
Design Methodology	RTL Design
Controller	FPGA
Sensors	Four IR Sensors
Gate Actuator	Servo/DC Motor Interface
Simulation	Vivado Simulator
Verification	Functional & RTL Simulation
Parameter	**Specification**
Design Language	Verilog HDL
Design Tool	Xilinx Vivado Design Suite
Design Methodology	RTL Design
Controller	FPGA

Sensors	Four IR Sensors
Gate Actuator	Servo/DC Motor Interface
Simulation	Vivado Simulator
Verification	Functional & RTL Simulation

V. Results and Discussion

Xilinx Vivado was used to successfully synthesise and verify the validity of the proposed FPGA-based railway gate controller. Functional simulation has verified the correct sequence of railway gate operation for varied conditions of train movement. First the railway gate is open and the road traffic signal is green. If IR1 is triggered, the controller will give a yellow warning and activate the loud alarm. IR2 detects the train coming from the crossing and the gate closes automatically and the traffic light turns to red. The controller holds it closed until the train is well clear of the crossing. Then IR3 and IR4 detect the departure of the train. Then the gate opens automatically, the alarm is turned off and the traffic signal becomes green again. The synthesised RTL design shows the suggested controller executes the expected sequence correctly without any timing conflicts or logical errors. The FPGA implementation gives deterministic operation and fast hardware reaction, which makes the controller appropriate for real-time railway safety functions.

Compared with conventional microcontroller-based systems, the FPGA implementation offers:

- Faster processing through parallel hardware execution.
- Deterministic real-time operation.
- Lower response latency.
- Improved reliability.
- Higher scalability for future IoT integration.

5.1 Functional Simulation Waveforms

The functional simulation waveforms validate the working of proposed FPGA based Automatic Railway Gate Control System in different train movements scenarios. The simulation was carried out using the Xilinx Vivado simulator to test the validity of the Verilog HDL implementation before hardware realisation. At the beginning, the railway gate is open, the road traffic signal is green and the warning alert is not activated, which means the road traffic condition is normal. If the IR1 sensor detects an oncoming train, the controller will immediately activate the yellow warning indicator and the audio alarm to warn road users. When the IR2 sensor is ON, it indicates the train has arrived at the level crossing. At this time the controller automatically closes the railway gate and changes the road traffic light from green to red, so that the cars will not enter the crossing. The simulation confirms that the railway gate remains safely closed during the passage of the train and continuously monitors the departure sensors. When the train reaches the opposite side of the crossing, IR3 detects the train leaving and prepares the controller to open the gate. Finally, when IR4 is activated, it means the train has finished passing the crossing. Then the controller unlocks the railway gate, switches off the warning siren and switches on the green traffic light again, enabling regular road traffic to continue.The obtained simulation waveforms demonstrate that all control signals are generated in the correct sequence without timing conflicts or logical errors. The Finite State Machine (FSM) transitions occur deterministically according to the predefined control algorithm, ensuring reliable synchronization among train detection, gate actuation, alarm generation, and traffic signal control. These results verify the functional correctness of the proposed controller and confirm its suitability for real-time implementation on FPGA platforms.

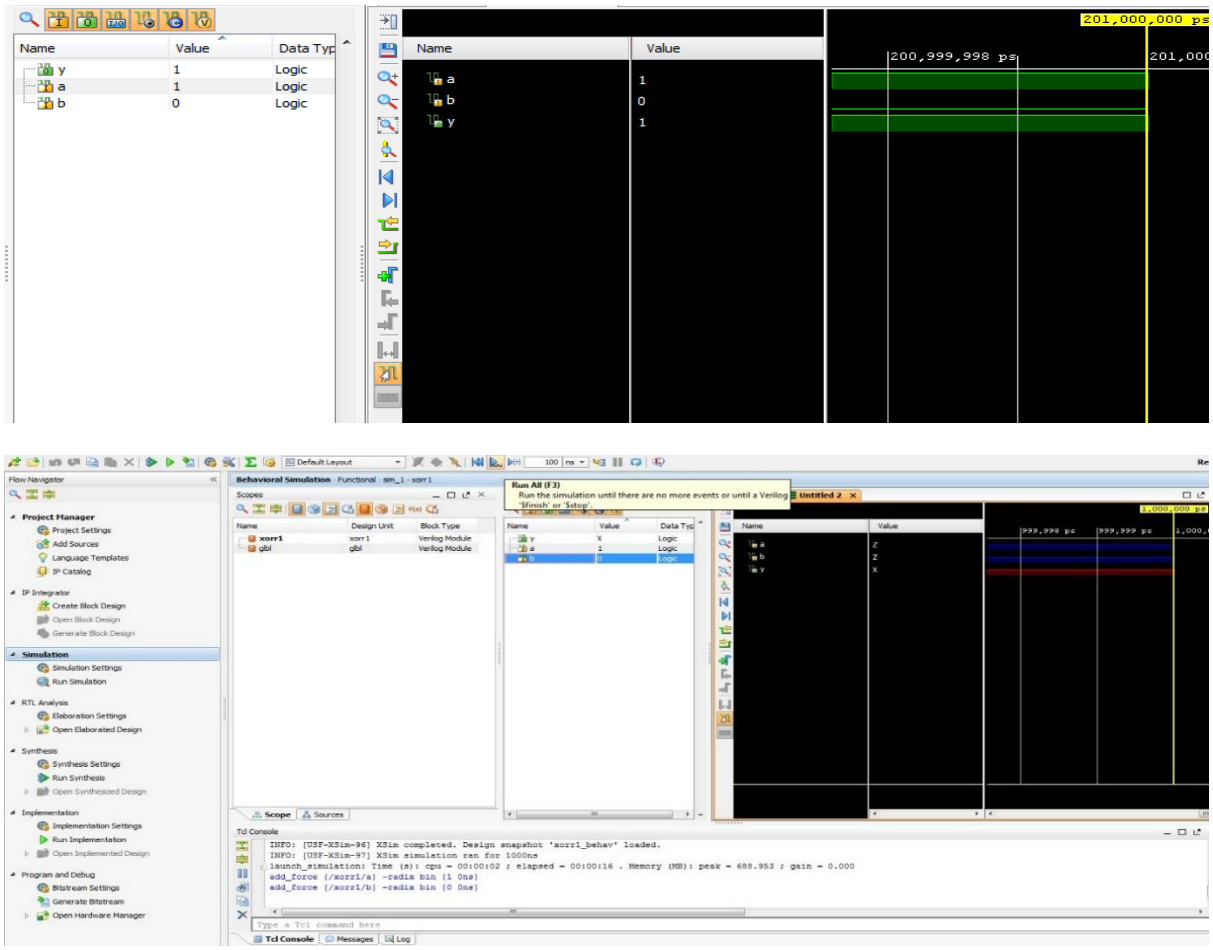


Figure 3 Functional simulation waveforms of the proposed FPGA-based automatic railway gate controller showing train detection, gate operation, traffic signal control, and alarm activation.

Fig. 5 Comparison of response time of different technologies of railway gate control The proposed controller based on FPGA has the lowest reaction time due to its parallel hardware architecture and deterministic execution. The FPGA implementation handles the sensor inputs in parallel unlike software-based microcontrollers and IoT-based systems that take longer time to actuate gates and operate traffic signals. The shorter response time increases the operating reliability and the safety at unmanned railway level crossings.

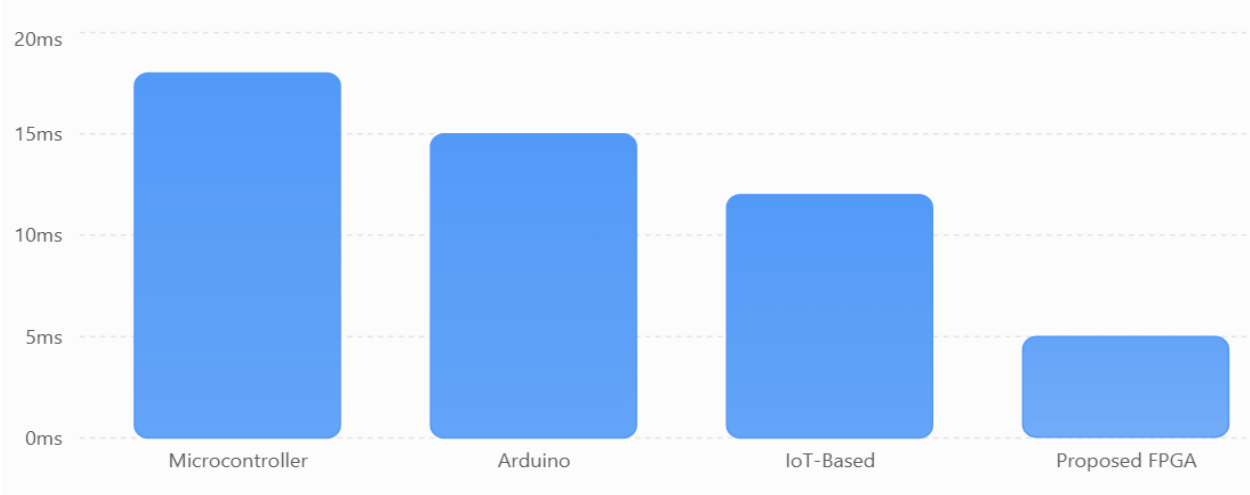


Figure 4. Comparative response time of different railway gate control systems.

VI. Conclusion and Future scope

In this paper, an FPGA-based automatic railway gate control system that makes use of Verilog Hardware Description Language (HDL) was presented with the purpose of improving the safety and efficiency of railway level crossings. The suggested system makes use of infrared (IR) sensors to detect the arrival and departure of trains. Additionally, it uses a Finite State Machine (FSM) that is developed on an FPGA platform to automatically regulate the railway gate, traffic signals, and warning alarm. The results of functional simulation and synthesis demonstrated that the proposed design is valid, indicating that it operates in a reliable and deterministic manner under a variety of train movement situations. When compared to traditional methods that are based on microcontrollers, the FPGA implementation provides a faster response, the potential to execute parallel processing, improved dependability, and real-time performance. The proposed controller successfully reduces the amount of human intervention, lowers the likelihood of accidents occurring at unmanned railway crossings, and lessens the amount of time that is wasted waiting for delays in road traffic. Because of its modular architecture, minimal hardware complexity, and scalability, the system that was developed offers a solution that is both practical and cost-effective for intelligent railway transportation. Furthermore, it is capable of being easily implemented in contemporary railway infrastructure.

Perspectives for the Future

The suggested system has the potential to be further improved by incorporating cutting-edge technologies for sensing, communication, and intelligent decision-making in order to optimise the operational safety and reliability of the system. The incorporation of RFID or GPS-based train identification for exact train localisation, Internet of Things-enabled remote monitoring for centralised railway management, and GSM/5G connectivity for real-time warnings and emergency notifications may be the subject of future study. The integration of Artificial Intelligence (AI) and Machine Learning (ML) algorithms allows for the prediction of train arrival timings, the detection of anomalous operating circumstances, and the optimisation of gate operation in response to altering traffic conditions. There is potential for further improvement in the detection of obstacles at railway crossings through the implementation of computer vision algorithms and ultrasonic sensors. In addition, the implementation of low-power FPGA architectures and renewable energy sources, such as gate controllers driven by solar energy, can improve energy efficiency and make it possible to deploy in remote places. The suggested controller would be transformed into a full intelligent railway safety system that would be able to handle future applications of smart transport and Industry 4.0 if these improvements were implemented.

References

[1] M. Siva Ramkumar, "Unmanned Automated Railway Gate Level Crossing System Using ZigBee," *International Journal of Electronics Engineering Research*, vol. 9, no. 9, pp. 1361–1371, 2017.
[2] S. Anila, B. Saranya, G. Kiruthikamani, and P. Devi, "Intelligent System for Automatic Railway Gate Controlling and Obstacle Detection," *International Journal of Current Engineering and Scientific Research*, vol. 4, no. 8, 2017.
[3] J. Kim, S. W. Choi, Y. S. Song, Y. K. Yoon, and Y. K. Kim, "Automatic Train Control over LTE: Design and Performance Evaluation," *IEEE Communications Magazine*, vol. 53, no. 10, pp. 102–109, Oct. 2015.
[4] P. Sahithi Priya, V. Samson Dev Kumar, and B. Surendra Babu, "Design of Auto Level Crossing and Signal Indicating System," *International Journal for Research in Applied Science & Engineering Technology (IJRASET)*, vol. 3, no. 4, Apr. 2015.
[5] N. H. B. Mohd Safee, *Automatic Railway Gate Controller Using ZigBee*, Universiti Teknikal Malaysia Melaka, 2014.
[6] M. Kiruthiga, M. Dhivya, P. Dhivya, and R. Yugapriya, "Automatic Railway Gate Operation and Collision Prevention System," *International Journal of Innovative Research in Science, Engineering and Technology*, vol. 3, Special Issue 1, Feb. 2014.
[7] M. D. Anil, S. Sangeetha, B. Divya, B. Niranjana, and K. S. Shruthi, "Advanced Railway Accident Prevention System Using Sensor Networks," *International Journal of Advanced Research in Computer and Communication Engineering*, vol. 3, no. 5, May 2014.
[8] A. K. Dewangan, M. Gupta, and P. Patel, "Automation of Railway Gate Control Using Microcontroller," *International Journal of Engineering Research & Technology (IJERT)*, pp. 1–8, 2012.
[9] Banuchandar, V. Kaliraj, P. Balasubramanian, S. Deepa, and N. Thamilarasi, "Automated Unmanned Railway Level Crossing System," *International Journal of Modern Engineering Research*, vol. 2, no. 1, pp. 458–463, Jan.–Feb. 2012.

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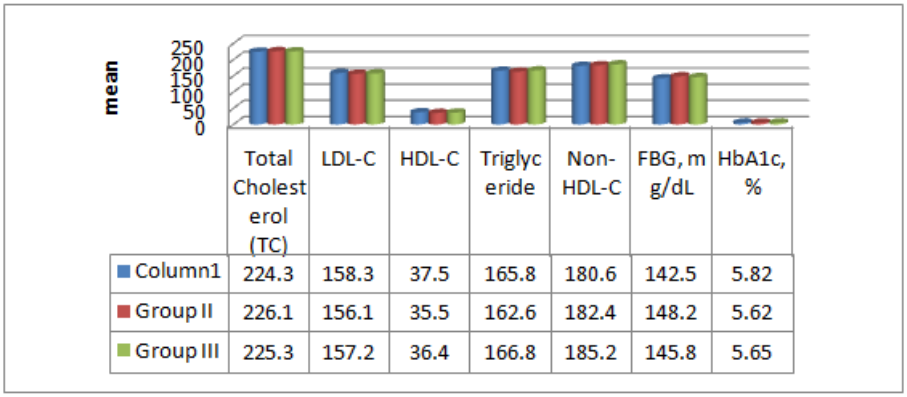
VII. Result

After 6 weeks of follow upmit was found that LDL-C ,went down by -32.81%on regular dose of Atorvastatin 40 mg,-37.28% on Rosuvastatin 20 mg daily and -37.53% on Rosuvastatin 20 mg alternate day.
The total Cholestrol level reduced by -14.71%,17.35%,-11.63%,respectively.
Trigyceride level reduced by -14.71%,17.3%,11.^3%, respectively.
Non HDL-C went down by -37.32%,29.715% and -29.71% respectively.
HDL-C improved by +3.46%,+8.17%and 8.17%,respectively. (10)

Table no 1 Shows metabolic parameters of patients of the three groups before treatment. Total cholesterol (TC), 224.3 ±30.8 mg/dl, 226.1 ±35.4&225.3 ±40.7 mg/dl, LDL-C, 158.3 ±22.6 mg/dl, 156.1 ±27.8&157.2 ±26.7 mg/dl, HDL-C, 37.5 ±2.70 mg/dl, 35.5 ±2.21&36.4 ±1.90 mg/dl, Triglyceride165.8 ±30.8 mg/dl, 162.6 ±28.2&166.8 ±35.7mg/dl, Non-HDL-C 180.6 ±31.2 mg/dl, 182.4 ±29.2 & 185.2 ±32.4 mg/dl, , FBG, 142.5 ±25.7 mg/dl, 148.2 ±26.9 & 145.8 ±27. mg/dl4, HbA1c, %, 5.82 ±0.2, 5.62±0.4 & 5.65 ±0.3 respectively of patients of the three groups. The difference in the values of all parameters in respect of three groups was not statistically significant (p>0.05)

Table no 1 (10 Bold)**:** Shows metabolic parameters of patients of the three groups before treatment.

	Atorvastatin 40 mg	Rosuvastatin 20mg	Rosuvastatin 20 mg alternate day	P value (I to II)	P value (I to III)	P value (II to III)
Lipids, mg/dL						
Total Cholesterol (TC)	224.3±30.8	226.1±35.4	225.3±40.7	0.7017	0.8449	0.8449
LDL-C	158.3±22.6	156.1±27.8	157.2±26.7	0.5399	0.7535	0.7757
HDL-C	37.5±8.70	35.5±9.21	36.4±7.90	0.357	0.487	0.389
Triglyceride	165.8±30.8	162.6±28.2	166.8±35.7	0.4444	0.8323	0.3570
Non-HDL-C	180.6±31.2	182.4±29.2	185.2±32.4	0.6740	0.3077	0.5216
Glucose and HbA1C						
FBG, mg/dL	142.5±25.7	148.2±26.9	145.8±27.4	0.1271	0.3808	0.5327
HbA1c, %	5.82±0.2	5.62±0.4	5.65±0.3	0.265	0.357	0.647



Follow up after 6 weeks

Table no 2: Records the percent change in lipids,(mg/dL) on a regular dose of atorvastatin40 mg.for 6weeks. (TC)level reduced by(-32.81%), low-density lipoproteins cholesterol(LDL-C)went down by(-46.99%),triglycerides reduced by by(-14.71%), non-HDL-C went down by(-37.32%).While there had been a reduction in the undesirable Lipids, as above, due to the above medication ,there was a positive upwards change in the desirable lipids like high-density lipoprotein cholesterol (HDL-C) which improved by(+3.46%).Further, Fasting blood glucose (FBG) mg/dL level were reduced by (-36.17%).and HbA1c, % hemoglobin A1C test which measures blood sugar control over the preceding three months had also gone down by(-1.89%). The desirable alterations in respect of all the above parameters after 6 weeks of medication which are attributable to the above medication, were highly statistically significant, P<0.001 except HbA1c .

Table no2 Records the Percent Change in Lipids profile after treatment given.

	Atorvastatin 40 mg (before)	Atorvastatin 40 mg (After)	Percentage Change	P value
Lipids, mg/dL				
Total Cholesterol (TC)	224.3±30.8	150.7±22.2	-32.81%	<0.001
LDL-C	158.3±22.6	83.9±15.1	-46.99%	<0.001
HDL-C	37.5±2.70	38.8±3.5	+3.46%	0.003
Triglyceride	165.8±30.8	141.4±22.6	-14.71%	<0.001
Non-HDL-C	180.6±31.2	113.2±18.1	-37.32%	<0.001
Glucose and HbA1C				
FBG, mg/dL	142.5±25.7	90.95±7.9	-36.17%	<0.001
HbA1c, %	5.82±0.2	5.71±0.3	-1.89%	0.198

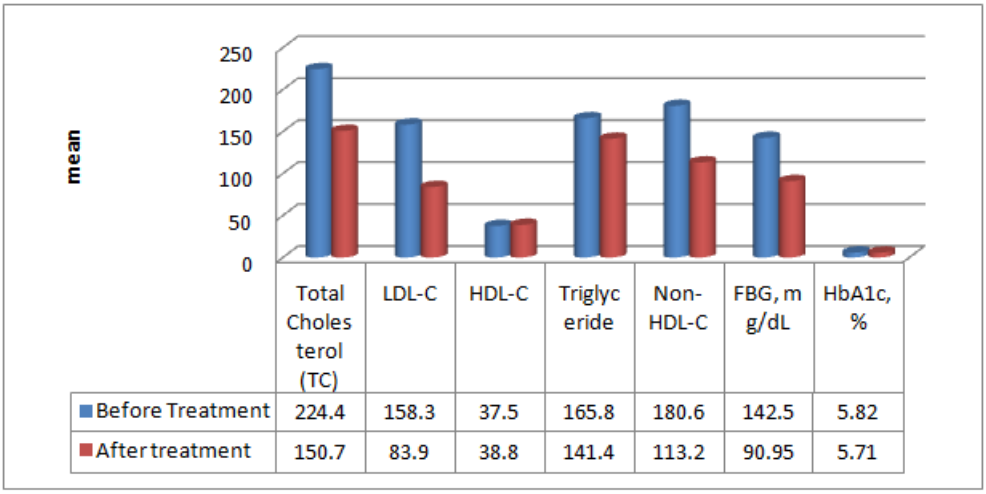


Table no3: Shows Percent Change in Lipids,(mg/dL) on a regular dose of Rosuvastatin 20mg for 6weeks. Total Cholesterol (TC)level reduced by(-26.49%), Low-density lipoproteins cholesterol(LDL-C) went down by (-37.28%), Triglyceride reduced to(-17.3%), Non-HDL-C went down by(-29.71%),after 6 weeks of medication. While there had been a reduction in the undesirable Lipids due to the above medication ,there was a positive upwards change in the desirable Lipids like high-density lipoprotein cholesterol (HDL-C) which improved by (+8.17%), Further, Fasting blood glucose, FBG, mg/dL level were reduced by (-37.95%). and HbA1c, % hemoglobin A1C test which measures blood sugar control over the preceding three months had also gone down by(-11.00%). The desirable alterations in respect of all the above parameters which were attributable to the above medication, were statistically significant, P<0.001---0.033.

Table no 3 : Shows Percent Change in Lipids,(mg/dL) on a regular dose of Rosuvastatin 20mg for 6 weeks**.**

	Rosuvastatin 20mg (before)	Rosuvastatin 20mg (After)	Percentage Change	P value
Lipids, mg/dL				
Total Cholesterol (TC)	226.1±35.4	166.2±25.7	-26.49%	<0.001
LDL-C	156.1±27.8	97.9±14.7	-37.28%	<0.001
HDL-C	35.5±2.21	38.4±3.6	+8.17%	<0.001
Triglyceride	164.6±28.2	136.2±23.4	-17.3%	<0.001
Non-HDL-C	182.4±29.2	128.2±20.5	-29.71%	<0.001
Glucose and HbA1C				
FBG, mg/dL	148.2±26.9	91.95±8.8	-37.95%	<0.001
HbA1c, %	5.62±0.4	5.5±0.2	-2.13%	0.187

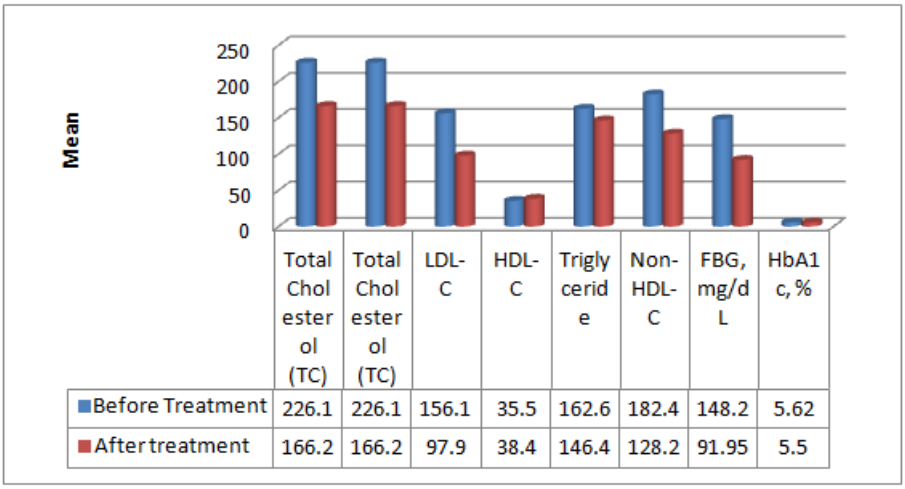


Table no4 Shows Percent Change in Lipids,(mg/dL) on a dose of Rosuvastatin 20mg on alternate Days for 6weeks. Total Cholesterol (TC)level reduced by(-26.36%), Low-density lipoproteins cholesterol (LDL-C) went down by (-37.53%), Triglyceride reduced by by(-11.63%), Non-HDL-C went down by(-29.71%),. While there had been a reduction in the undesirable Lipids due to the above medication ,there was a positive upwards change in the desirable Lipids like high-density lipoprotein cholesterol (HDL-C) which improved by(+8.17%), Further, Fasting blood glucose, FBG, mg/dL level were reduced by (-36.65%). and HbA1c, % hemoglobin A1C test which measures blood sugar control over the preceding three months had also gone down by(+4.07%). The desirable changes in respect of all the above parameters attributable to the above medication, were statistically highly significant, P<0.001---0.033 except HbA1c.

	Rosuvastatin 20 mg alternate day (before)	Rosuvastatin 20 mg alternate day (After)	Percentage Change	P value
Lipids, mg/dL				
Total Cholesterol (TC)	225.3±40.7	165.9±23.1	-26.36%	<0.001
LDL-C	157.2±26.7	98.2±16.3	-37.53%	<0.001
HDL-C	36.4±1.90	38.5±2.9	+5.76%	< 0.001
Triglyceride	166.8±35.7	140.4±21.9	-15.83%	<0.001
Non-HDL-C	185.2±32.4	127.2±19.9	-31.31%	<0.001
Glucose and HbA1C				
FBG, mg/dL	145.8±27.4	92.35±9.6	-36.65%	<0.001
HbA1c, %	5.65±0.3	5.66±0.4	+0.17%	0.287

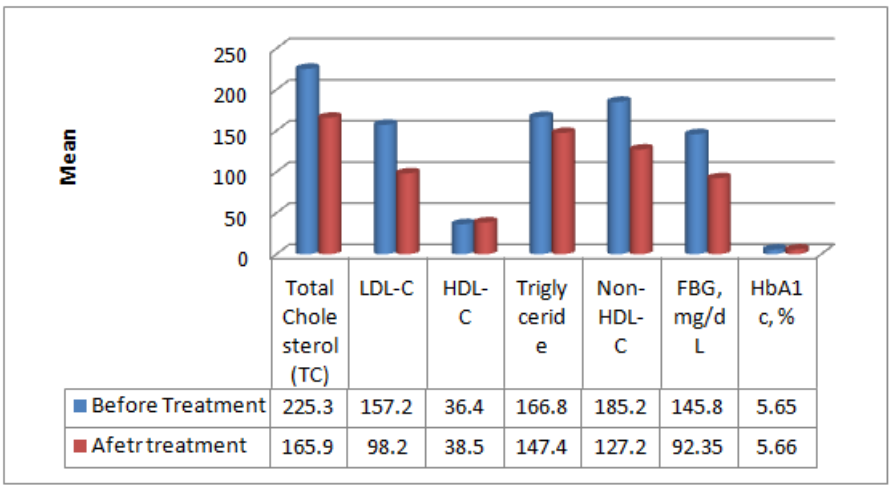


Table no 5 Shows metabolic parameters of patients of each of the three groups after 6 weeks of treatment. Metabolic parameters of patients of the three groups after 6 weeks of medication reveal that not only maximum quantities of harmful lipids like total cholesterol, LDL-C, Triglyceride, Non-HDL-C, Glucose, mg/dL ,have gone down, there was an increase in the useful lipids like HDL-C and in the patients treated with a regular dose of Atorvastatin 40 mg. In that group of patients the HbA1c, % level was also well within the normal range of4%

to 5.6%. The variation in the quantities of Total Cholesterol , LDL-Cand HbA1c, % among the patients of the three groups was statistically significant as P<0.001.

Table no 5 : Shows metabolic parameters of patients of each of the three groups after 6 weeks of treatment.

	Atorvastatin 40 mg	Rosuvastatin 20mg	Rosuvastatin 20 mg alternate day	P value (I to II)	P value (I to III)	P value (II to III)
Lipids, mg/dL						
Total Cholesterol	150.7±22.2	166.2±25.7	165.9±23.1	<0.001	<0.001	0.9309
LDL-C	83.9±15.1	97.9±14.7	98.2±16.3	< 0.001	< 0.001	0.8914
HDL-C	38.8±3.5	38.4±3.6	38.5±2.9	0.4266	0.5100	0.8290
Triglyceride	141.4±22.6	146.4±23.4	147.4±21.9	0.1259	0.0580	0.7554
Non-HDL-C	113.2±18.1	128.2±20.5	127.2±19.9	< 0.001	< 0.001	0.7267
Glucose and HbA1C						
Glucose, mg/dL	90.95±7.9	91.95±8.8	92.35±9.6	0.398	0.261	0.759
HbA1c, %	5.71±0.3	5.5±0.2	5.66±0.4	0.013	0.010	0.056

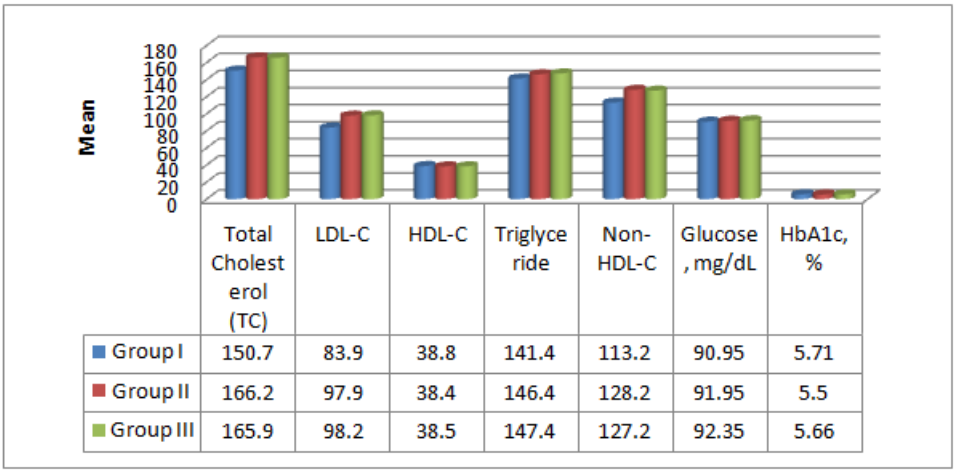
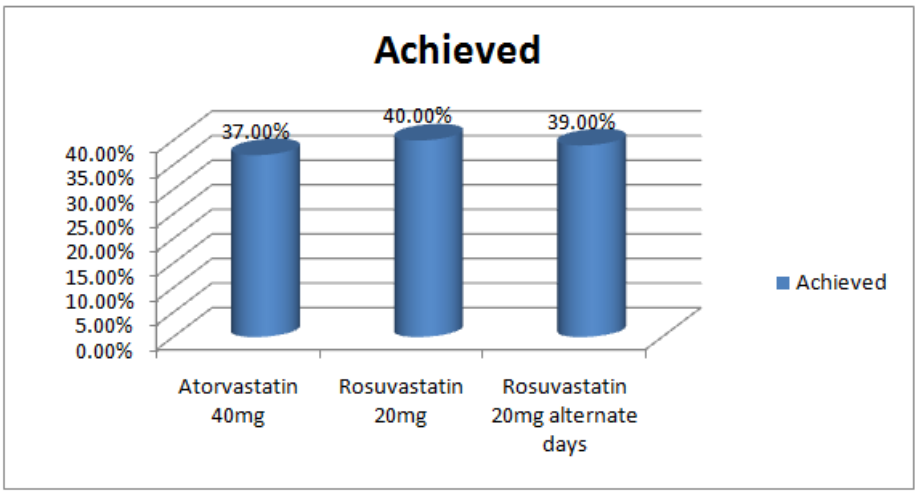


Table no 6 *National Cholesterol Education Program* NCEP ATP III goal. Figures show that while NCEP ATP III goal was achieved by40 (40%) patient treated with a regular dose of Rosuvastatin 20mg, 39 (39%)patient could achieve the goal with an alternate dose of Rosuvastatin 20mg . As for treatment with Atorvastatin 40mgwas concerned only 37 (37%) patient achieved the goal as stipulated by *National Cholesterol Education Program* NCEP ATP III goal.

Table no 6 : National Cholesterol Education Program NCEP ATP III goal**.**

Number of patients (%) achieving NCEP ATP III goal		
Statin therapy	Achieved (%)	Total
Atorvastatin 40mg	37 (37)	100
Rosuvastatin 20mg	40 (40)	100
Rosuvastatin 20mg alternate days	39 (39)	100
Total	116(38.66)	300



VIII. Discussion

Dyslipidemia in patients with diabetes plays an important role in development of atherogenesis. The standarded of treatment for dyslipidemia have been statins.For the treatment of dyslipidemia the most commonly used statins are are atorvastatin and rosuvastatin.

The four major statin beneficiary groups have already been defined by NCEP 2013 report.

There is a wealth of evidence suggesting that lowering low density lipoprotein cholesterol (LDL-C) reduces the risk of cardiovascular disease (CVD). Both European and US guidelines for CVD prevention recommend the use statins as first-line therapy for dyslipidemia and specify target LDL-C levels. Previously, a National Cholesterol Education Program (NCEP) report had proposed to lower target levels to even more aggressive LDL-C goals for very high-risk patients.

Despite the proven benefits of LDL-C reduction ,lipid managenent is suboptimal and many patients fail to achieve recommended LDL-C goals[11,12]. Themost likely reasons for this are the use of agents with poor efficacy for LDL-C lowering and suboptimal dose titration.

Such aggressive LDL-C goals,however are harder to achieve. The most effective statin at the lowest dose would represent a simple, effective treatment strategy, enabling more patients to achieve goals without the need for dose titration.

Rosuvastatin, at a dose of 20 mg, has demonstrated high efficacy for LDL-C lowering, enabling patients with hypercholesterolemia to achieve their lipid goals[10,11].

Currently no Indian study is available for treating diabetic patients with dyslipidemia or dyslipidemia alone with statin on alternate day and no previous study has documented the efficacy, safety and cost effectiveness of various statins prescribed to diabetic patients. Thus the present study aimed to build on this growing awareness of atherosclerosis-specific care of diabetes patients, by examining efficacy and safety of the two most commonly prescribed statins in India.

The present study was an open label prospective comparative study done in Department of General Medicine, at Dr. Ram Manohar Lohia Combined Hospital a tertiary care teaching hospital,Lucknow, Uttar Pradesh in the time interval of November 2014 to November 2015..

The study, shows that rosuvastatin (20mg daily and 20 mg on alternarnate days) was found to be the most effective statin at reducing LDL-C when compared with atorvastatin (40 mg) daily. In other words, rosuvastatin at its lowest dose in this study (20 mg) on alternate days was more effective at reducing LDL-C levels than atorvastatin at their higher dose (40 mg) daily. Our results are consistent with STELLAR trial which is one of the major open-label, randomized, and multicenter trials to compare rosuvastatin (10, 20, 40, or 80 mg) with atorvastatin (10, 20, 40, or 80 mg), pravastatin (10, 20, or 40 mg), and simvastatin (10, 20, 40, or 80 mg) across dose ranges for reduction of LDL-C[13]. The results of the STELLAR trial revealed that rosuvastatin was consistently, across all doses, the most effective at reducing LDL-C levels in comparison to all of the other statins.

Brunzell JD et al reported the lowering of triglycerides is another important goal in reducing CVD risk among diabetic patients.[5] In the present study, the greatest reduction in triglycerides was (−17.3%, $P < 0.01$) and was achieved by patients taking rosuvastatin (20 mg daily). This was the case, even in comparison with rosuvastatin 20 mg on alternate days and to higher doses of atorvastatin (40 mg). However, it is important to note that rosuvastatin (20 mg on alternate day) and atorvastatin (40 mg) both achieved the second highest reduction in triglycerides (−15.83%, $P < 0.05$, and −14.71%, $P<0.05$), respectively. These findings are similar to the majority of studies in the literature, which have shown a slightly higher reduction in triglycerides in patients taking rosuvastatin in comparison to atorvastatin as reported by Clearfield MB et al.[14]. It thus appears that, reduction in

triglyceride levels is equal with rozuvastatin and atorvastatin in relation to this factor (triglycerides), and that both rosuvastatin and atorvastatin are effective in reducing it.

Raising HDL-C levels is another major factor known to reduce CVD risk. In the present study, all of the statins were found to increase HDL-C levels as has been shown in previous studies. Rosuvastatin (20 mg daily) lead to maximal increase (+8.17%).

IX. Conclusion

Rosuvastatin 20 mg on every other regimen had equal effect when compared to daily dose regimen of atorvastatin 40 mg &rosuvastatin 20mg.

References

[1]. National Cholesterol Education Program (NCEP) Expert Panel on Detection, Evaluation, and Treatment of High Blood Cholesterol in Adults (AdultTreatment Panel III) Third report of the national cholesterol education
[2]. program (NCEP) expert panel on detection, evaluation, and treatment of highblood cholesterol in adults (adult treatment panel III) finalreport. Circulation. 2002;106(25, article 3143).
[3]. Bener A, Zirie M, Janahi IM, Al-Hamaq AOAA, Musallam M, Wareham NJ.Prevalence of diagnosed and undiagnosed diabetes mellitus and its risk factorsin a population-based study of Qatar. Diabetes Research and Clinical Practice. 2009;84(1):99–106.
[4]. Bener A, Zirie M, Musallam M, Khader YS, Al-Hamaq AOAA. Prevalence ofmetabolic syndrome according to adult treatment panel III and internationaldiabetes federation criteria: a population-based study. Metabolic Syndrome
[5]. and Related Disorders. 2009;7(3):221–230
[6]. Bener A, Dafeeah E, Ghuloum S, Al-HamaqAOAA.Association between psychological distress and gastrointestinal symptoms in type 2 diabetes mellitus. World Journal of Diabetes. 2012;3(6):123–129
[7]. Brunzell JD, Davidson M, Furberg CD, et al. Lipoprotein management inpatients with cardiometabolic risk:consensus statement from the American diabetes association and the american college of cardiology
[8]. foundation.Diabetes Care. 2008;31(4):811–822
[9]. Colhoun HM, Betteridge DJ, Durrington PN, et al. Primary prevention of cardiovascular disease with atorvastatin in type 2 diabetes in the collaborative atorvastatin diabetes study (CARDS): multi centrer trial. The Lancet. 2004; 364(9435) :685–696.
[10]. Shepherd J, Barter P, Carmena R, et al. Effect of lowering LDL cholesterol substantially below currently recommended levels in patients with coronary heart disease and diabetes: the treating To new targets (TNT) study.Diabetes Care. 2006;29(6):1220–1226.
[11]. American Diabetes Association.Standards of medical care in diabetes. Diabetes Care. 2009;32(supplement 1):S13–S61.
[12]. Henry RR. Preventing cardiovascular complications of type 2 diabetes: focus on lipid management. Clinical Diabetes.
[13]. Jones PH, Davidson MH, Stein EA, et al. Comparison of the efficacy and safety of rosuvastatin versus atorvastatin, simvastatin, and pravastatin across doses (STELLAR* trial) American Journal of Cardiology.2003;92(2):152–160.
[14]. Group EUROASPIREIIS: Lifestyle and risk management and use of drug therapies in coronary patients from 15 countries.
[15]. Principal results from EUROASPIRE II. Eur Heart J 2001,22:554-572.
[16]. Schuster H, Barter PJ, Cheung RC, Bonnet J, Morrell JM, Watkins C, Kallend D, Raza A, for the MERCURY I Study Group: Effects ofswitching statins on achievement of lipid goals: MeasuringEffective Reductions in holesterol
[17]. Using Rosuvastatin Therapy (MERCURY I) study. Am Heart J 2004,147:705-713.
[18]. Pharmaceutical Management Agency. Prescription for pharmacoeconomic analysis: methods for cost-utility analysis.