

Design of programmable gain amplifiers for Bio-Medical Applications

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Abstract— With growing demand for bio medical electronics, healthcare monitoring and AI integrated bio medical applications, bio medical sensor and signal processing has become a vital part of the industry. The most important part of the biomedical electronics is to interface the sensor with the nervous system of the subject, sense the neuro transmitted signal, amplify the signal to machine readable amplitude, sample the signal, convert it to digital for and perform DSP. Instrumentation amplifiers are the crucial part of these biomedical sensors not only in terms of EEG, ECG and other lifesaving technologies but also in brain signal detection and modification. This paper talks about the crucial intermediate step of amplification of sensed neural transmitted signals to the level that can be read by Sampling circuits and ADCs.

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I. INTRODUCTION

This paper aims to present a programmable gain amplifier for brain signal detection in the range of 2 Hz to 70 Hz extended up to 250 Hz. The detected signal needs to be free of device noise, supply noise and any other harmonics that can be added during signal amplification. Hence, features like Output noise, Offset, PSRR and linearity become the crucial parts of the PGA design.

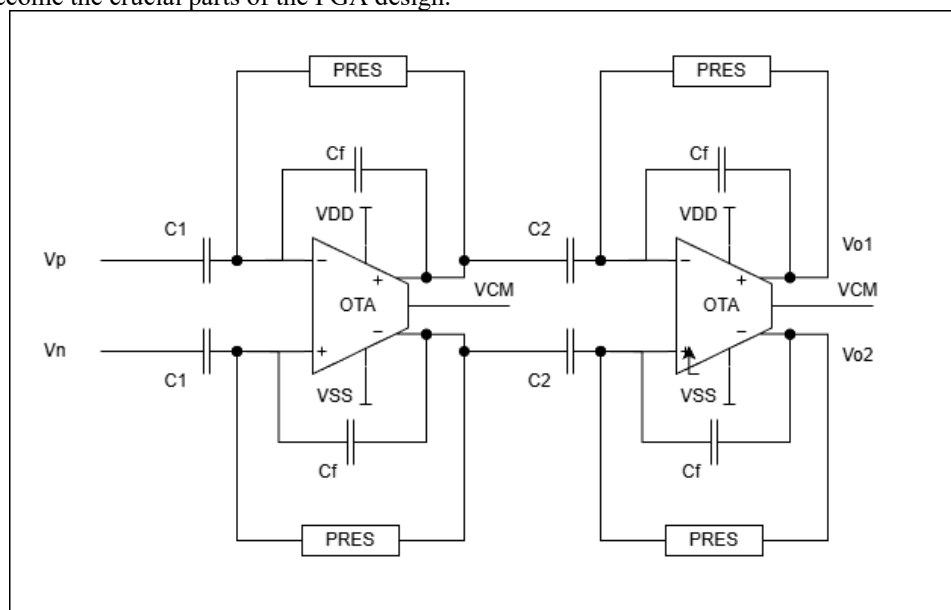


Fig. 1. Proposed schematic

This paper aims to present one of the widely used solutions with folded cascode architectures which includes features like chopping and low power, low bandwidth design. This PGA is designed in Cadence Virtuoso tool in 180nm technology. The paper explains in detail about the building blocks, gain control and crucial elements of the PGA design.

II. FULLY DIFFERENTIAL AMPLIFIER

Fully differential amplifiers are the core of the PGA for bio medical applications. The main requirements of a fully differential amplifier. Folded cascode architecture is a preferred architecture as high gain is preferred at low power consumption and low noise specifications. The bias points are externally generated, and the common mode feedback is taken care with a simpler OTA architecture. High PSRR and CMRR are also the preferred characteristics of this OTA.

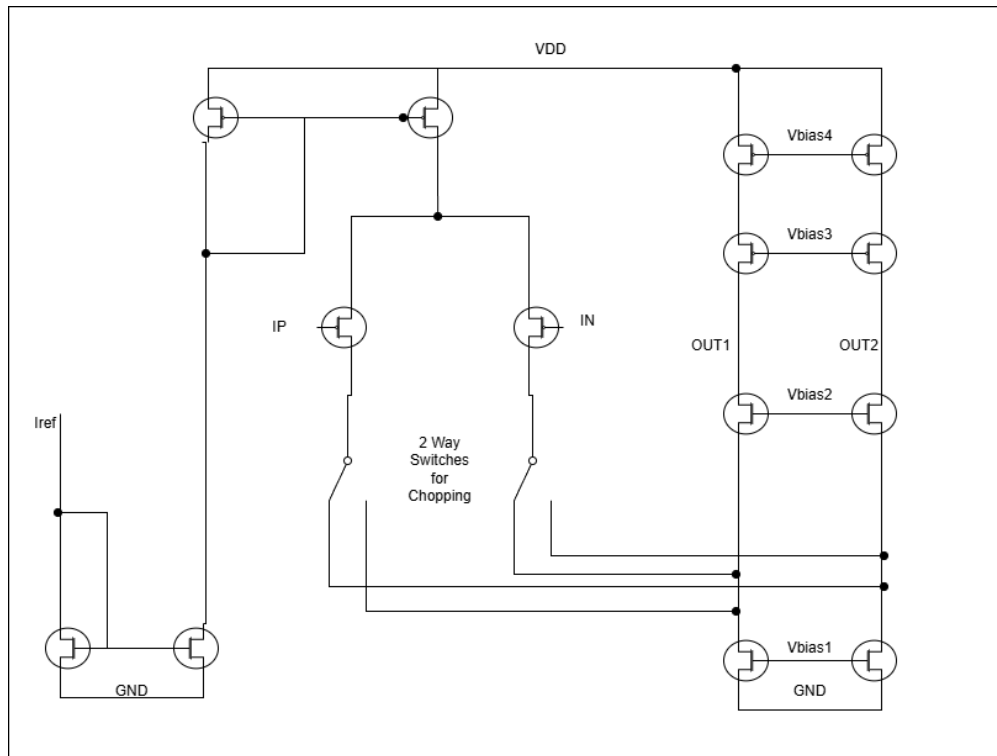


Fig. 2. folded cascode architecture with chopping

The above figure shows chopping enabled folded cascode op-amp architecture used in this design. This architecture also includes a common mode feedback loop which is beyond the scope of this paper.

III. DESIGN OF FEEDBACK CIRCUIT AND PROGRAMMABILITY

Feedback circuits are designed using capacitive feedback in the case of bio medical applications. This helps avoid the thermal noise that is generated out of the resistance feedback circuits. This leaves us with the problem of bias point setup. Hence a large pseudo resistance is used complete the feedback loop as discussed in section V.

The loop Feedback is given by the expression C_{in}/C_{fb} in case of this fully differential architecture.

Expected Gain	Cf (fF)	C1 (fF)	C1 segment (fF)	Cf (fF)	C2 (fF)	C2 segment (fF)	Stage 1 Gain	Stage 2 Gain	Final Gain
0.5	100	50	50	100	100	100	0.5	1	0.5
143	100	1430	1380	100	1000	900	14.3	10	143
286	100	2860	1430	100	1000	500	28.6	10	286
429	100	2860	-	100	1500	500	28.6	15	429
572	100	2860	-	100	2000	500	28.6	20	572
715	100	2860	-	100	2500	500	28.6	25	715

858	100	2860	-	100	3000	500	28.6	30	858
1000	100	2860	-	100	3500	500	28.6	35	1001

Table. 1. Gain programmability setting

IV. THERMOMETRIC DECODER FOR GAIN CONTROL

A Thermometric Decoder in simple words measures how many 1s are in a binary representation of a number. This is an important part of the PGA design as it uses capacitor feedback system. Here changing the gain is easy compared to resistor feedback systems. In this case, the feedback capacitor is directly increased or decreased by adding and removing the capacitor banks in parallel. And thermometric decoder provides proper scaling using a 3:7 decoder implementation.

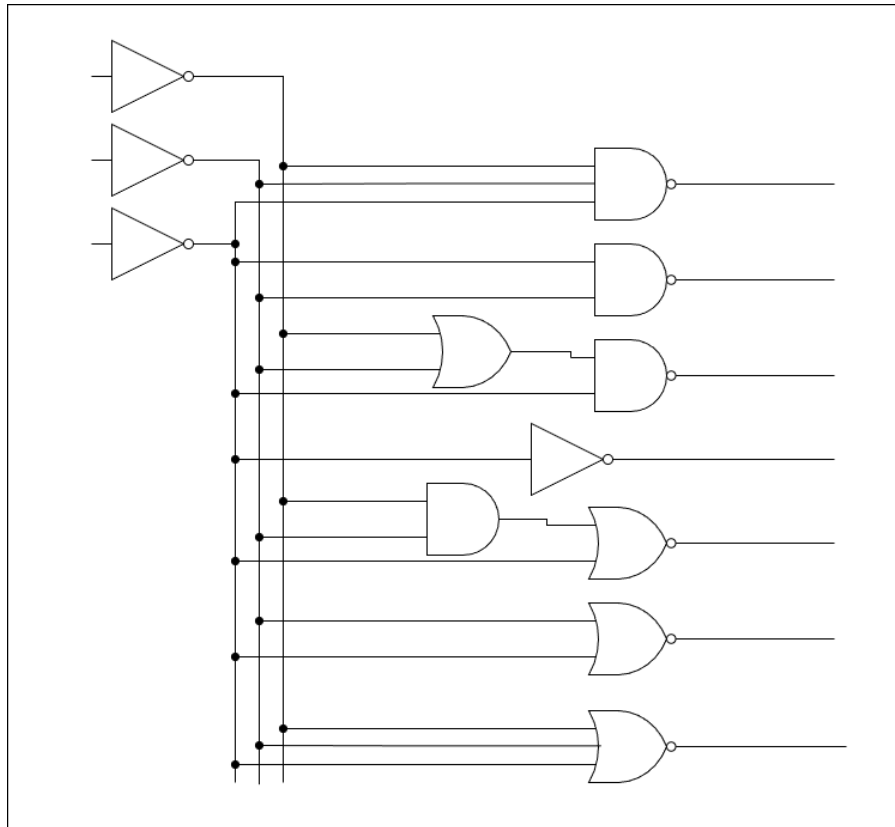


Fig. 3. 3 to 7 thermometric decoder

Gain2	Gain1	Gain0	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

Table 2. Thermometric decoder setting

The detailed setting of the capacitor segments in discussed in section III. The thermometric decoder is used to sequentially add or remove the capacitors to the C1 and C2 sections to adjust the gain.

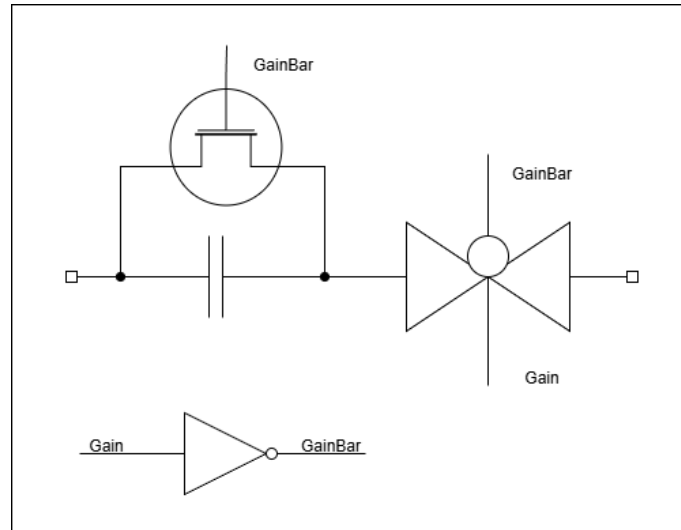


Fig. 4. Gain segment

The above figure shows the gain segment of a capacitance. Whenever a segment is added to the gain, the switch across the capacitor is turned off and the transmission gate is turned on. When it is disconnected from the gain block the transmission gate is turned off and the switch across the capacitor is shorted. It is important to make sure these segments are in parallel and the Transmission gate is connected to the input of the op-amp and not the output of the previous stage.

V. PSEUDO RESISTOR DESIGN AND CONTROL

Pseudo resistors are used to set common mode feedback in the PGA. Also, it eliminates the offsets in the low frequency range of the biomedical signals is between 0.1 Hz to 10 kHz, while the amplitude range is around $20\mu V - 10\text{ mV}$. But the offset of the amplifier itself ranges between 1mV to 50mV. In such cases a high pass filter needs to be implemented using a pseudo resistor and capacitor combination. The body diode of the mosfet under 0.2V forward bias acts as a large resistance. And since we can pack capacitors on chip cannot exceed few pF. By this relation we design a high pass filter using the relation $f=1/2\pi RC$.

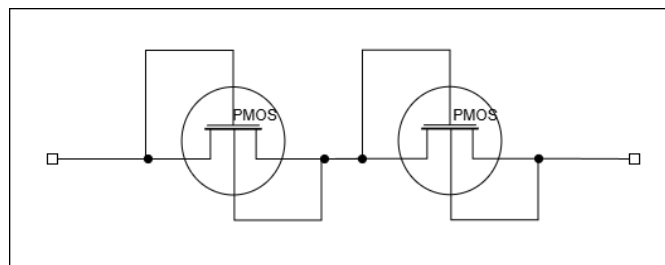


Fig. 5. Pseudo resistor

These pseudo resistors offer resistance from order of $M\Omega$ to $T\Omega$. depending upon the technology, fabrication, and the design node. Separate experimental tests with ideal capacitor needs to be run with simple 1st order filters to determine the pseudo resistance. It is also crucial to ensure the body diode models are accurate.

VI. SIMULATION RESULTS

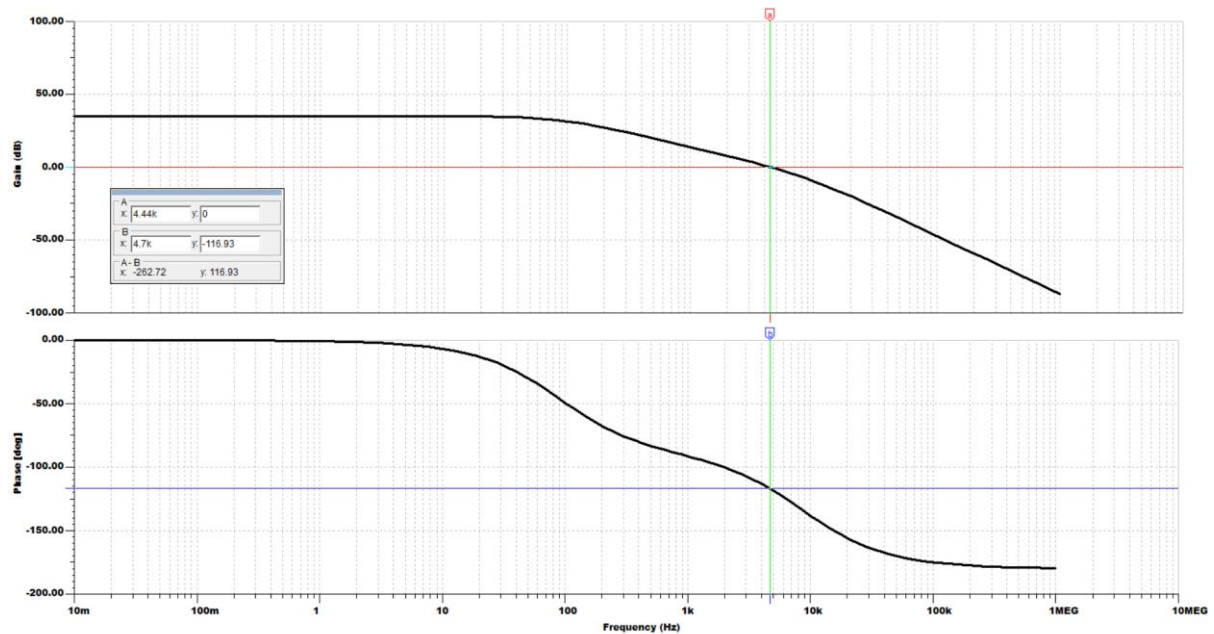


Fig. 4. OTA gain and bandwidth

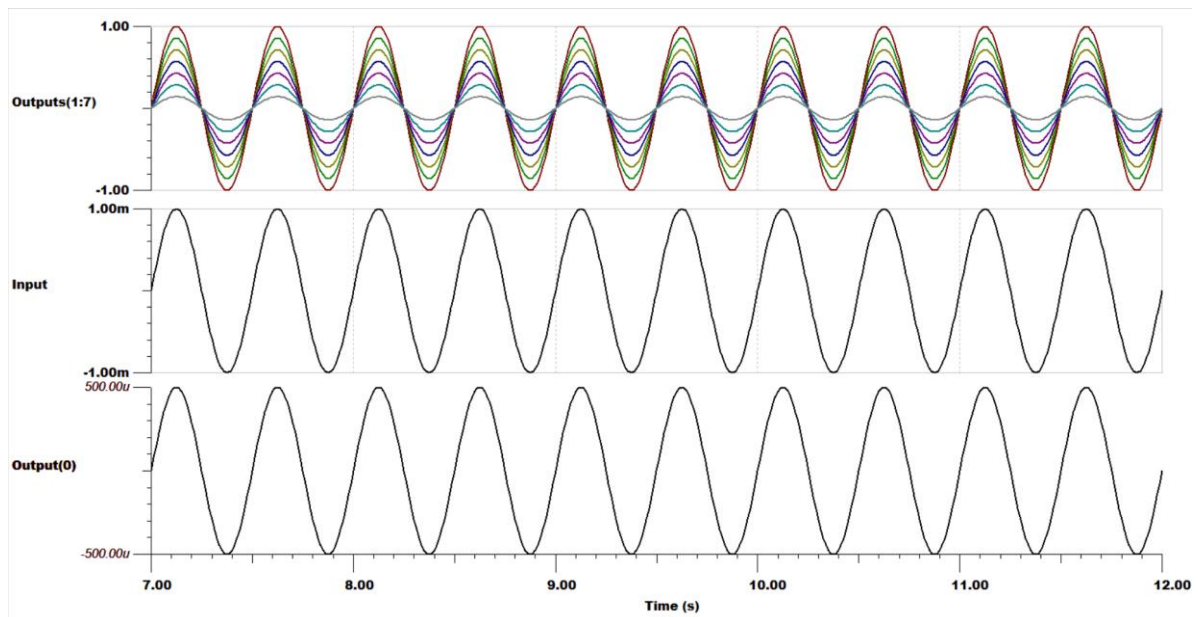


Fig. 6. Transient results

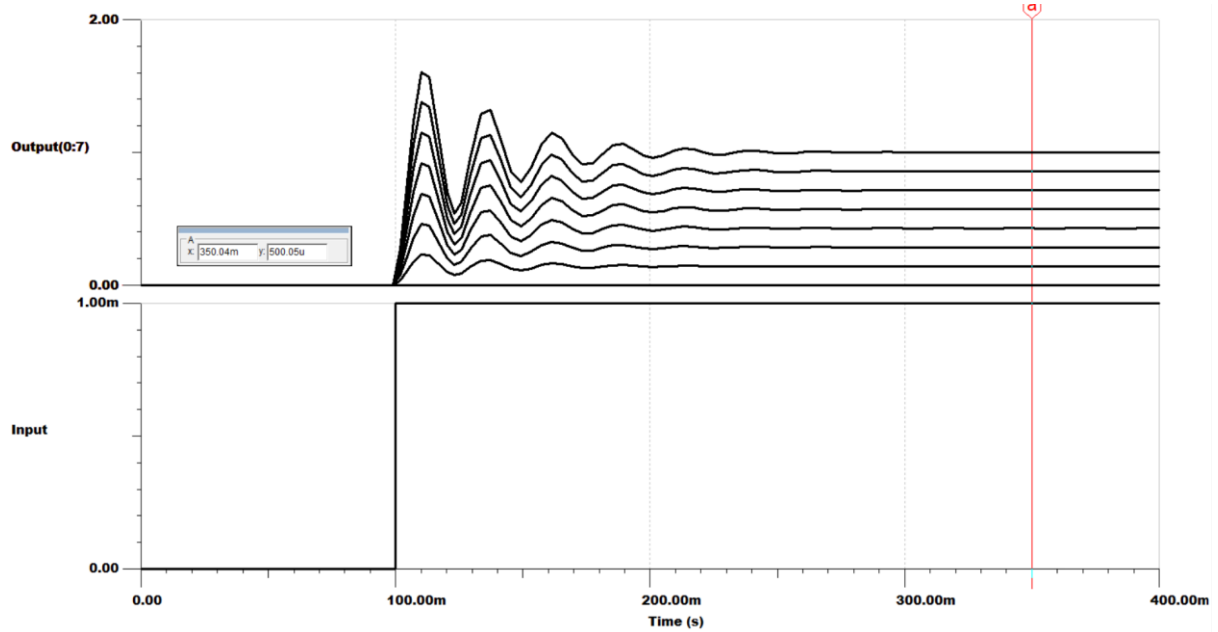


Fig. 7. Transient stability analysis

SLNO	Parameter	Description	Min	TYP	Max	Units
1	VDD	Supply Voltage	1.62	1.8	1.98	V
2	TEMP	Operating Temperature	0	25	60	°C
3	IQ	Power consumption			12	μA
4	GAIN	Gain 0:7 0.5 to 1000	0.5		1000	V/V
5	INTEGRATED NOISE	Integrated noise 2Hz to 70Hz	13.8	44.1	92.08	pV/Hz ²
6	PSRR	PSRR DC	79.8	80.24	88.11	dB
7	PSRR 250Hz	PSRR at 250Hz	77.18	78.63	82.13	dB
8	Linearity	Linearity slope (gain vs amplitude)	0.83	0.91	0.989	V/V
9	Area	Total Area in mm ²			0.65	mm ²
10	Amplitude	Maximum input Amplitude			1	V

Table 3. Figures of merit

VII. CONCLUSION

The PGA design for low noise and low power application has been implemented. Component selection and design methodology has been explained. The figures of merit and simulation results have been discussed. The advantages of the introduced techniques and the drawbacks of traditional amplifiers have been discussed in detail.