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Design And Implementation Of 44 Vedic Multiplier With Reduced Transistor Count And Competitive Power Consumption

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Abstract
The multiplication is one of the most important arithmetic function in Digital signal processing, ALU and various communication systems. The Multiplication method require more hardware resources and more time than other arithmetic and logical circuits such as Addition, Subtraction etc. But the need for fast computation along with low on chip area and the low power dissipation is increased in recent times. In recent years, lot of work has been done to improve speed of multiplier while reducing transistor count(on chip area).The different designs such as Array multiplier, Wallace-tree multiplier and Vedic multiplier are proposed. The Vedic multiplication is based on the ancient Indian literature called as sutras.
In this paper we have proposed architecture of 44 Vedic multiplier based on the Urdhva-Tiryagbhyam sutra along with some modifications in it. It uses the standard designed blocks such as AND gate, OR gate, Half Adder and the Full Adder blocks to implement the 2 vedic multiplier. Then with help of designed 44 vedic multiplier further 44 vedic multiplier is designed. This 44 multiplier is design and simulated in the cadence virtuoso software with the help of 180 nm technology. The results of proposed design show an improvement of approx 70% in the on chip area and 73% less delay in comparison to CMOS Vedic multiplier.
Key words:- *Vedic Multiplier, 180 nm, Cadence Virtuoso, Transistor count.*

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I. Introduction To Vedic Multiplication

Multiplication is a mathematical operation. The Number repeatedly added to itself for the specific number of times. For example if A multiplied by B, then A is added B times with itself Multipliers required more on chip area and propagation time, than other arithmetic operations. Processors spend enormous amounts of time and a lot of hardware on multiplying, in order to make the multiplication as fast as possible [1].So, considering this the design of hybrid vedic multiplier is proposed as seen in Figure 1 and implemented using the CADENCE Virtuoso in 180 nm Technology.

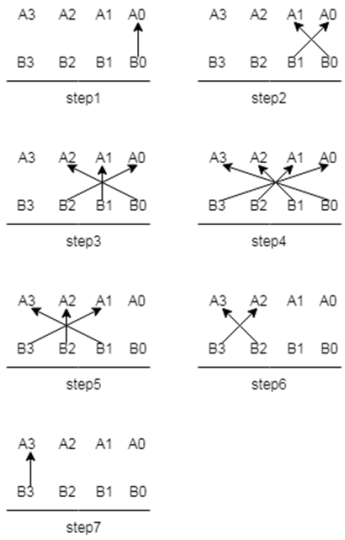

Figure 1: Basic vedic multiplication method

Vedic Mathematics is a system of mathematics that originated in ancient India and is based on the Vedas, which are ancient Hindu scriptures. This system is known for its unique and efficient techniques for performing mathematical calculations, including multiplication. There are special 16 sutras which describe the vedic Multiplication. Like Ekadhikina Purvena, Nikhilam Navatashcaramam Dashatah, Paraavartya Yojayet. These sutras describe the natural way of solving mathematical problems. Vedic Multiplier complexity is less as compared with any of other type of multiplier such as booth multiplier architecture[2], Array multiplier[3], Walles-tree multiplier[4] etc. Vedic multiplier hardware uses less no of transistors. Therefore Vedic multiplier has more advantages in the terms of on chip area or transistor count, propagation delay [5], power dissipation and complexity. In simple way it gives high performance [6] in compare to others. Using these techniques in the computation algorithms of the co-processor will reduce the complexity, execution time, area, power etc.

We basically worked on the URDHVA- TIRYAGBYHAM which is nothing but multiplication vertically, cross wise and then addition. This technique is shown in figure.1. We have worked on some similar technique but with small changes in it. This works by separating the one 4 bit number into 2 different 2 bit numbers. Then we can multiply the 4 bit number by 2 bit numbers separately ex. A3A2A1A0 is first number and B3B2B1B0 is second number which we have to multiply.ThentheBisgetdivideinto2groupslike(B3 B2) are MSB bits and (B1 B0) are LSB bits. Modified 42multiplication shown in Figure.2.

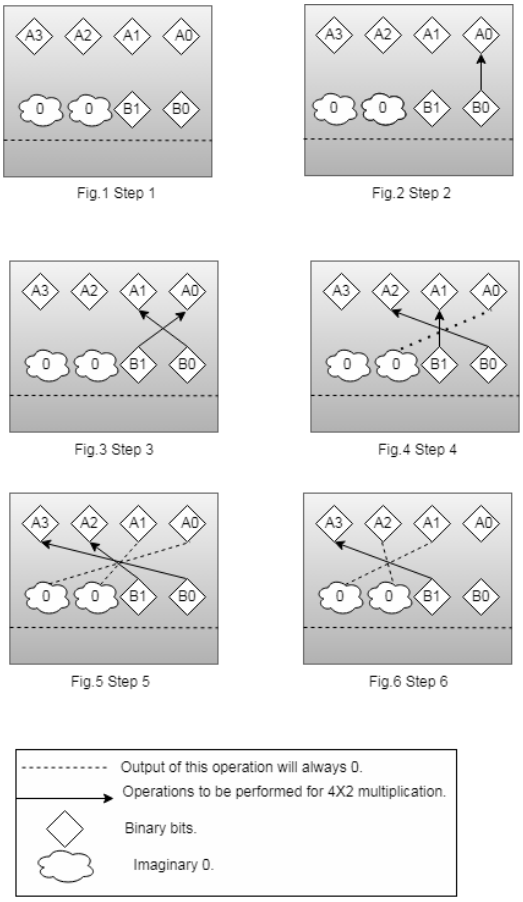

Figure 2: Modified 42 multiplication method

II.Design

According to the URDHVA-TIRYAGBYHAM the vedic multiplier is designed below. The 42 vedic multiplier block and with help of this block the 44 vedic multiplier is designed.

Design Of 42 Vedic Multiplier

As per shown in Figure.2, the 42vedic multiplier is designed. The output equations of 42 Vedic Multiplier is

Y0=A0.B0
Y1=A1.B0+A0.B1
Y2=A2.B0+A1.B1+C0 Y3=A3.B0+A2.B1+C1 Y4= A3.B1 + C2
Y5=C3

The Modified 42 Vedic multiplier is shown in the Figure.3 below

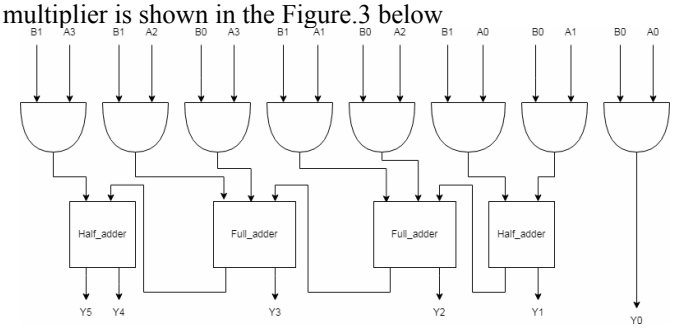

Figure 3: Modified 42 VEDIC Multiplier Block Diagram

Design of 44 Vedic Multiplier

Using the designed module of 42 vedic multiplier the 44 vedic multiplier is designed as shown in Figure 4. In Design of 44 vedic multiplier 2 blocks 42 multiplier is used along with half adder [7], full adder [8]

AND OR gate circuits for the addition of bits.

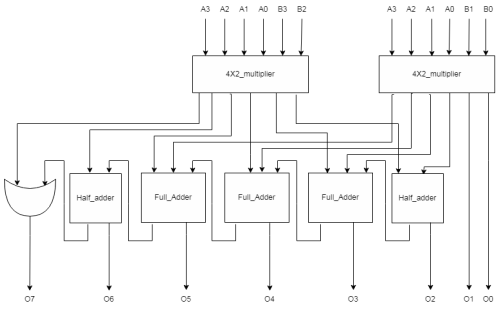

Figure 4: Modified 44 VEDIC Multiplier Block diagram

III. Experimental

The schematic and simulation results of the standard blocks along with Proposed design's is given below figures. For the design of 42 vedic multiplier AND gate, OR gate, HALF ADDER and FULL ADDER is used. To design the 44vedic multiplier the OR gate alongwith above mentioned circuits is used.

AND Gate

We designed the AND gate by CMOS approach, it have less power dissipation and less delay along with good voltage levels. The results of the simulation is given below in Figure.5.

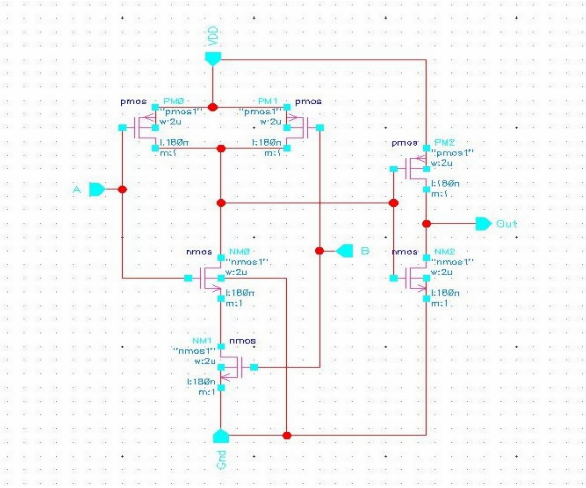

Figure 5 : Conventional AND gate diagram

OR Gate

We designed the OR gate by CMOS approach, it have less power dissipation and less delay along with good voltage levels. The results of the simulation is given below in fig- ure.6.

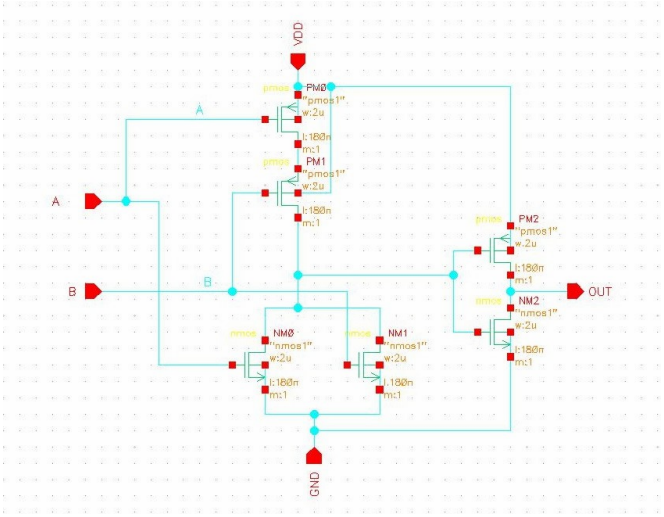

Figure 6: Conventional OR gate diagram

Half Adder

Half adder is a basic digital circuit which performs the addition of two binary bits. It is one of the most important circuit in Arithmetic addition of binary numbers. There are lots of ways to design the Half adder circuit. Like us- ing EXOR gate and AND gate[**?**], using pass transmission logic etc. We have designed the Half Adder using 10 transistor with Hybrid logic. The schematic and the results of the 10T half adder circuit is given below in Figure. 7 .

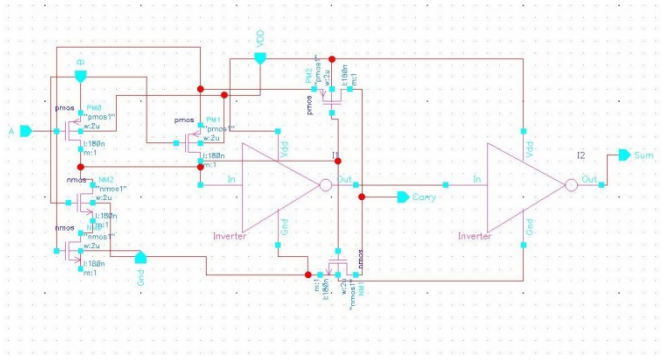

Figure 7:10T modified half adder diagram

The results of Half adder is verified on the frequency of 500MHz.The circuit gives the output as sum and carry. The result of the above represented 10T half adder circuit is shown in Figure. 8

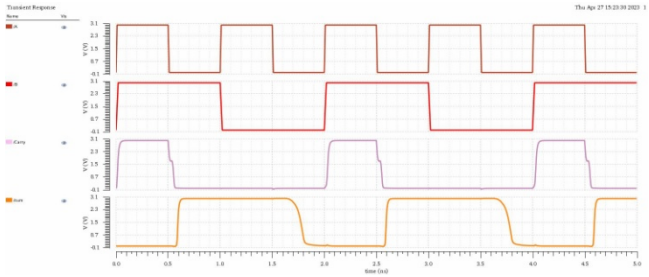

Figure 8: 10T modified half adder Result

Full Adder

The full adder circuit is basic digital circuit which is used for the addition of the three one bit binary number and generate the result in form of the sum and carry. Similar as the half adder, full adder [9] can be designed using many different approaches. Basic full adder can be de- signed using the 2 half adder and 1 OR gate circuits. We have designed the Full adder using the 20T modified full adder design approach. The 20T full adder is shown in schematic diagram given in Figure.9.

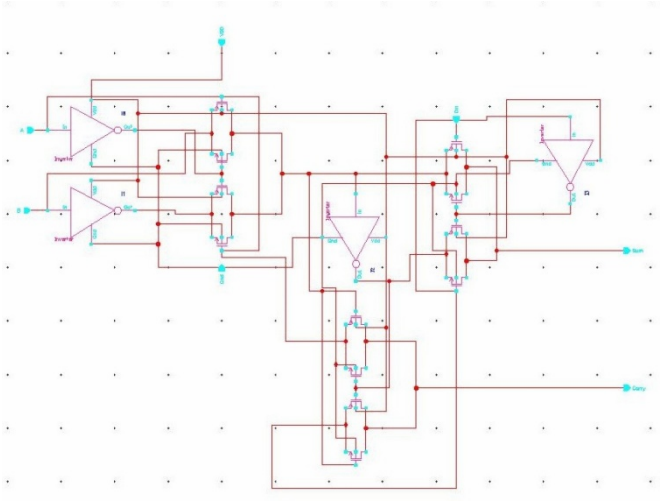

Figure 9:20T modified full adder diagram

The results of Full adder are verified on the frequency of 500 MHz. The results shown in Figure.10 below

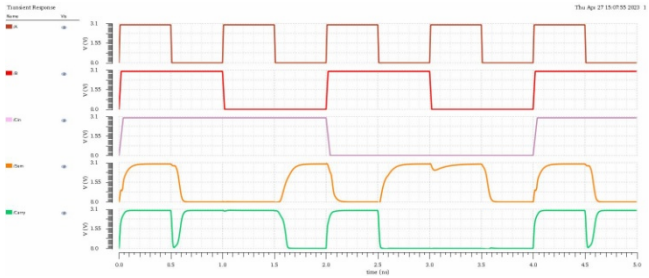

Figure 10:20T modified full adder Result

42 Vedic Multiplier

The 42 vedic multiplier is designed using all the blocks above mention such as Half adder, Full adder, OR gate and AND gate. The schematic diagram of the 42 vedic multiplier is shown in below Figure.11

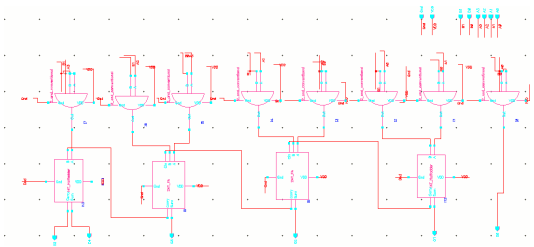

Figure 11: Modified 42 multiplier schematic

The results of the 42 Vedic multiplier is shown below in Figure.12

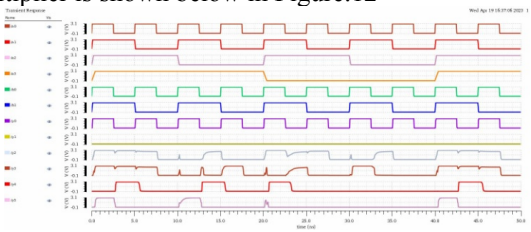

Figure 12: Modified 42 multiplier Result

44 Vedic Multiplier

Our final objective is to design 44 vedic multiplier [10]. We used the basic block of half adder, full adder and 42 vedic multiplier to design it.The schematic of this blockis shown below in Figure.13

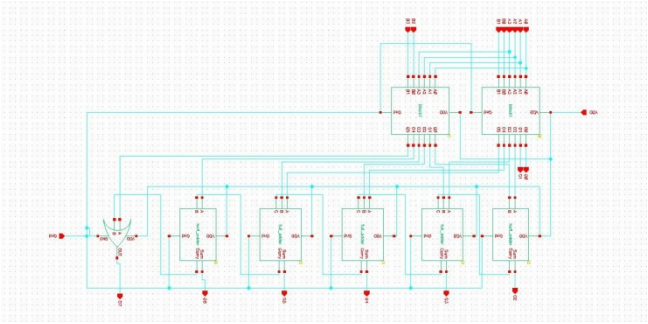

Figure 13:Modified schematic of 44 vedic multiplier

The simulation results of the modified 44 vedic multiplier is shown below in Figure.14.The A3A2A1A0 And B3B2B1B0 are the inputs for multiplier [6] while the O0-O7 are the outputs.

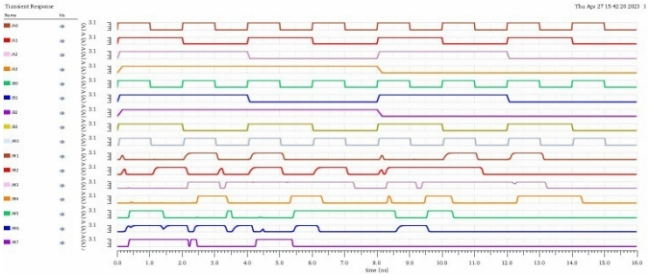

Figure 14: Modified 44 vedic multiplier result

The result of vedic multiplier is verified at the frequency of 500MHz.

IV. Result And Comparative Analysis

The comparison and analysis of the Vedic multiplier [6] in terms of the Transistor count, Power dissipation and Delays is given below in table.1 and also the graph of the data is shown below in Figure 15-17.

Table.1

Design	No.of Transistors	Power dissipation	Delay
CMOS	998	11.188ns	17.034nW
CPL	1146	12.068ns	30.849nW
DPL	920	11.293ns	25.599nW
Using SERF adder	400	1.23ns	2.11uW
Conventional adder	520	0.39ns	9.55uW
Using 1BIT adder	520	1.45ns	9.07uW
Using DPL adder	616	2.31ns	4.47uW
Using TX-GATE adder	445	3.01ns	3.11uW
Array multiplier	554	34.04ns	745.7uW
Vedic multiplier	464	27.09ns	741.3uW
Wallace-tree multiplier[11]	500	31.96ns	752.2uW
Vedic multiplier	464	27.09ns	741.3uW
Proposed Modified Vedic Multiplier	**302**	**2.931ns**	**5.09uW**

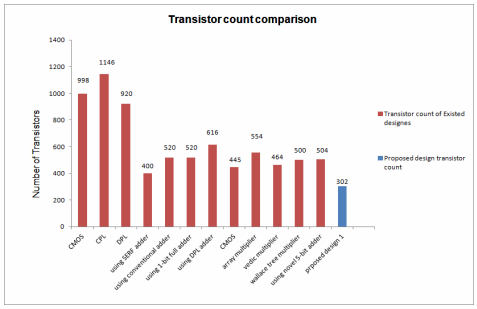

Figure 15: Transistor count comparison

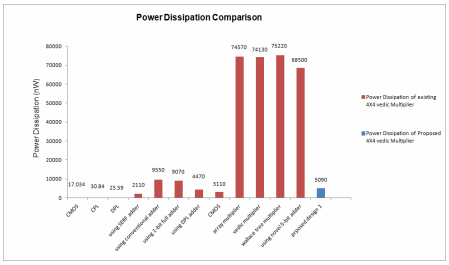

Figure 16: Power dissipation comparison

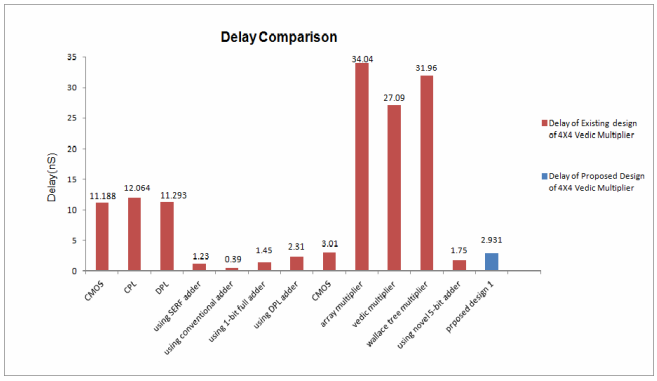

Figure 17: Delay comparison

V. Conclusion

The results of proposed design 1 shows the improvement of approx 70% in the number of transistors and 73% less delay but it has high power dissipation in comparison to CMOS Vedic multiplier. All though this circuit have high propagation delay (Tpd) in compare to some other designs shown in table.1.So,the analysis shows that by using the proposed architecture for Vedic multiplier the NO. of transistor required will reduce significantly.

Future Plan

Future work can include the reduction of the power dissipation and dependency of performance on change in technology trend and implementation of same architecture for higher bit size.

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