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Design Steps, Simulation, and Analysis of a 1-bit ALU in Cadence at 90 nm CMOS Node

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Abstract:
This paper presents the design and analysis of a 1-bit Arithmetic Logic Unit (ALU) with and without a full adder circuit. The objective of the study is to compare the outputs of the two designs considering the performance factors of delay, power, and surface area. The designs were implemented using Cadence Virtuoso and simulated using a 90 nm CMOS process technology. As such, the circuit is built from two paired MOS transistors (i.e., using both N- and P-type MOSs in the pull-down and pull-up circuits, respectively) having a 90 nm gate length. The gate widths are selected as 1 and 2 □m, respectively. Transistors are nominated from the general design CMOS process kit at 90 nm technology node, i.e. gpdk090 library of the Cadence. DC, transient, and noise analyses were performed with a 3.8 V DC power supply to characterize the behavior of the circuits. The results indicate that the ALU without the full adder has lower delay and power consumption but a larger area, while the ALU with the full adder has higher delay and power consumption but a smaller area. The findings of this study can provide insights for designers to choose the appropriate ALU design based on their specific requirements and provide a confidence boost up before going into the fabrication steps.

Keywords*: CMOS; ALU; Logic Gate; Adder; Performance Analysis; Cadence; 90 nm Node; VLSI.*

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I. Introduction and Background Knowledge

There is an increasing demand for high-speed and low-power consuming devices, such as laptops, tabs, smartphones, etc. in the recent time. That provokes numerous research exertions in the semiconductor device and associated circuit design and manufacturing industries. However, the tremendous progress works in the VLSI circuit design industry is going on following the Moore's law to double transistors on a Si chip every 3 years [1-3]. In fact, the MOS transistors' sizes are scaled down continuously, but the interconnections have also increased at the same time to impede the transistors' increment in a smaller chip. In the Very Large Scale Integrated (VLSI) circuits, MOSFET is the rudimentary efficient component [1]. As this component's size is being curtailed progressively to provide accommodations for more devices in the equivalent amount of space in an assimilated circuit conforming the Moor's law [1-2]. Nevertheless, the abridged version of transistors possess numerous unfavorable impacts, such as short channel effects or SCE [3-4], low-frequency drain current flicker noise difficulties [5, 6], subthreshold regime drain current consequences [7-8], electron or hole mobility dilapidation in the inversion channel region [9], surface potential barrier dropping problem [10-11], temperature effects on diverse operating parameters of the MOS devices [12-13], etc. Therefore, the behavior of the VLSI circuits must be investigated using a professional simulator, like Cadence tool [14].

At present, microprocessors are indispensable to design and fabricate diverse electronic products, such as radio, smart TV, smartphones, home appliances, laptops, computers, etc. MOS transistors are the key constituents for the microprocessors [1-2]. The major challenges to design a microprocessor are to get optimum speed, power, bandwidth, cost, efficiency, supply rail voltage drop, interconnect noise, crosstalk, reliability, clock distribution, etc. [1-2]. The Arithmetic Logic Unit (ALU) is the principal part of in a computer and a full adder is the core part of an ALU [15-16]. Therefore, the designed adder circuit for the ALU has to meet these area, power, and speed requirements, at least. Therefore, the objectives of this research work are to-

1. Design and simulate a 1-bit ALU with basic logic gates (AND, OR, XOR, NOT) using Cadence tool with its general purpose CMOS process design kit of 90 nm, i.e., gpdk090.
2. Test the functionality of the 1-bit ALU by incorporating a full adder to perform addition operations.
3. Implement and test the functionality of the 1-bit ALU by performing transient analysis and comparing the results with expected values using Cadence tool.

4. Perform DC analysis to analyze the behavior of the 1-bit ALU under varying input conditions.
5. Conduct a parametric analysis to evaluate the performance of the 1-bit ALU with respect to different parameters.

Currently, the available working technology nodes in Cadence simulation tool are 180, 90, 65, and 45 nm [17]. In this work, we designed and analyzed a 1-bit ALU circuit at a 90 nm technology node.

II. Literature Review and Problem Statement

In the literature, it was found that advanced digital circuits were designed using Cadence tool, such as ALU was designed and implemented using reversible logic [18] or multiplexer for the ALU using Quantum Dot Cellular Automata (QCA) [19].

Another research paper explored the design of a 1-bit ALU by means of several full adders, such as Transmission Gate (TG), Complementary Metal Oxide Semiconductor (CMOS), Gate Diffusion Input (GDI), and Modified GDI logic. The authors of this paper mainly designed 1-bit ALUs using diverse full adders to get low-power and high-speed circuit operation with wide voltage swing. From their analysis they found that the GDI is the area optimizing, high-speed and low-power option. They designed their ALU with the CMOS technology nodes at 180 nm and 130nm. [20].

In a research paper, the authors designed an Arithmetic Logic Unit (ALU) using the concept of Dual Mode Logic (DML). Their ALU comprises 4×1 multiplexer, AND gates, XOR gates, and a full adder circuit to implement various arithmetic and logic operations. Power and delay of ALU were calculated and compared with two other modes of ALU design, such as static and dynamic modes. The circuit was designed and simulated utilizing Mentor Graphics Pyxis Schematic Tool with 1.8 V DC and at 180 nm node. [21].

In an earlier published research paper, the authors presented a method for designing an 8-bit ALU using a 16:1 multiplexer in Verilog HDL. It was found that this circuit is more efficient, takes less power, occupies fewer surface-areas, and provides faster speed for the conventional ALU. Only 9 out of 16 inputs were utilized for the ALU tasks [22].

In another research article, the authors integrated binary Memristor Ratioed Logic (MRL) with the CMOS logic components to create structure of an ALU and then simulated the designed 1-bit ALU using LTSpice so that model parameters can be changed widely. After that, the analyses of an optimized 1-bit ALU was performed and it confirmed that the transistor counts were improved and delay was reduced [23].

The authors of a paper presented a design of a 4-bit ALU using the Gate Diffusion Input (GDI) technique and using the multiplexers and full adder circuits to have various logical and arithmetic operations. They used the Tanner EDA simulator by means of TSMC BSIM 250 nm node and compared with the prior designs implemented with the pass transistor and CMOS logic. The simulation results illustrate that the circuit consumes smaller power, occupies fewer surface area, and executes instructions very fast as compared to the other techniques [24].

Based on the research literature review, we decided to investigate the ALU operations by designing it using the Cadence simulation tool. For this purpose, we designed the basic transistor-level circuits at 90 nm CMOS technology node, such as AND, OR, XOR, and NOT gates as well as a 4:1 multiplexer. Then we created their symbols and combined those symbols to get the complete 1-bit ALU.

III. Theory and Design Methodology of the ALU

The digital circuit that can implement the micro-operations from the stored arithmetic and logical instructions and data in the sequential register circuit is called an Arithmetic Logic Unit (ALU). Such digital circuit gets some of the data from the external input devices and the other information from the sequential circuit-based registers. After that, they can perform some specific operations sequentially as given by the control circuit. A very simple design of such an ALU is depicted in Fig. 1 to elucidate this working principle. The control unit is designed using a combinational 4:1 multiplexer circuit that has 4 inputs, 2 select inputs, and 1 output. There are four logic operations as recorded in Table 1. These are logic AND, OR, XOR, and NOT operations. These logical tasks are materialized by utilizing the basic logic gates as depicted in Fig. 1.

Table 1. Truth Table for the logic operation of 1-bit ALU

S_2	S_1	Desired Logic Operation	Boolean Output Expression
0	0	AND	$F = AB$
0	1	OR	$F = A + B$
1	0	XOR	$F = A \oplus B$
1	1	NOT	$F = \bar{A}$

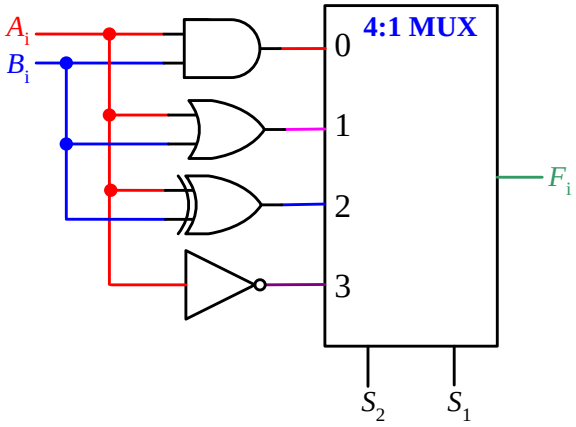


Figure 1. Block diagram representation of the one-stage logic circuit of the 1-bit ALU.

Then a 1-bit full adder was added at one of the inputs of the 4:1 multiplexer instead of the NOT gate to perform the addition operation as shown in Fig. 2. The addition operation is realized using the Full Adder (FA) symbol. A full adder digital circuit is well-defined as a combinational-type digital circuit that executes on the given 3 input bits, called *A*, *B*, and C_{in} and then produces the sum (*F*) and the carry outputs (C_{out}). The arithmetic and logic operations are shown in Table 2.

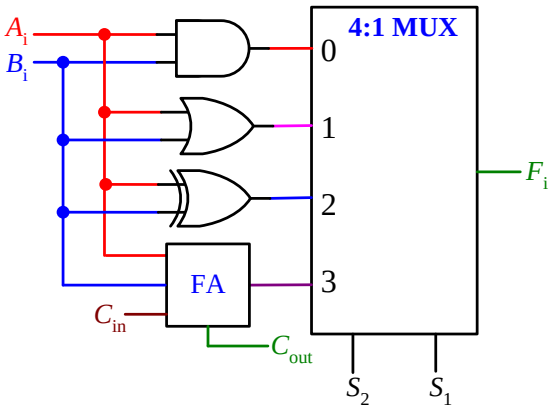


Figure 2. Block diagram representation of combining the logic and arithmetic circuits of the 1-bit ALU.

A digital multiplexer is also a kind of combinational-type circuit that can be built using the MOS devices. This circuit has several select bits and multiple input bits. The number of select bits are decided by the number of input bits of the multiplexer. If there are *n* number of input bits then the number of select input bits are $s = \lfloor log_{10}^{n} \rfloor$. Based on the select input signal combinations, the multiplexer circuit routes one of the n input signals to a single output channel. If the inputs of the multiplexer contain logical and full adder circuit output then it is possible to get a desired output choosing the appropriate control signals according to the signal combinations shown in Fig. 2 and Table 2.

Table 2. Truth table of the 1-bit ALU

Control Signals		Desired ALU Operation	Boolean Output Expression of the ALU Operation	Carry Output Expression after the ALU Operation
S_2	S_1			
0	0	AND	$F = AB$	X
0	1	OR	$F = A + B$	X
1	0	XOR	$F = A \oplus B$	X
1	1	SUM	$F = A \oplus B \oplus C_{in}$	$C_{out} = AB + BC_{in} + C_{in}A$

An Arithmetic Logic Unit, or ALU, is a combinational circuit that produces either logical or arithmetic operation results based on its control signals. In computers and other such types of digital hardware circuits, an ALU is like a heart. The arithmetic unit of the ALU performs different arithmetic operations (such as, addition, subtraction, multiplication, division, increment, decrement, etc.) and the logic maneuvers of the ALU perform

various logic operations, such as AND, OR, XOR, NOT, etc. The data for the arithmetic and logical operations are stored in various registers or memory devices. A 1-bit ALU circuit is portrayed in Fig. 2 that has 1-bit logical unit, 1-bit full adder unit, and a carry out bit. All of these sections are combined and a decision is to be taken by the controller on which operation to be executed. The design methodology used in Cadence is shown below:

1. The logical operations were designed in Cadence and those designed was represented as symbols for the schematic size issue. The design and the symbols are shown in Figs. 4-7.
2. Following the theory, all the symbols was organized and designed the ALU. One ALU is for only logical circuit and another one is designed with the logical and arithmetic circuit (full adder).
3. For the analysis, the inputs are *A*, *B*, C_{in}, and the selector pins are S_1 and S_2 were added to the circuit.

We used NMOS and PMOS transistors in the CMOS circuit from the gpdk090 library of the Cadence design tool. Table 2 presents the design parameters including the library and cell view names used for the common source amplifier circuit.

Table 3. Design parameters and isntance names used in the Cadence environment

Library Name	Cell View Name	Properties
Symbols (Customized)	AND, OR, XOR, FULL ADDER, 4:1MUX	Total Width = 1u/2u, Length = 90n
gpdk090	pmos1v	Total Width = 2u, Length = 90n
gpdk090	nmos1v	Total Width = 1u, Length = 90n
analogLib	vpulse (as the input signal)	voltage1 = 0V, voltage2 = 3.8V, minimum pulse period = 20n, minimum pulse width = 10n
analogLib	vdc	DC voltage = 3.8V
analogLib	vdd	
analogLib	vss	
analogLib	gnd	

The created symbols were used to design the final 1-bit ALU circuit. This makes the schematic diagram well organized and easy to analyze. The designed cell views for the ALU is shown in Fig. 3 where cell names are visible in the Symbols library.

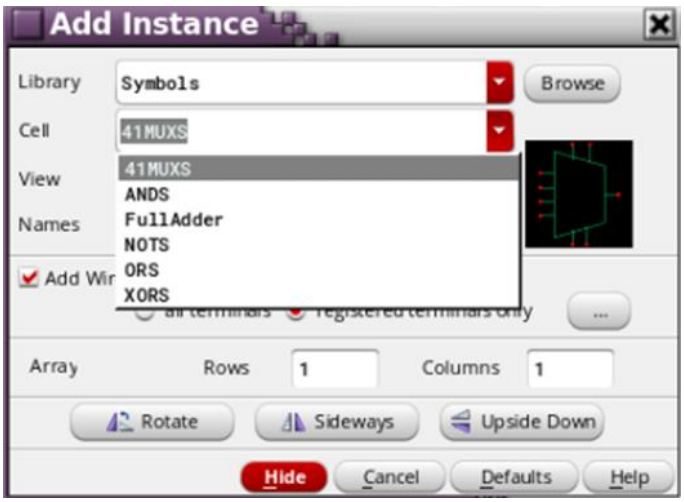
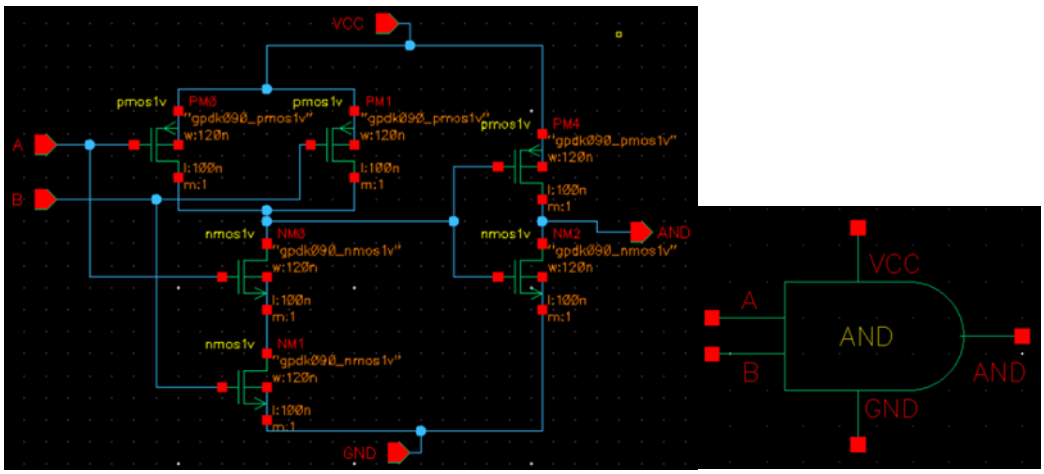


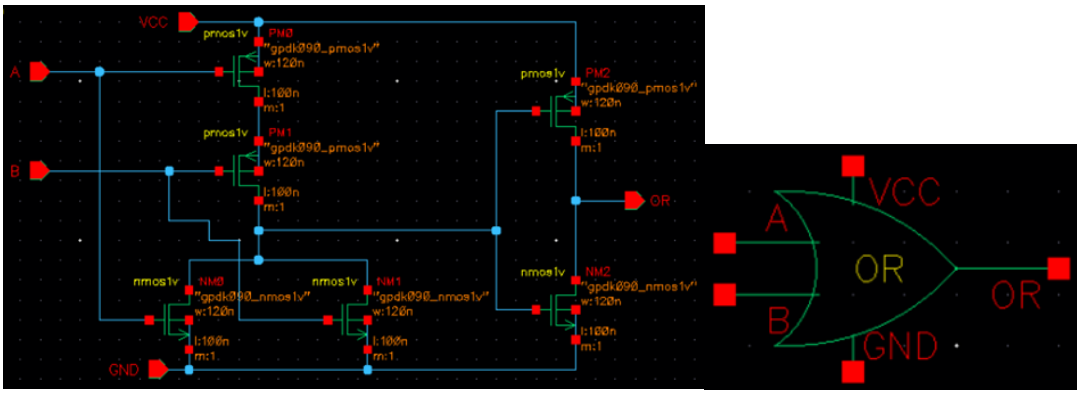
Figure 3. The instance names of the ALU circuit in the Symbols library

To design the ALU circuit with MOS transistors' length of 90 nm, we used the gpdk090 library and attached its technology file to our design library. After that, we opened the schematic window and inserted various components like transistors by creating various instances from various component libraries, pins, sources, ground, etc. from various libraries. We changed the parameter values and properties of them based on our design requirements shown in Table 2. Then we connected those using wires. A design methodology was employed in Cadence tool to develop a 1-bit Arithmetic Logic Unit (ALU). Customized symbols were designed to represent the logical operations of AND, OR, XOR, NOT, Full Adder, and 4:1 Multiplexer due to the schematic size issues. The designed schematic circuit diagrams and associate customized logic symbols are shown in Figs. 4-9.



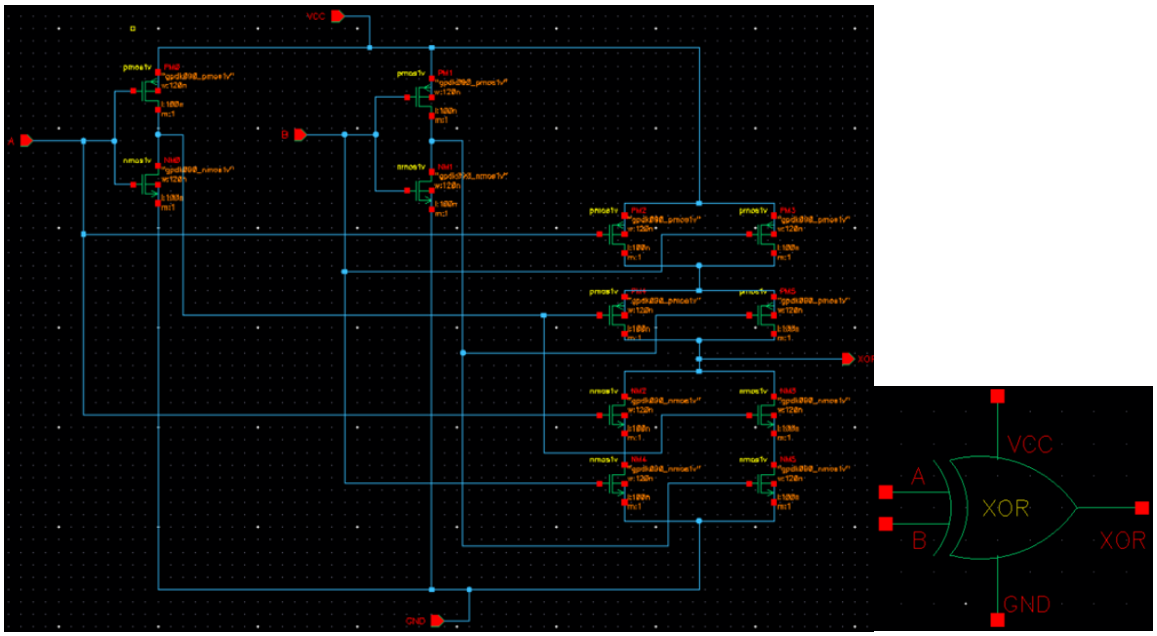
(a) (b)

Figure 4. (a) The schematic diagram of the logical AND operation circuit and (b) its customized logic symbol



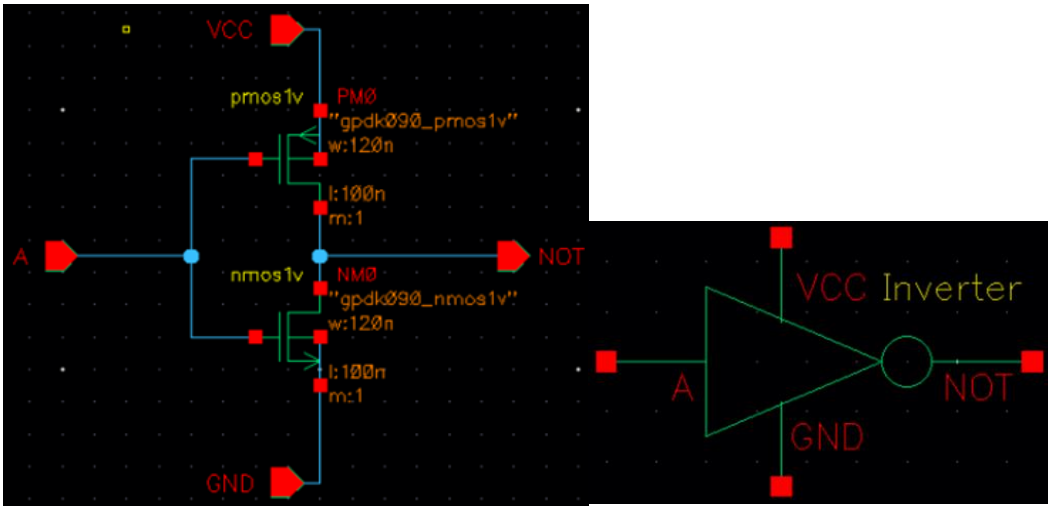
(a) (b)

Figure 5. (a) The schematic diagram of the logical OR operation circuit and (b) its customized logic symbol



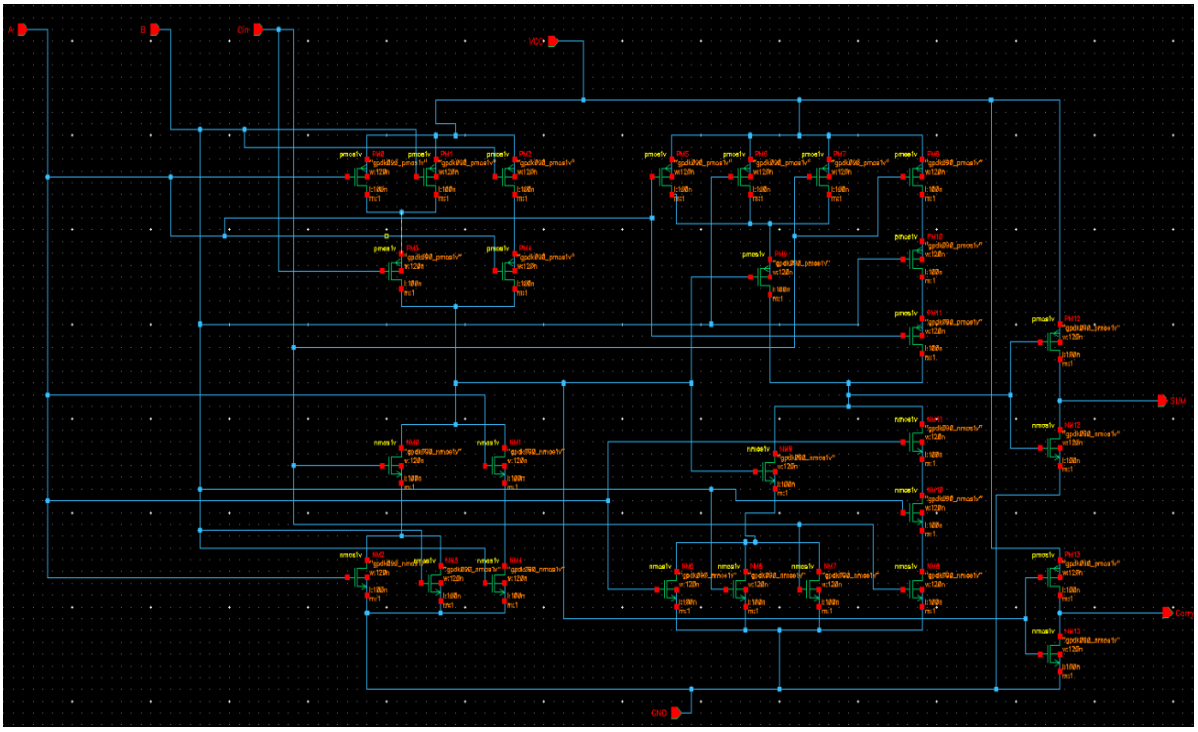
(a) (b)

Figure 6. (a) The schematic diagram of the logical XOR operation circuit and (b) its customized logic symbol

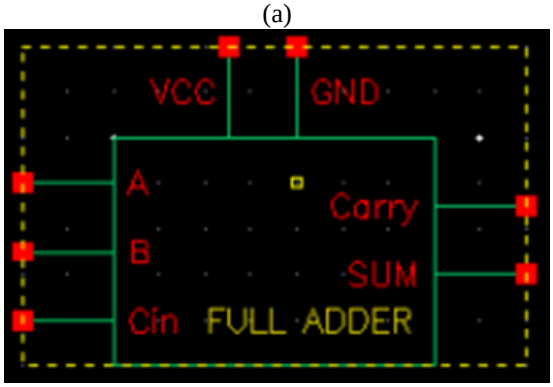


(a) (b)

Figure 7. (a) The schematic diagram of the logical NOT operation circuit and (b) its customized logic symbol

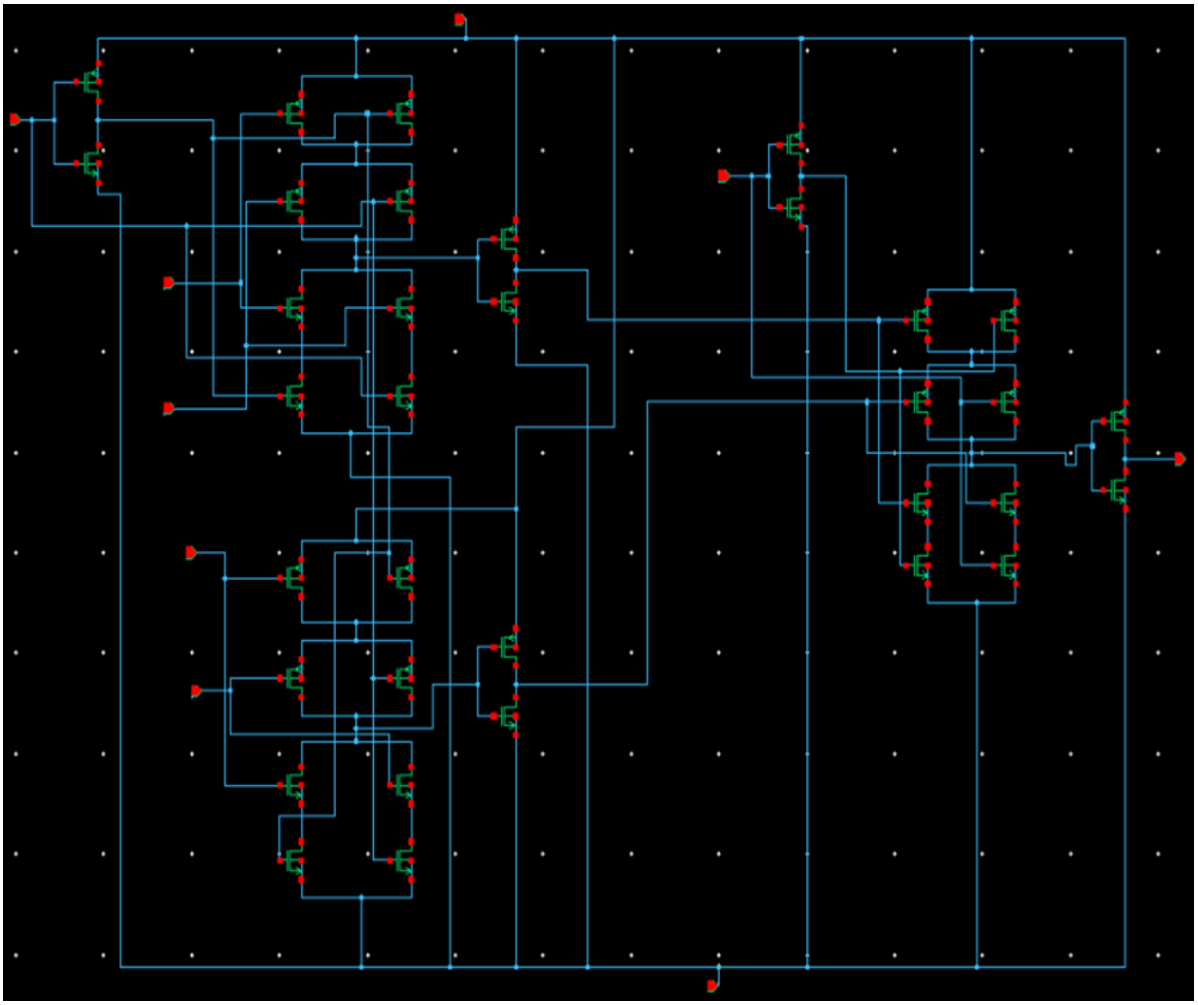


(a)

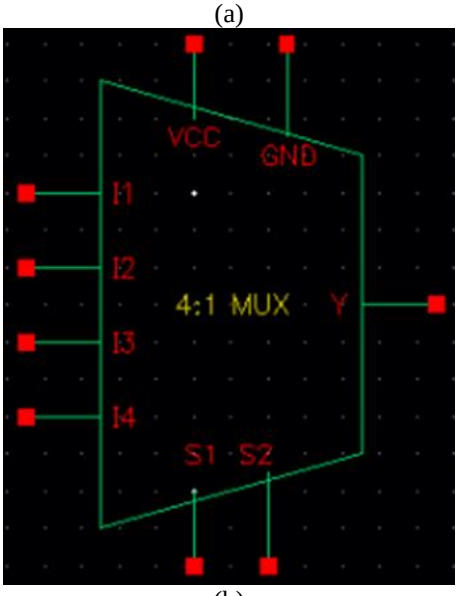


(b)

Figure 8. (a) The schematic diagram of the logical FA operation circuit and (b) its customized logic symbol



(a)



(b)

Figure 9. (a) The schematic diagram of the logical MUX operation circuit and (b) its customized logic symbol

The designed symbols were then organized and utilized to design two ALUs, one with logical circuits only and the other with both logical and arithmetic circuits. Input parameters, including *A*, *B*, C_{in}, and selector pins, S_1 and S_2, were incorporated into the circuit for proper operation of the designed circuit. The schematic diagram of the 1-bit ALU was well-organized and easy to analyze. The logical operations were designed using basic logic gates, while the arithmetic operations were carried out using full adder circuit. The 1-bit ALU is

capable of performing arithmetic and logical functions based on the inputs and the control signals received from the multiplexer, which then routed the appropriate signals at its output terminal.

The complete schematic circuit drawing of the one stage logical circuit is portrayed in Fig. 10. The VCC terminals of the symbols are connected to the Vdd source, the GND terminals of the symbols are connected to the ground, and the input pins of the symbols are connected to the Vpulse sources. The final schematic diagram of the one-bit ALU circuit using all symbols is shown in Fig. 11.

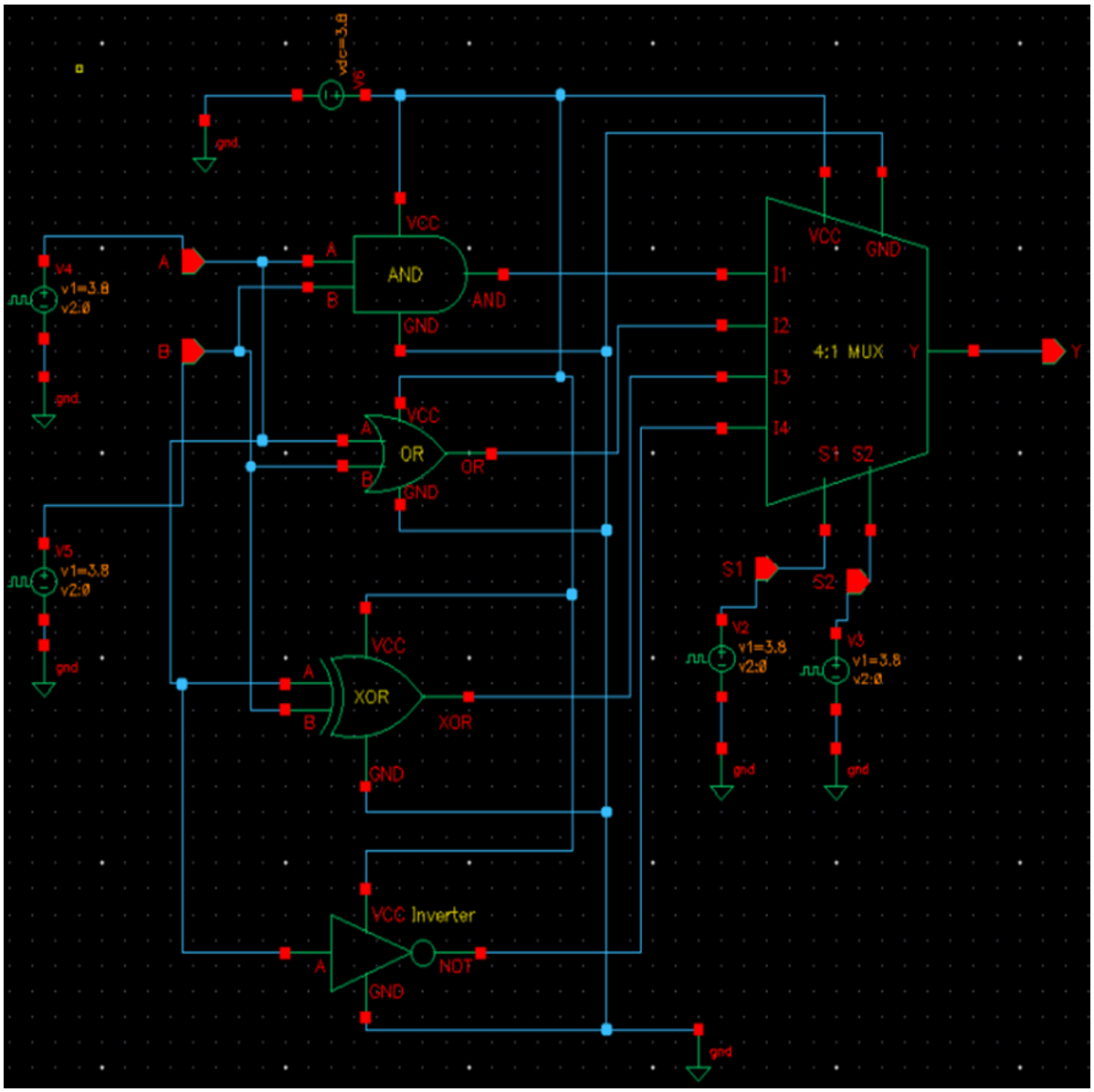


Figure 10. The schematic drawing of the one-stage logical circuit

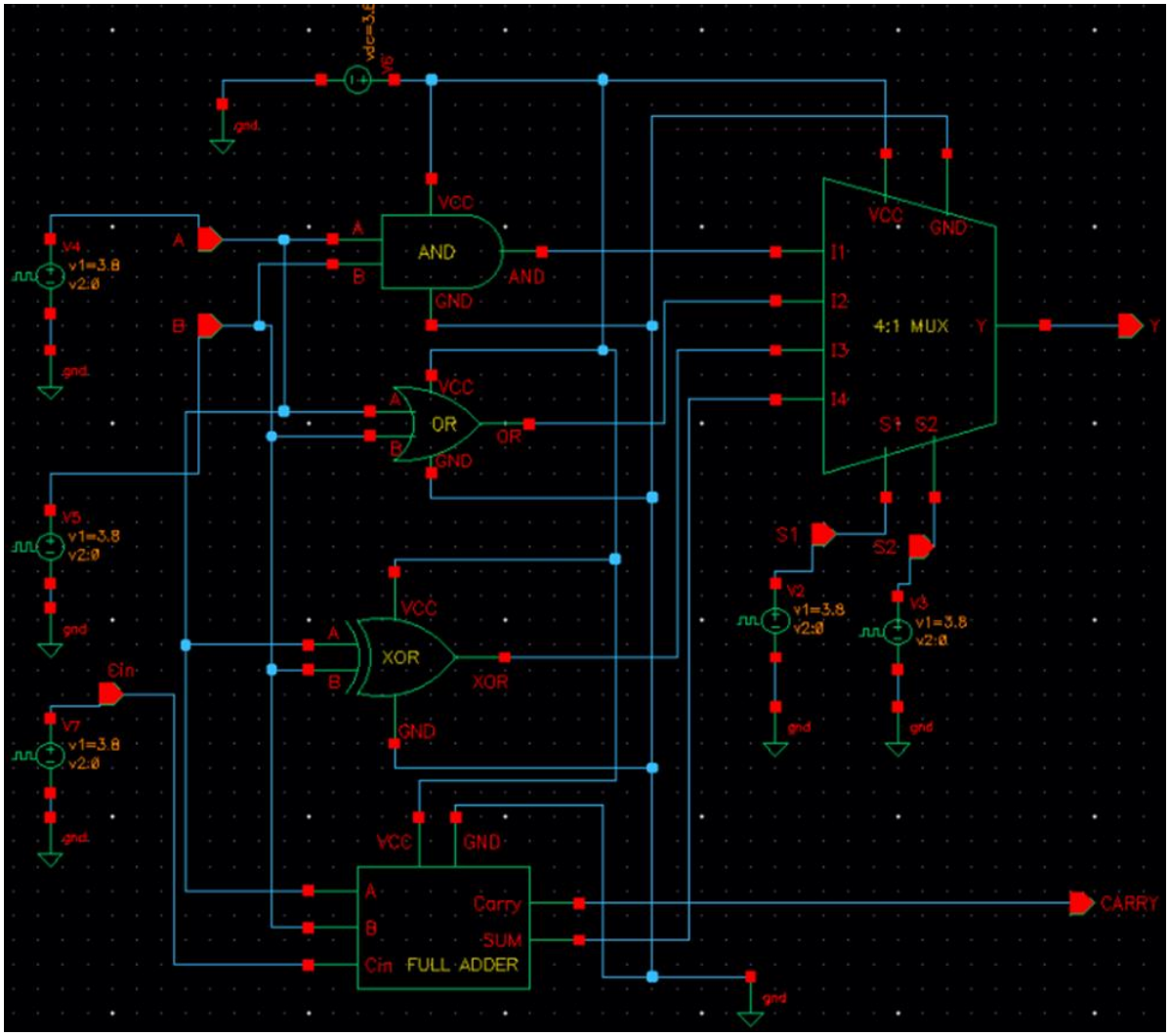


Figure 11. The schematic drawing of the one-bit ALU circuit using all symbols

IV. Results and Discussions

To simulate the designed 1-bit ALU circuit, we used Analog Design Environment (ADE) of Cadence tool. We accomplished our analysis for a duration of maximum 320 ns time to get the outputs through the transient analysis for different input signal combinations with typical process parameters. The transient simulation results are shown in Figs. 12-13. The simulation results were analyzed to verify the functionality of the designed ALU and to evaluate its performance. The simulation parameters that were used in this work are shown in Table 4.

Table 4. Simulation parameters and isntance names used in the Cadence environment

Library Name	**Cell View Name**	**Properties**						
			Logic Circuit			**Combined Circuit**		
			Input	Period	Pulse	Input	Period	Pulse
analogLib	vpulse (as the input signal)	voltage1 = 0V, voltage2 = 3.8V, minimum pulse period = 20n, minimum pulse width = 10n	S_2	160n	80n	S_2	320n	160n
			S_1	80n	40n	S_1	160n	80n
			A	40n	20n	A	80n	40n
			B	20n	10n	B	40n	20n
						C_{in}	20n	10n
analogLib	vdc	DC voltage = 3.8V						
analogLib	gnd	DC voltage = 0V						

After that, various types of simulations were performed, such as transient and DC analysis, parametric sweep, power and delay computation, etc. Figure 12 shows the functional simulation output for the 1-bit ALU's

logical portion is obtained by the transient analysis. The simulation results show that when the multiplexer's select inputs (S_2 and S_1) is 00 then we get the AND operation, that is when both inputs (A and B) to the ALU is 11, the output signal (Y) is HIGH otherwise it is LOW. When the multiplexer's select inputs (S_2 and S_1) is 01 then we get the OR operation, that is when both inputs (A and B) to the ALU is 00, the output signal (Y) is LOW otherwise it is HIGH. When the multiplexer's select inputs (S_2 and S_1) is 10 then we get the XOR operation that is when both inputs (A and B) to the ALU is either 00 or 11, the output signal (Y) is LOW otherwise it is HIGH. Finally, when the multiplexer's select inputs (S_2 and S_1) is 11 then we get the NOT operation, that is when a single input (A) to the ALU is 0, the output signal (Y) is HIGH otherwise it is LOW.

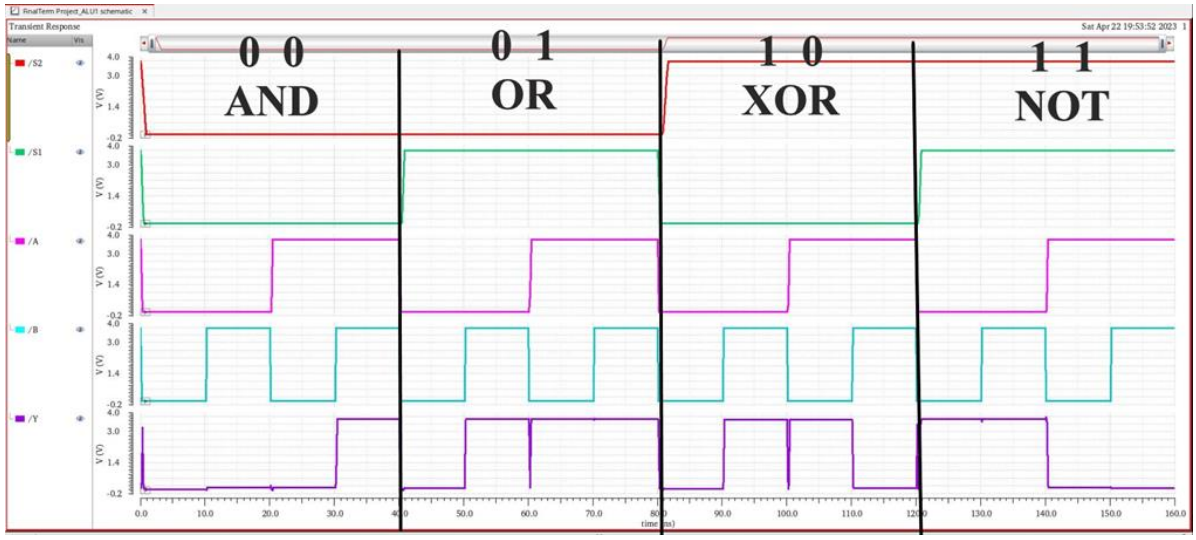


Figure 12. Simulated output voltage for applied input signals obtained by the transient response analysis of the logical part of the 1-bit ALU

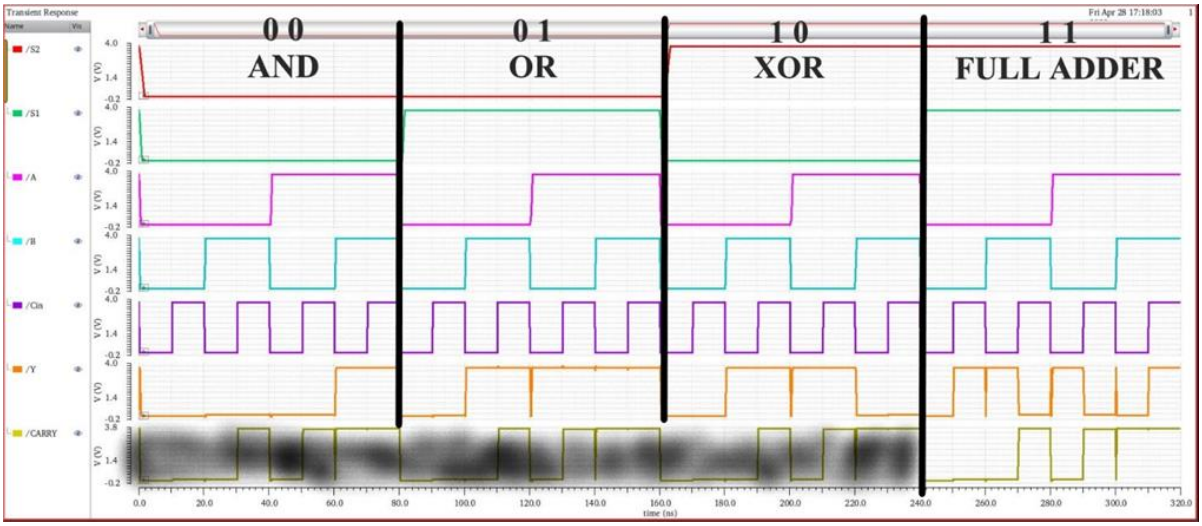


Figure 13. Simulated output voltage for applied input signals obtained by the transient response analysis of both logical (outputs are blurred) and arithmatic part of the 1-bit ALU

The analysis of the circuit was carried out using a timing diagram or transient analysis. Both the one-stage logical circuit and the combined logical and arithmetic circuit were analyzed for a duration of 160ns and 320ns, respectively. The analysis results indicate that the circuit is performing well. However, it was observed that the carry output is showing even in other operations, which may be attributed to the combined analysis of all possible input combinations.

The DC analysis was conducted to ensure that the circuit functions properly in steady-state conditions. DC analysis was performed for both the one-stage logical circuit and the combined logical and arithmetic circuit for one of the input signals (here it is B) from 0 V to +3.8 V keeping other signals constant DC signals at 3.8 V. Then the circuit's response was analyzed. For both circuits, the input and output voltages were analyzed, and the voltage levels were found to be within the acceptable range. The DC analysis confirmed that the circuits were

functioning correctly in steady-state conditions. Since the voltage is applied to the NMOS transistor's input, the output voltage goes to approximately 100 mV (LOW) when the input voltage becomes 3.8 V (HIGH). The voltage is not exactly zero voltage when the input is completely turned ON due to the saturation resistance of the transistor.

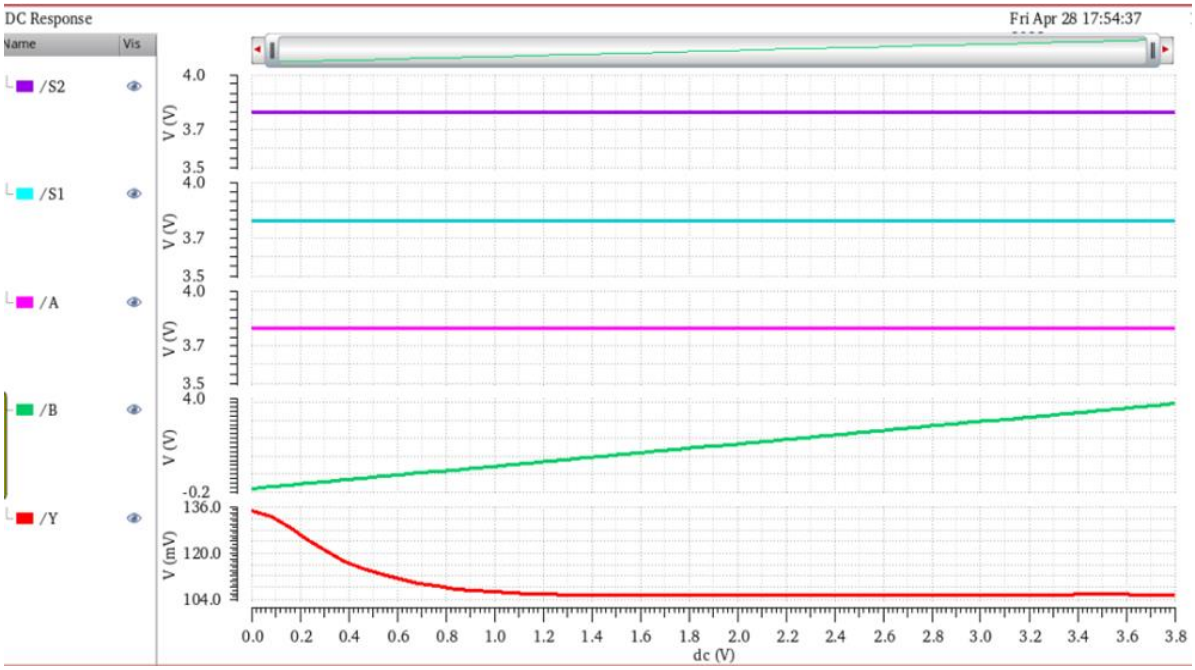


Figure 14. Simulation result of the DC analysis of 1-bit ALU (only logical part)

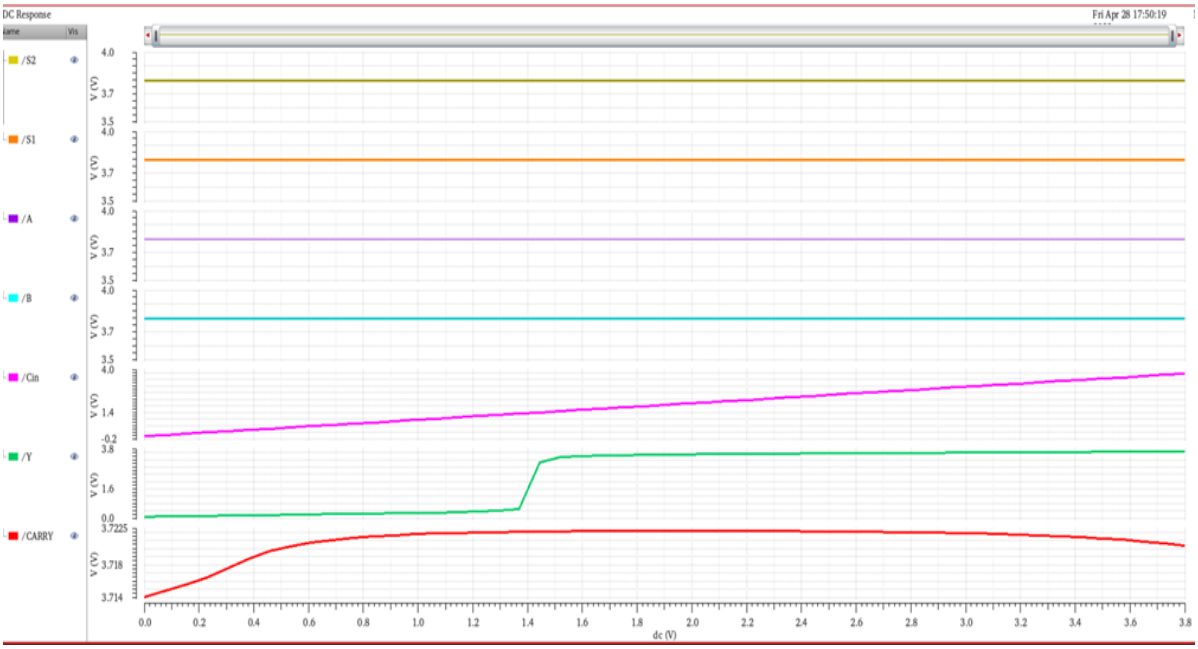


Figure 15. Simulation result of the DC analysis of 1-bit ALU (only arithmatic part)

A parametric analysis, also known as a sweep analysis, was conducted to determine the effect of varying the VCC voltage on the DC response of the designed circuits for its sum (Y) and carry (C_{out}) outputs. The VCC voltage was changed from 1 V to 5 V and the DC response was analyzed. The results of the parametric analysis showed that the circuits were operating as expected within the tested voltage range.

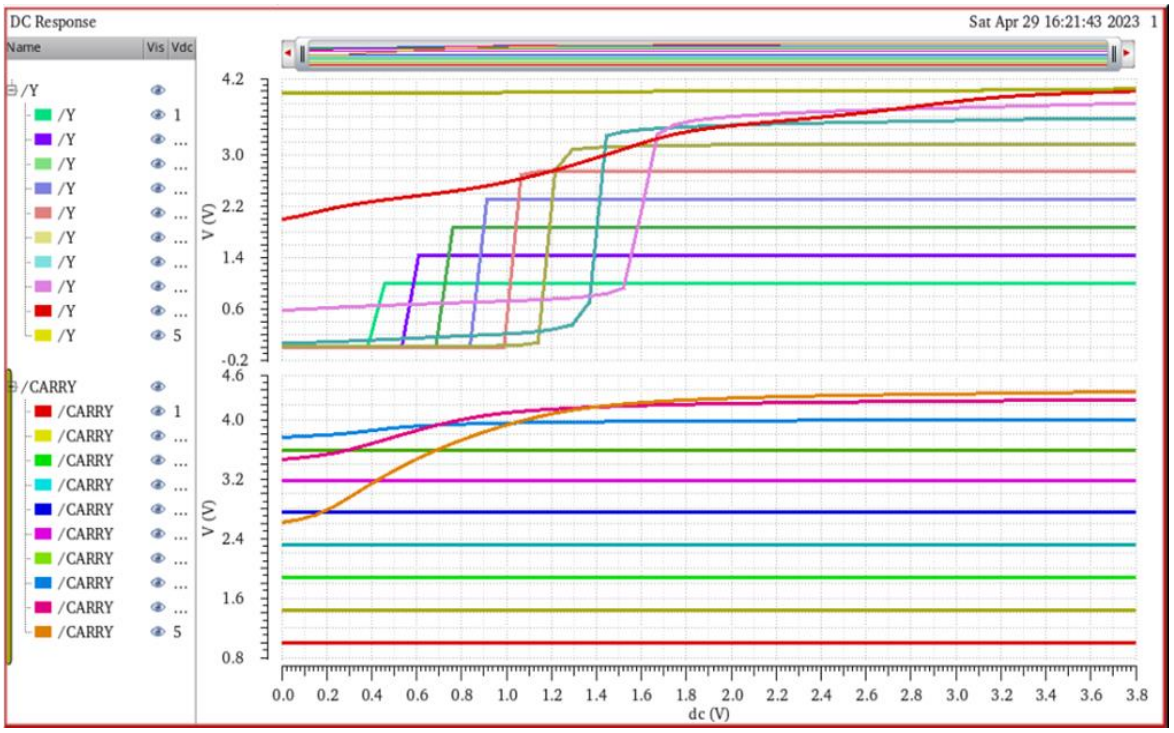
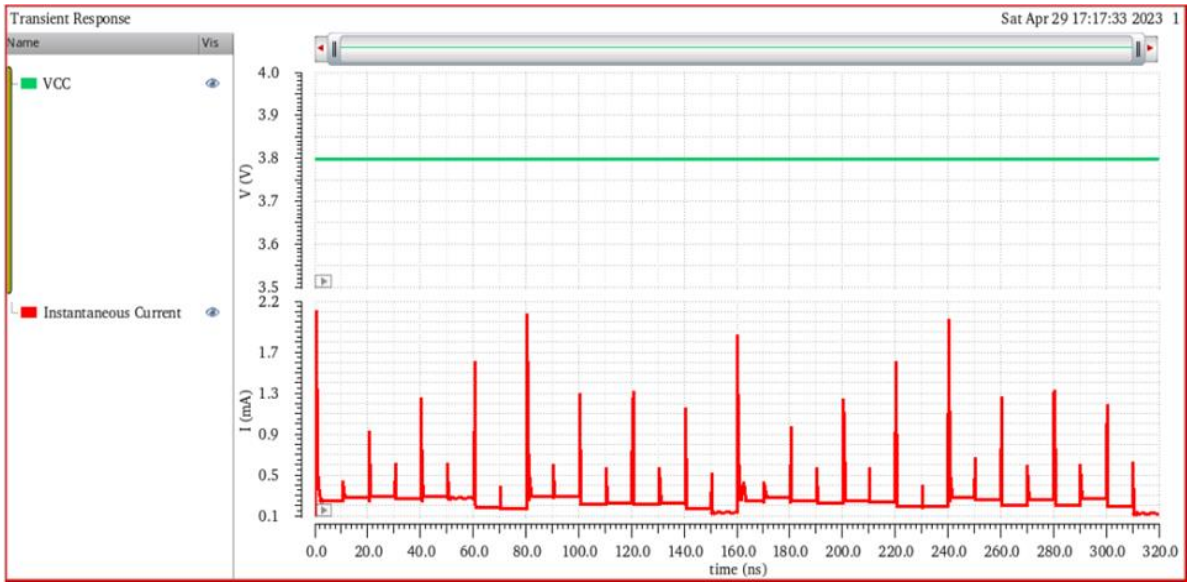
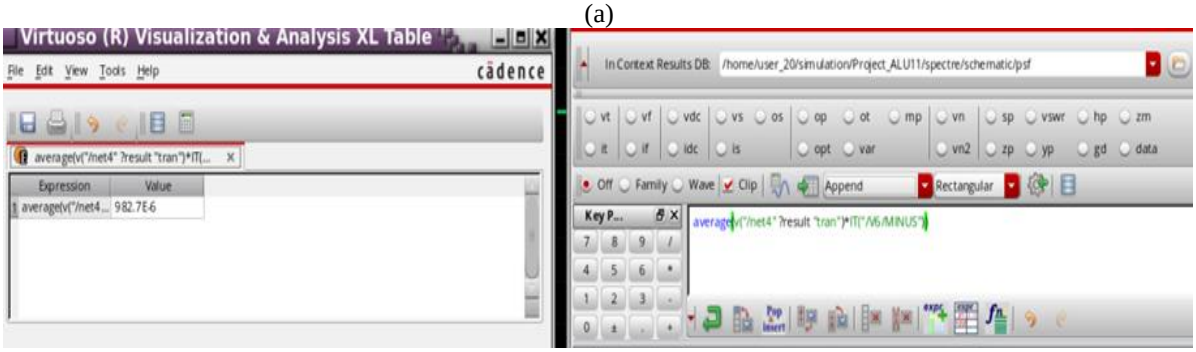


Figure 16. Simulation result of the parametric analysis of 1-bit ALU (only arithmatic part)



(a)



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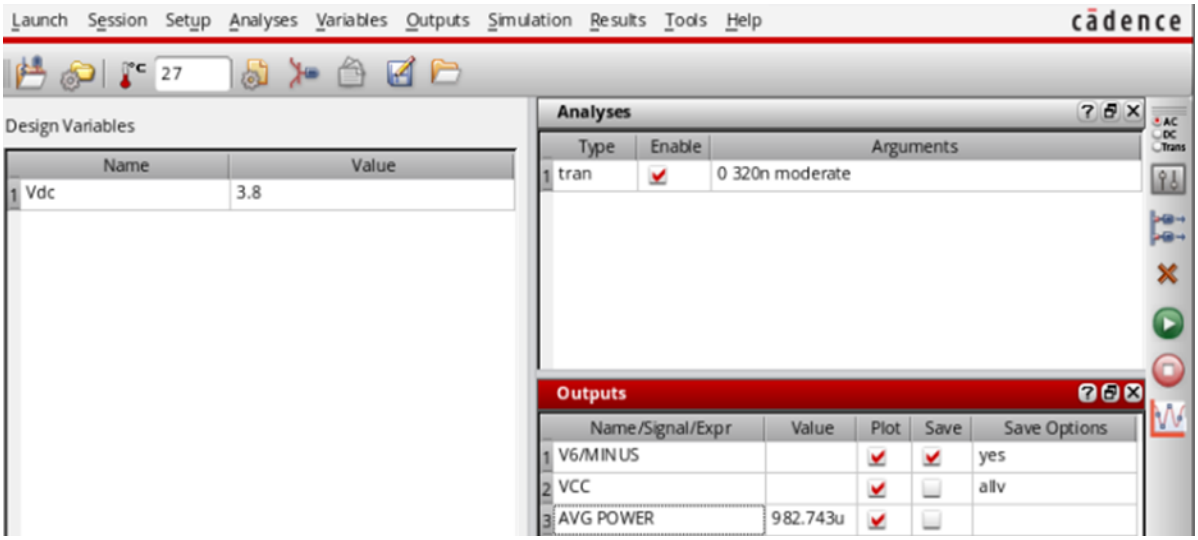

(c)

Figure 17. Simulation result of the power consumption analysis of 1-bit ALU (only arithmatic part)

The average power consumption of the designed 1-bit ALU circuit was calculated using the ADE of the Cadence tool. The simulation was run for a specific period of time, and the power was calculated by integrating the product of voltage and current over time. The simulation results showed that the average power consumption of the combined logical and arithmetic circuit was 982.743 □W. This information is useful for estimating the power requirements of the circuit and optimizing its performance.

Delay measurement was performed to evaluate the propagation time of signals through the circuits. The delay was calculated by analyzing the time variance between the input and the output signal. The measurement results showed that the circuits had almost no delay, indicating a fast signal propagation through the circuit. This suggests that the circuit can process the input signals with minimal latency, which is desired for many applications.

V. Conclusions and Future Directions

The research-based design and analysis work is aimed to plan and inspect a 1-bit Arithmetic Logic Unit (ALU) using Cadence Virtuoso design and simulation software at a 90 nm technology node. Customized symbols for logical operations were created and used to produce the schematic diagram for the ALU. Two circuits were designed, one with only logical operations and another with both logical and arithmetic operations. The circuits were analyzed using transient, DC, and parametric analysis. The results showed that the circuits were performing well with almost no delay and low power consumption. However, during the analysis, it was found that the carry output was showing even in other operations, which may be due to the combined analysis of all operations together. Further investigation is required to determine if this is a real-world issue or a limitation of the analysis.

In conclusion, the research work successfully designed and analyzed a 1-bit ALU using Cadence design software. The results showed that the circuits were performing well with low power consumption and no significant delay. Further improvements can be made by investigating the issue with the carry output and optimizing the design for specific applications. Overall, the circuit demonstrates the importance of proper design and analysis techniques in the development of electronic circuits.

In the forthcoming days, additional investigations will be performed for the same designed circuit using the state-of-the-art CMOS technology node and for the multi-bit ALU circuits. Besides, a comparative analysis of the same ALU may be prepared for diverse CMOS technology nodes. Describing the design and simulation methods may give novice designers many important insights of this advanced professional VLSI circuit design tool and this also assists the teachers to prepare valuable teaching and learning materials for the VLSI Circuit Design laboratory course works.

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