Design of Current-Mode Pulsed Flip-Flop with Enable for Low power Clock Distribution

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Abstract: *In this paper, we propose a new paradigm for clock distribution that uses current, rather than voltage, to distribute a global clock signal with reduced power consumption. The Current-mode (CM) signaling can be used for one-to-many clock distribution network. To accomplish this, we create a new high-performance current-mode pulsed flip-flop with enable (CMPFFE) using Tanner tool in 180nm CMOS technology. When the CMPFFE is combined with a CM transmitter, the first CM clock distribution network exhibits 32% lower average power compared to traditional voltage mode (VM) clocks. CM clocking can play an important role in low-power systems. CM signaling offers many potential advantages such as higher operating speed, low voltage operation, ease of processing and reduced power consumption compared to voltage-mode (VM) techniques.*

Index Terms: *Current-mode, Voltage-mode, Clock distribution network, flip-flop, low-power.*

I.   Introduction

Low-power design has become quite critical in synchronous application specific integrated circuits (ASICs) and system-on-chips (SOCs) because interconnect in scaled technologies is consuming an increasingly significant amount of power. Portable electronic devices require long battery lifetimes which can only be obtained by utilizing low-power components. Flip-flops (FFs) are the basic storage elements and are used extensively in designs of all digital systems. Today's technology adopts the pipelined architecture in each and every system to improve its performance. Clock system consists of a clock generator, clock distribution network (CDN) and number of flip-flops. Clock distribution networks synchronize the flow of data signals among synchronous data paths. The design of these networks can dramatically affect system-wide performance and reliability. Researchers have demonstrated that the major consumers of this power are global buses, clock distribution networks (CDNs), and synchronous signals in general [1]. The CDN in the POWER4 microprocessor, for example, dissipates 70% of total chip power [2].

In addition to power, interconnect delay poses a major obstacle to high-frequency operation. Technology scaling reduces transistor and local interconnect delay while increasing global interconnect delay [3], [4]. Moreover, conventional CDN structures are becoming increasingly difficult for multi-GHz ICs because skew, jitter, and variability are often proportional to large latencies. Low-swing and current-mode signaling, however, are highly attractive solutions to help address the interconnect power and variability problems. Traditionally, the static power dominates dynamic power consumption in a CM signaling scheme [5]. However, the static power is often significantly less than VM dynamic power and latency is significantly improved over VM in global CM interconnect. CM signaling schemes also offer higher reliability since they are less susceptible to single-event transient upsets due to the absence of buffers with source/drain diffusion areas that can be hit by high-energy particles.

In this paper, we present a new CM pulsed D-type FF with enable (CMPFFE) where the clock (CLK) input is a CM, receiver and the data input (D), an active low enable (EN), and output (Q) are VM.

II.   Existing Flip-Flops In Voltage-Mode (Vm)

A. Low-Power Pulse-Triggered Flip-Flop Design with Conditional Pulse Enhancement Scheme (CPEFF) [6]:

A low-power pulse-triggered flip-flop (FF) design is presented. A simple two-transistor AND gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. The fig. 1 shows the circuit diagram of CPEFF.
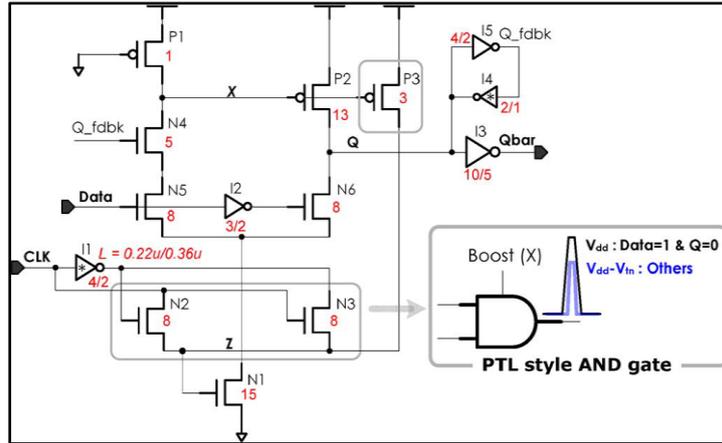
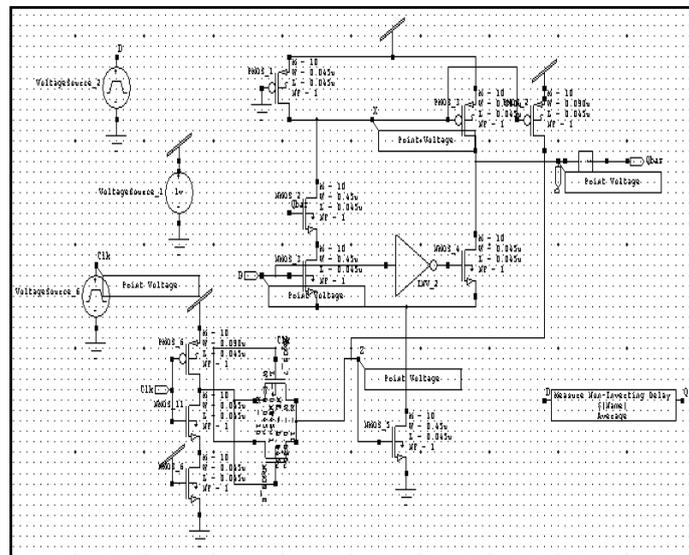**Fig 1**: Circuit diagram of CPEFF

Fig 2: Schematic diagram of CPEFF

The design supports a mechanism to conditionally enhance the pull down strength when input data is "1." Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at "0" most of the time. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. The parallel conduction of two NMOS transistors (N2 and N3) speeds up the operations of pulse generation. In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normally turned off because node X is pulled high most of the time. This provides additional boost to node Z. The generated pulse is taller, which enhances the pull-down strength of transistor N1.

B. Low-Power Dual Dynamic Node Pulsed Hybrid Flip-Flop (DDFF) [7]:

In Dual Dynamic Node Hybrid Flip-Flop (DDFF), there are two nodes in the circuit among which one is purely dynamic and another is pseudo-dynamic. So, it is called as dual dynamic. It is hybrid in nature as it is having dynamic front end and static output, this flip-flop is named as DDFF. The dual dynamic node hybrid flip-flop (DDFF) eliminates the large capacitance present in the precharge node by following a split dynamic node structure to separately drive the output pull-up and pull-down transistors.

Fig.3 shows DDFF architecture. Node *X*1 is pseudo-dynamic, with a weak inverter acting as a keeper and node *X*2 is purely dynamic. The operation of the flip-flop can be divided into two phases:
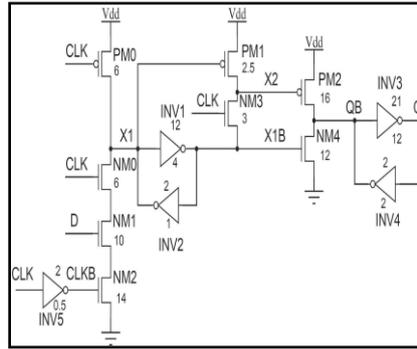1) evaluation phase, when CLK is high, and
2) precharge phase, when CLK is low
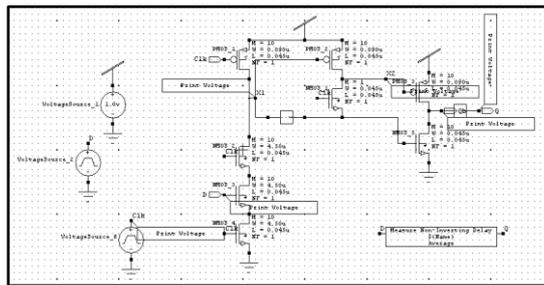
Fig 3: Circuit diagram of DDFF

Fig 4: Schematic diagram of DDFF

The actual latching occurs during the 1–1 overlap of CLK and CLKB during the evaluation phase. If *D* is high prior to this overlap period, node *X*1 is discharged through NM0-2. This switches the state of the cross coupled inverter pair INV1-2 causing node *X*1*B* to go high and output *QB* to discharge through *NM*4. The low level at the node *X*1 is retained by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, node *X*2 is held high throughout the evaluation period by the PMOS transistor *PM*1.

As the CLK falls low, the circuit enters the precharge phase and node *X*1 is pulled high through *PM*0, switching the state of INV1-2. During this period node *X*2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node *QB* and maintain their voltage levels through INV3-4.

III.   Current-Mode Pulsed Flip-Flop With Enable (Cmpffe)

A current-mode pulsed D-type FF with enable (CMPFFE) [8] is proposed where the clock (CLK) input is a CM, receiver and the data input (D), an active low enable (EN), and output (Q) are VM. The figure 5 shows the circuit of the proposed current-mode pulsed DFF with enable (CMPFFE). The CMPFFE uses an input current-comparator (CC) stage, a register stage, and a storage cell. The CC stage compares the input push-pull current with a reference current and conditionally amplifies the clock to a full-swing voltage pulse that triggers the data to latch at the register stage.
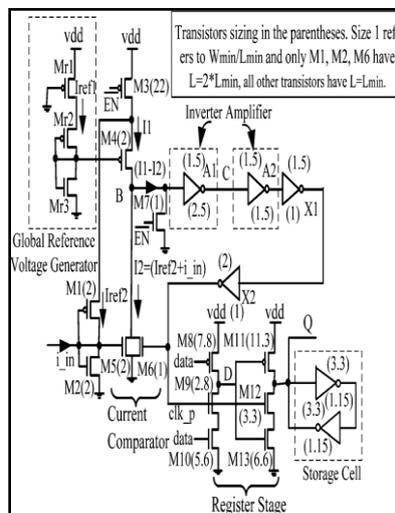

Fig 5: Circuit diagram of CMPFFE

CM Rx/logic circuits consume a significant amount of static power even when the circuits are in sleep mode. The CMPFFE incorporates an active-low enable (EN) signal that, when low, connects PMOS (M4) to Vdd for normal operation. On the other hand, it disables the static current I1 in stand-by mode when high. Since internal node B is decoupled in this stand-by mode, an additional transistor M7 is required to ground the internal clock node and prevent any unintentional latching of input data. Transistor M7 is disabled during normal operation.

In the input stage, the reference voltage generator (Mr2–Mr3) creates a reference current (Iref1) that is mirrored by M4 and generates I1. Similarly, the M1–M2 pair creates the FF reference current (Iref2) which is combined with the input current (i_in); this current is then mirrored by M5 to I2. A PMOS (Mr1) is added to replicate the voltage drop of M3. The input current (i_in) is obtained from the current-mode transmitter and passed into the flip-flop circuitry. The proposed CM transmitter converts an VM input signal to a push-pull current with minimal interconnect voltage swing and transmits the current to the CMPFFE circuit. The current transmitter uses a NAND-NOR design. The NAND gate uses the CLK signal and a delayed inverted CLK signal, Clkb, as inputs to generate a small negative pulse to briefly turn on M1. Similarly, the NOR gate utilizes the negative edge of the CLK and Clkb signals to briefly turn on M2. The non-overlapping input signals from the NAND-NOR gates remove any short circuit current from transmitter.
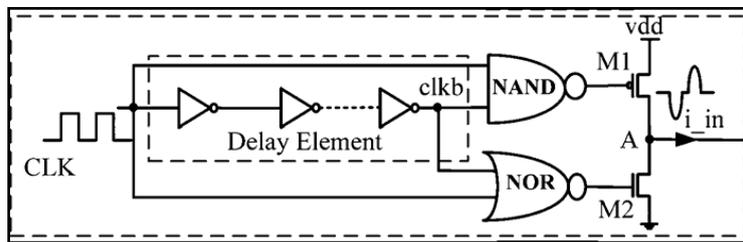

Fig 6: Circuit diagram of Current-mode Transmitter

The mirrored currents I1 and I2 are compared using the inverting amplifier (A1) at node B and further extended to a CMOS logic level at node C by another inverting amplifier (A2). The inverter pair (X1–X2) generate the required voltage pulse duration before the feedback connection in M6. The feedback connection from the generated voltage pulse with M6 quickly pulls down the current comparator node B which facilitates generating a small voltage pulse and results in fewer transistors in the register stage. The X2 inverter efficiently drives the clock capacitance of register stage without affecting circuit performance. The following figure 7 shows the schematic diagram of CMPFFE.
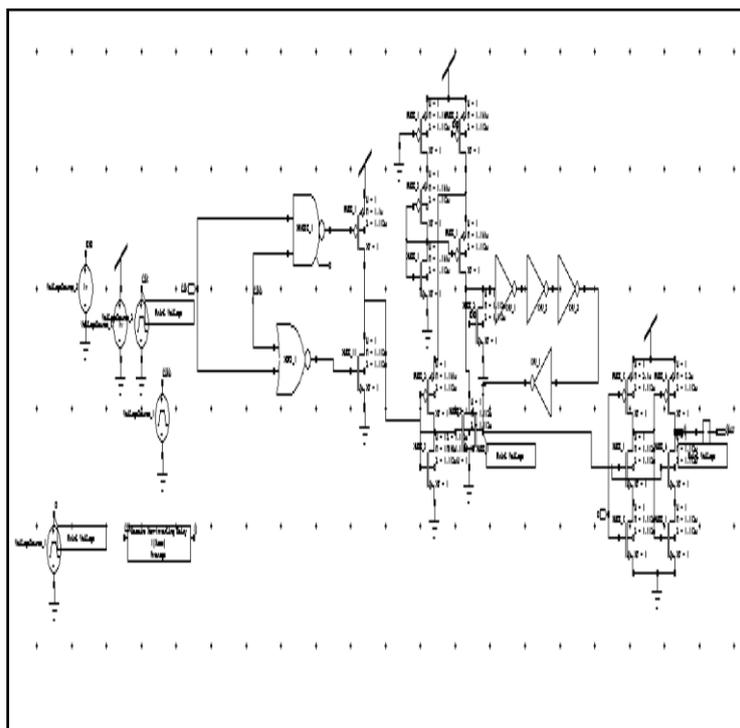

Fig 7: Schematic diagram of CMPFFE

IV.   Simulation Results

The simulations are carried out using Tanner tool in 180nm CMOS technology and the supply voltage is 1V. Based on post layout SPICE simulations, the performances of existing VM flipflops and proposed CM pulsed flipflop are evaluated. The following figures 8, 9, 10 and 11 show the simulation waveforms of the above flipflops.
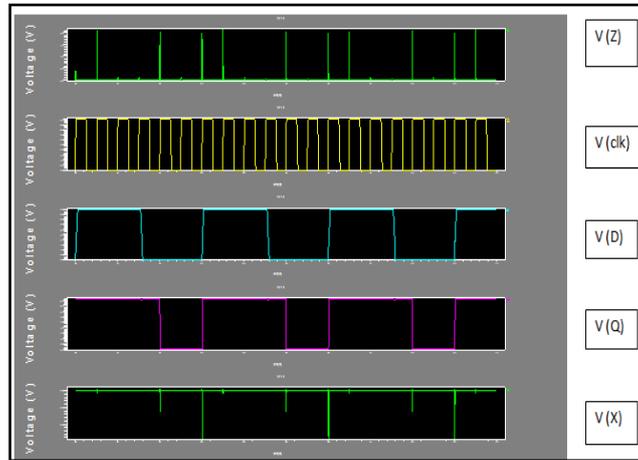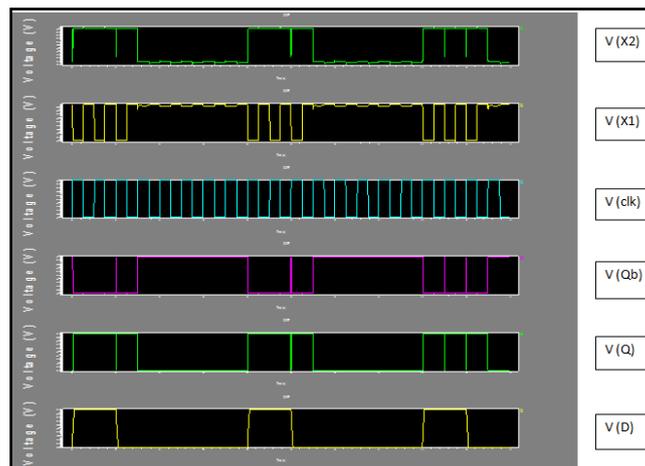
Fig 8: Simulation waveform of CPEFF
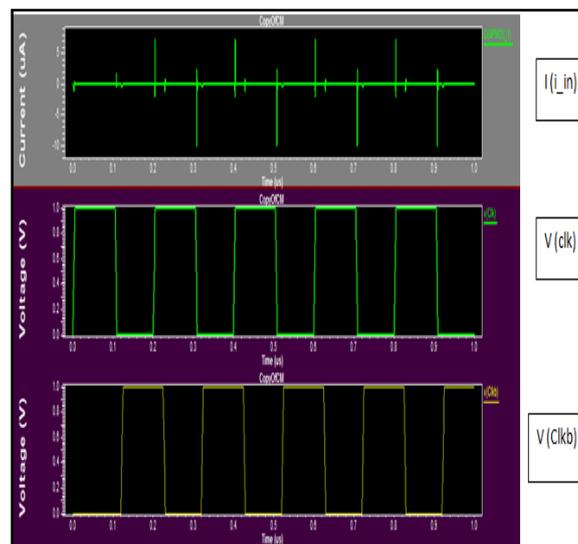
Fig 9: Simulation waveform of DDFF

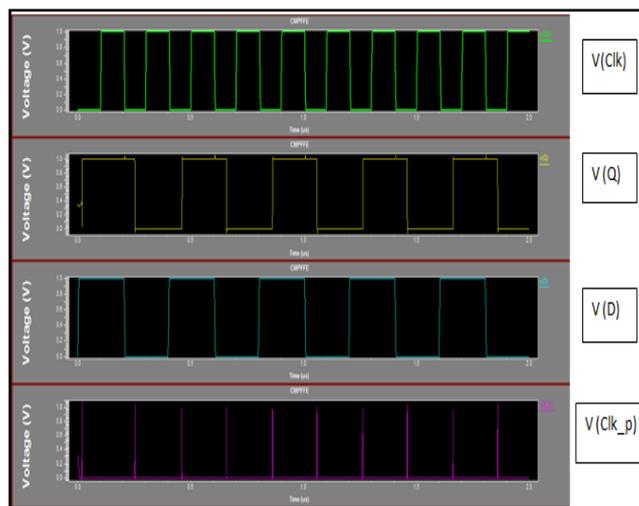**Fig 10:** Simulation waveform of Current-mode transmitter

Fig 11: Simulation waveform of proposed CMPFFE

Using T-SPICE simulations, the performance parameters are obtained using .power command between Vdd and Gnd. The Table-I shows the comparison of existing VM flip-flops and proposed CM flip-flop in terms of no. of transistors, delay and average power consumption.

Table-I

Flip-flop design	No. of Transistors	Delay(ns)	Average power consumption(mW)
CPEFF	18	68.1 ns	0.54 mW
DDFF	16	92.02 ns	0.40 mW
CMPFFE	25	19.02 ns	0.17mW

V. Conclusions

The Pulsed D-flipflop in Current-mode is presented. The proposed CMPFFE is 36% faster and requires less power. The CMPFFE enables a 32% reduction in power consumption compared to conventional VM flip-flops. The CMPFFE also eliminates the need for complex CM Rx circuitry and/or local VM buffers to drive highly capacitive clock sinks as in existing flipflop designs.

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