IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 11, Issue 3, Ser. I (May. - June. 2021), PP 01-17
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design and Performance Analysis of Low Voltage and Low Power Schmitt Trigger for 0.18 µm CMOS Process

Nahid A Jahan[1], Mohammad Fairuz Bin Amir[2], Md. Ashraful Islam[1], M Mofazzal Hossain[3*], Mamun Bin Ibne Reaz[2]

[1]*Department of Electrical and Electronic Engineering, Southeast University, Dhaka, 1208, Bangladesh*
[2]*Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia, Bangi, Selangor, Malaysia*
[3]*Department of Electrical and Electronic Engineering, University of Liberal Arts Bangladesh, Dhaka, 1209, Bangladesh*

Abstract:
This work presents the functionality of some unique Schmitt trigger circuits designed on the basis of the impact of load capacitance and supply voltages together with hysteresis width, propagation delay and average power dissipation. All the simulation results are performed for 0.18 µm CMOS process technology. It is found that through the recommended design a larger hysteresis width can be attained by modifying the arrangement and organization of transistors as well as the ratio of width to length of channel. The results of our analysis reveal that the designed Schmitt trigger can be driven using low voltage of 0.8-1.5 V and the power dissipation is reduced to only 47.24 pW. The total active area of our suggested trigger circuit is 10.80 × 10.65 µm^2. The proposed Schmitt trigger will be suitable and useful where large hysteresis width is required to improve the noise margin. Therefore, it may be propounded that our designed Schmitt trigger have low power dissipation, large hysteresis width and plausibly be operated with lower voltage compared to earlier designs found in literature.

Key Words*: Schmitt trigger; Hysteresis width; Power dissipation; Propagation delay.*

Date of Submission: 14-06-2021 Date of Acceptance: 28-06-2021

I. Introduction

The CMOS Schmitt triggers are one of the pertinent components of various emerging applications in the field of electronic devices. They serve as solid state comparators those are extensively employed to raise the noise immunity of circuit and unwanted perturbations. In general, it works as an inverter which consists of two PMOS transistors, two NMOS transistors, one feedback PMOS transistor and one feedback NMOS transistor[1]. It accepts slow-changing signals and produces an output that has oscillation-free transitions. The output is high when the input is below the negative threshold voltage, while the output is low if the input exceeds the positive threshold voltage[2]. The value of the two threshold voltages can be varied and regulated by calibrating the performances and dimensions of the transistors (PMOS and NMOS). Fig.1 shows a typical Schmitt trigger circuit. The performance and uniqueness of Schmitt trigger circuits can be best evaluated through their propagation delay, hysteresis width and average power dissipation. The reduction of propagation delay is one of the crucial challenges for the realization of an intricate Schmitt trigger. It is defined as the delay time from input source to output source[4] and is symbolically depicted by the term, $t_p = 0.69RC_L = (t_{PHL}+t_{PLH})/2$.

Hysteresis is another important parameter which helps eliminating the noise and thus produces fairer and reliable signal. The hysteresis voltage-width is defined as the voltage difference between the switching threshold voltages V_{IH} and V_{IL} at output[5]. The stable output logic level is retained by eliminating this voltage from the V_{IL} or adding with the V_{IH}[6]. Larger the width of hysteresis better the improvement in noise margin can be achieved. On this regard, we can see that Kumar et al.[6] used two layers of feedback devices to increase the hysteresis width, while Sapawi et al[7] achieved a large hysteresis width by proposing a circuit using NAND gate.
In line with these, limiting the power dissipation is another crucial aspect to improve the design efficiency which concerns three factors. These are dynamic power dissipation (DPD), static power dissipation (SPD) and the sub-threshold leakage channel. The dynamic power dissipation is controlled by the factors, namely switching power consumption and short circuit power consumption.

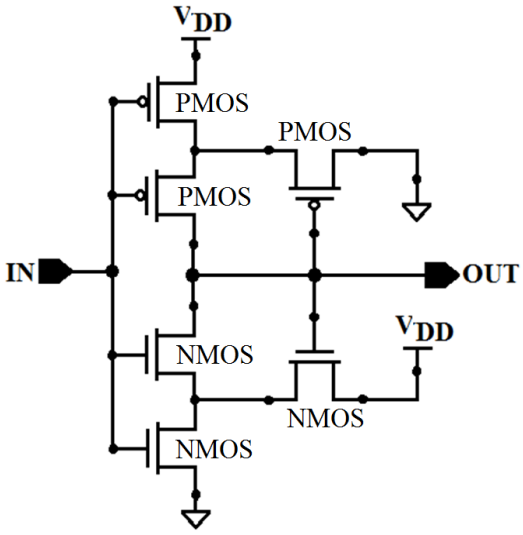


Figure 1: Typical Schmitt Trigger Circuit[3].

The short circuit power is consumed when both the pull-up and pull-down networks are simultaneously active and thus serves a direct-path current flowing between V_{DD} and ground and eventually the power consumed become large[8,9].The short circuit power and switching power dissipation are typically depicted in Fig. 2.

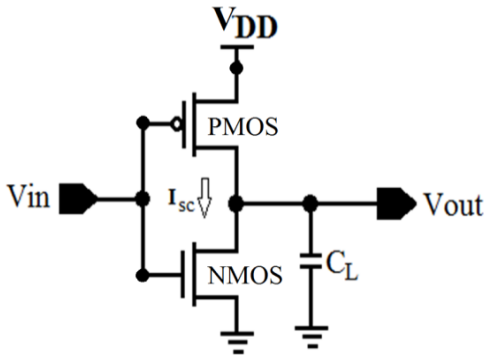


Figure 2: Short circuit power and switching power dissipation[8] .

The switching power dissipation occurs during the switchover of input that causes NMOS transistor turned ON and PMOS transistor turned OFF. The energy is consumed during charging/discharging of C_L. The energy drawn from one rise and following fall transition of the output[4.8.12.13] is, $E = C_L * V_{DD} * V_{DD}$. By lowering the switching activity and clock frequency, DPD can be lowered but it deteriorates the performance[8]. Seemingly reduction of supply voltage degrades the data stability. Hence, DPD can be lowered by reducing load capacitance without degrading the performance. The SPD consumption is, in general, ignored in static CMOS. However, most of these mechanisms are indirectly or directly governed by the device geometries[8, 12, 13].

Substantial research works have been carried out over the recent years to design some novel low power trigger circuits[3-19]. Some recommended construction of a logical threshold voltage control circuit incorporating tunable size of channel in MOS transistors that require demanding mask design, although this tunability is restricted to very small range[1]. In some of the reports we see the implementation of body biasing method to confirm separate switching thresholds for (+ve) and (–ve) going input signals[18], and some reported the use of static inverters to achieve the desired thresholds[19]. Thereafter, Yuan et al. offered a design of adjustable hysteresis where differential duos with tail currents were adopted, however this designs seem unfitting for low voltage manoeuvre[20]. The majority of the previous research on Schmitt trigger did not emphasize on the aspect of low power operation. This is because most of the applications have been using the medium power supply. Nowadays, there are varieties of applications which are mostly relied on either battery or rectified RF signal as the source of energy[21]. This trend is intensifying the need for further research on how to produce the circuits with low power.

Based on all these aforementioned aspects, we intend to look into the design of a better low power Schmitt trigger circuit that should have improved noise immunity, less propagation delay and better hysteresis width. It's worth mentioning that our developed circuits are compared with previous designs of[6] and[7], particularly. At this juncture, our suggested Schmitt trigger circuits are comprehensively analysed in various plausible means: such as by optimizing the width-length ratio of transistors and also by the variation of capacitive loads. As a result of our analysis, we show that our proposed circuit eventuates a large hysteresis width which can be attained by the combination of NAND gate (six transistors), one layer of PMOS feedback and two layers of NMOS feedback.

II. Methodologies

Based on the probe and explorations of the preceding works and theories proposed by Kumar et al.[6] and Sapawi et al.[7] we designed our Schmitt trigger circuit in this paper. The consolidation of these two theories can ensure the construction of Schmitt Trigger with low propagation delay and large hysteresis width. Corollary the basic structure of the Schmitt trigger circuit proffered in our paper is mainly based on the Schmitt trigger designed by Sapawi et al.[7] , where their design are categorized into two parts as follows:

In Part 1, the circuit can be viewed as a NAND gate design. Two p-channel MOSFET (PMOS) transistors (Q1 and Q2) are connected in parallel and two n-channel MOSFET (NMOS) transistors (Q3 and Q4) are connected in series. The propagation delay can be minimized because the total resistances in PMOS circuit are reduced by half with connecting PMOS transistor in parallel. Since, the delay in PMOS transistor is due to its low hole mobility, the circuit proposed by Sapawi et al.[7] is preferred to minimize the delay in PMOS transistor.

In Part 2, the design looks like a feedback circuit for a conventional Schmitt trigger. It consists of two transistors (one PMOS and one NMOS) where both gate terminals are connected together[6]. The Schmitt trigger circuit purposed by Sapawi et al.[7] is shown in Fig. 3.

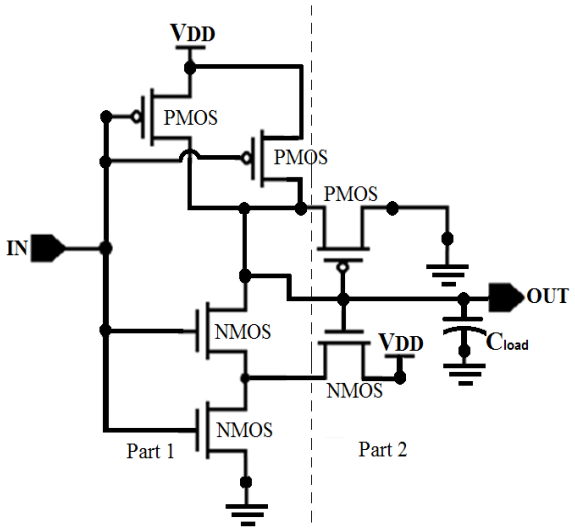


Figure 3: Schmitt trigger circuit[7].

Based on Ref. [6,7], the first proposed Schmitt trigger circuit is designed and analysed to increase hysteresis width. The design has three PMOS transistors (M1, M2, and M3), that are connected in parallel and three NMOS transistors (M4, M5, and M6) connected in series. The first proposed Schmitt trigger circuit is shown in Fig. 4.

Kumar et al.[6] suggested that two layers of a feedback device increases the hysteresis width. This design is same as conventional Schmitt trigger but it has three PMOS transistors, three NMOS transistors and four transistors for feedback circuit. The hysteresis width is increased with increasing switching threshold. It can be done with 'successive tapping' of NMOS and PMOS feedback devices[4]. The Schmitt trigger circuit proposed by Kumar et al.[6] is shown in Fig. 5.

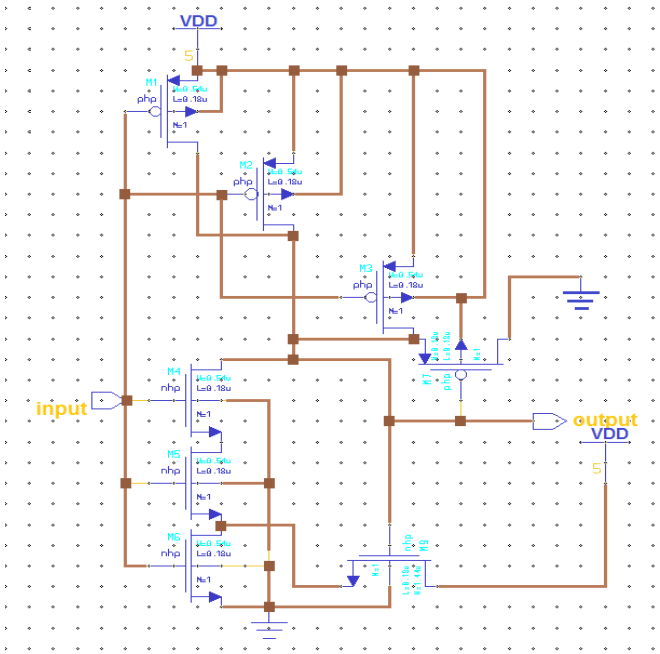


Figure 4: The first proposed Schmitt trigger circuit.

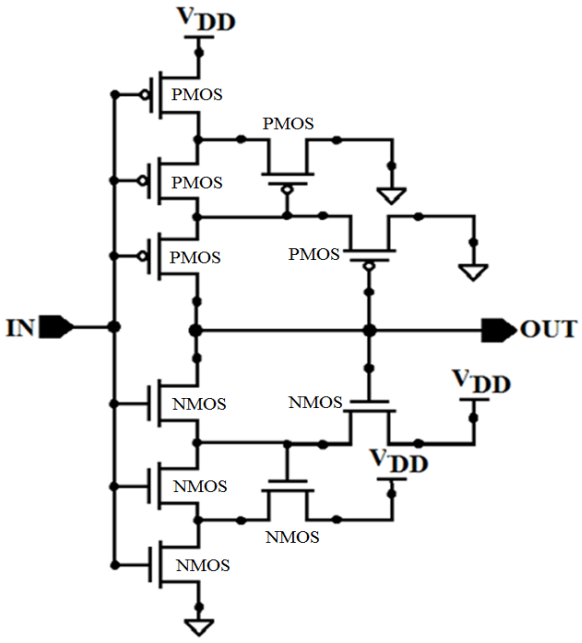


Figure 5: Schmitt trigger circuit with two layers feedback [6].

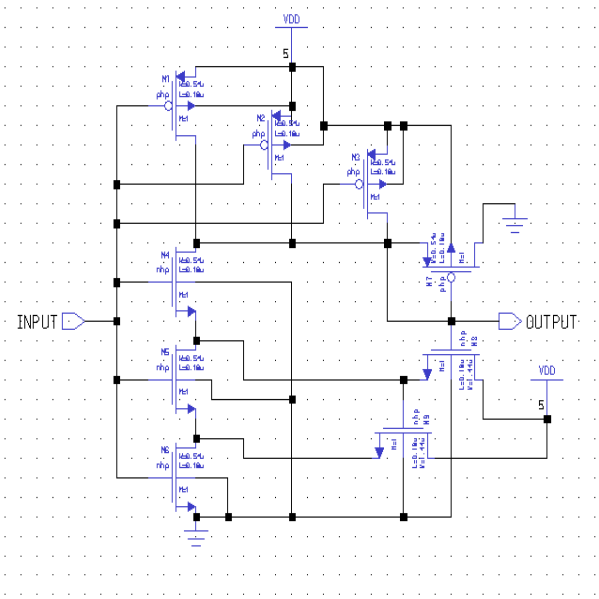


Figure 6: The second proposed Schmitt trigger circuit.

Based on previous works, the second proposed Schmitt trigger circuit is designed and analysed to get better hysteresis width which is compared with the first proposed Schmitt trigger.

The circuit is same as NAND gate by using three PMOS transistors, three NMOS transistors, one layer PMOS feedback and two layer NMOS feedback. The second proposed Schmitt trigger produces large hysteresis width and low power dissipation. The second proposed Schmitt trigger is shown in Fig. 6 and the stick diagram for this proposed Schmitt trigger is shown in Fig. 7. The layout of the second proposed Schmitt trigger is prepared by using the IC Station software and it is shown in Fig. 8. The total area of the proposed Schmitt trigger design is $10.80 \times 10.65\ \mu m^2$.

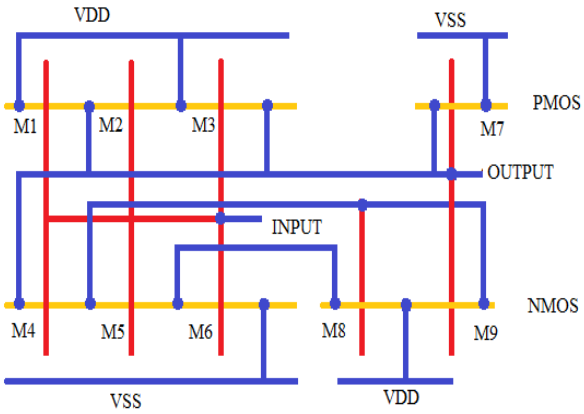


Figure 7: Stick diagram for second proposed Schmitt trigger.

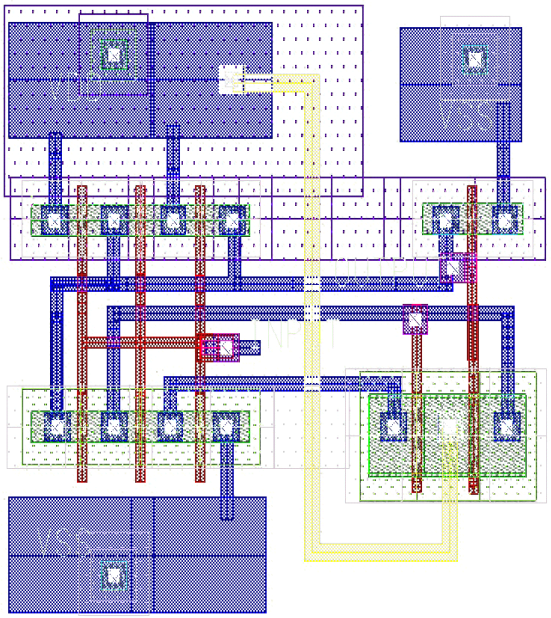
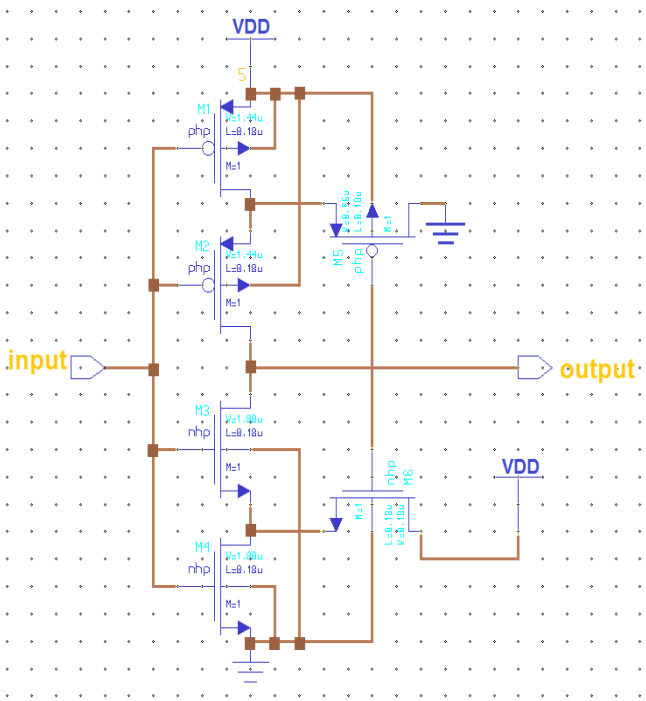


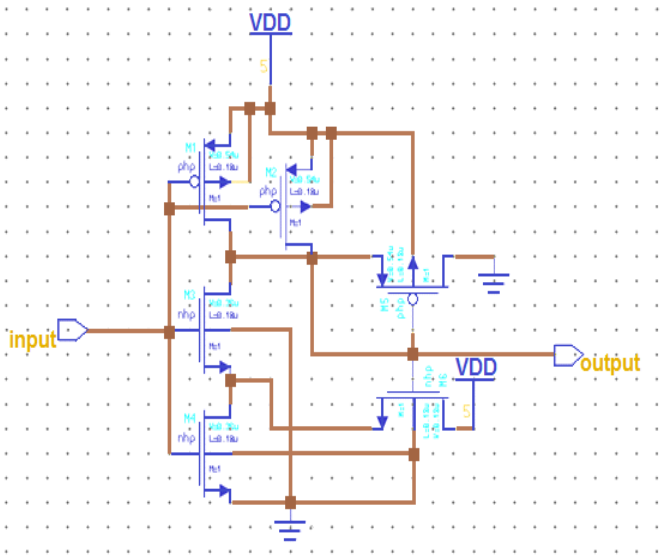
Figure 8: Layout of second proposed Schmitt trigger.

III. Results and Discussion

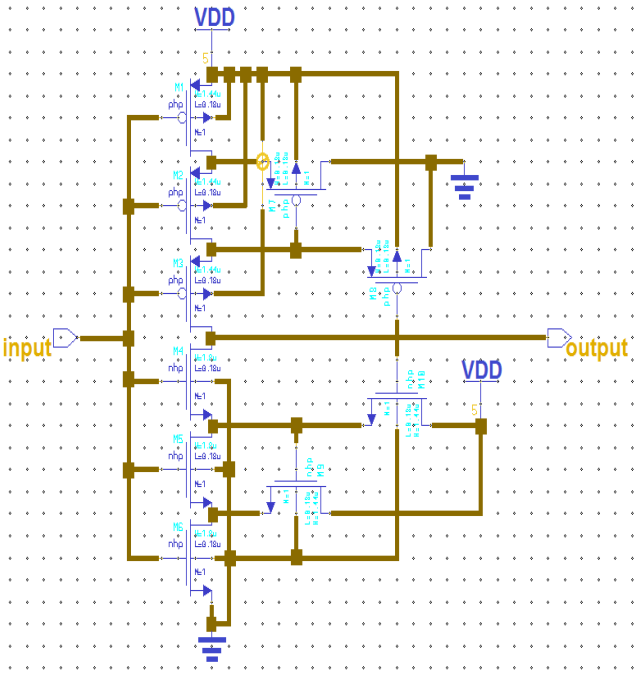
A conventional Schmitt trigger, two Schmitt triggers from previous research works[6,7] and two of our proposed Schmitt triggers were designed and simulated using Silterra's 0.18 µm standard CMOS process Mentor Graphics IC Design. All these five circuit designs and the respective transistor dimensions are shown in Fig. 9 and Table 1. The first design represents the typical Schmitt trigger with the ratio W/L of transistors as shown in the column (a) of Table 1. The second design represents the Schmitt trigger proposed by Sapawi et al.[7] with the ratio W/L of transistors as depicted in the column (b) of Table 1. While, the third design represents the circuit for Schmitt trigger proposed by Kumar et al.[6] with the ratio W/L of transistors as given in the column (c) of Table 1. The fourth and fifth designs represent our two proposed Schmitt triggers with the ratios W/L of transistors as depicted in the (d) and (e) columns of Table 1, respectively. All circuits are analysed and the results are compared in terms of the pertinent features such as propagation delay, hysteresis width and power dissipation. All designs are also analysed using variable load capacitances ranging from 0.0 pF to 0.0015 pF.



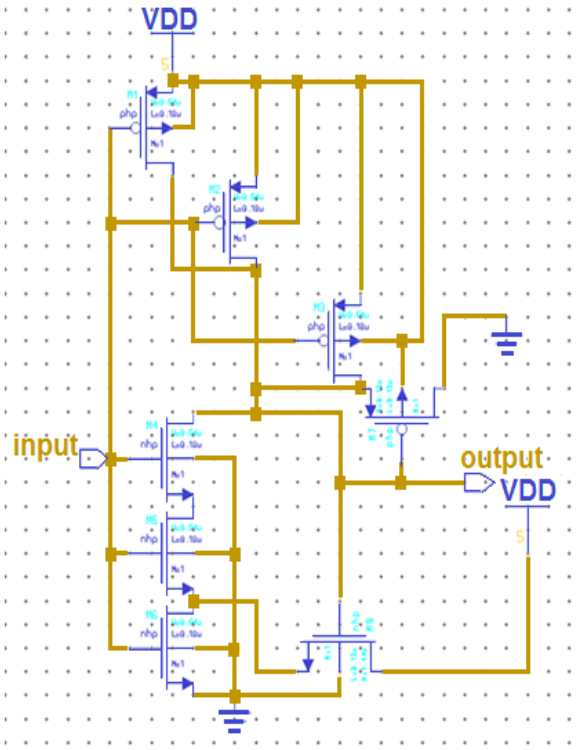
(a)



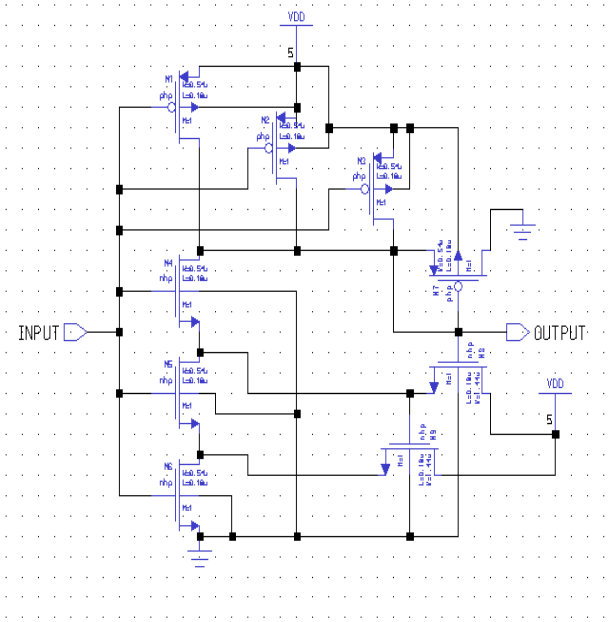
(b)



(c)



(d)



(e)

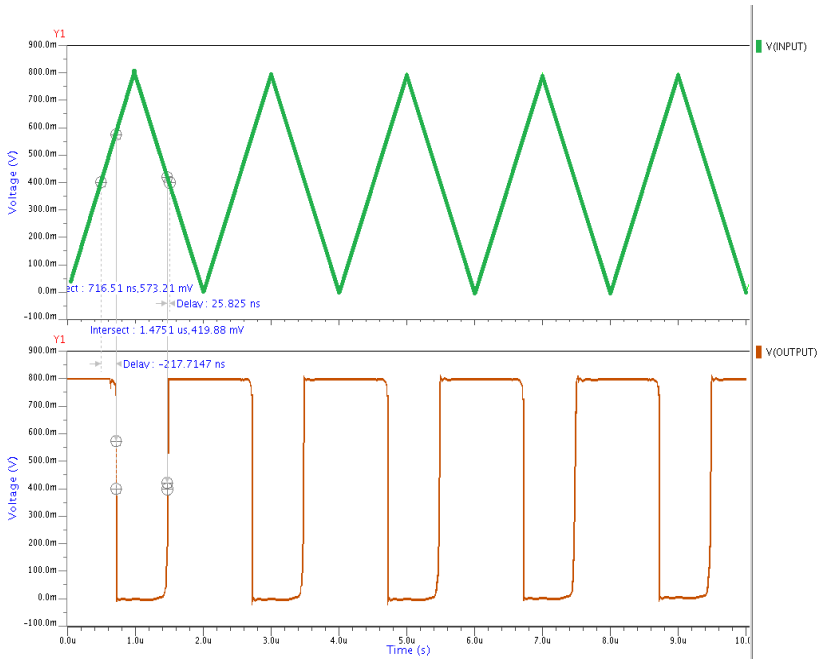
Figure 9: The Schmitt trigger circuits: (a) 1st Design, (b) 2nd Design, (c) 3rd Design, (d) 4th Design, and (e) 5th Design.

Table no 1: The transistor dimensions: for 1st Design, 2nd Design,3rd Design,4th Design,5th Design.

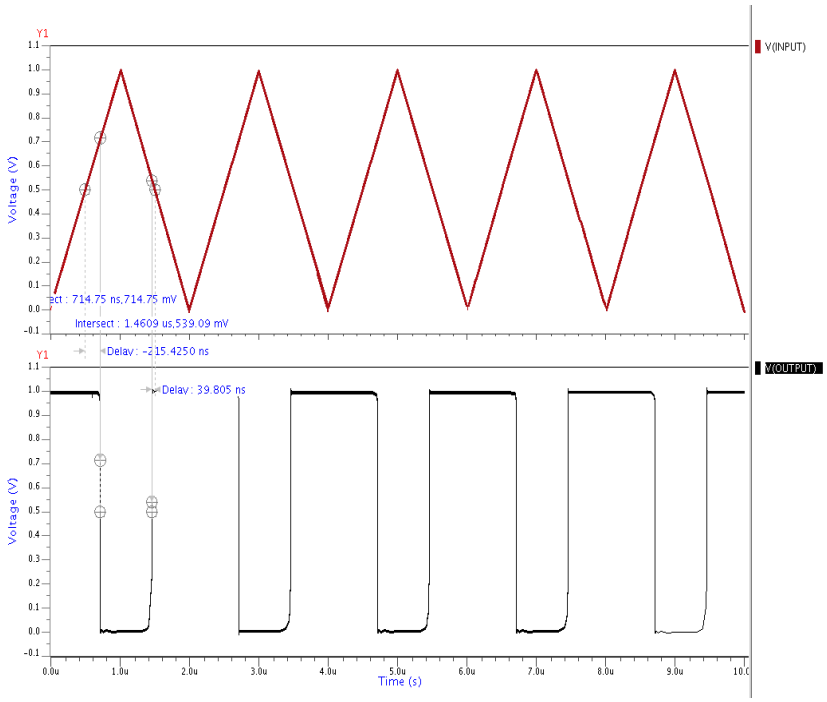
(a) 1st Design		(b) 2nd Design		(c) 3rd Design		(d) 4th Design		(e) 5th Design	
Transistor	W/L(µm)	Transistor	W/L(µm)	Transistor	W/L(µm)	Transistor	W/L(µm)	Transistor	W/L(µm)
M1-PMOS	1.44/0.18	M1-PMOS	0.54/0.18	M1-PMOS	0.54/0.18	M1-PMOS	1.14/0.18	M1-PMOS	0.54/0.18
M2-PMOS	1.44/0.18	M2-PMOS	0.54/0.18	M2-PMOS	0.54/0.18	M2-PMOS	1.14/0.18	M2-PMOS	0.54/0.18
M3-NMOS	1.8/0.18	M3-NMOS	0.36/0.18	M3-PMOS	0.54/0.18	M3-PMOS	1.14/0.18	M3-PMOS	0.54/0.18
M4-NMOS	1.8/0.18	M4-NMOS	0.36/0.18	M4-NMOS	0.54/0.18	M4-NMOS	1.8/0.18	M4-NMOS	0.54/0.18

M5-PMOS	0.18/0.18	M5-PMOS	0.54/0.18	M5-NMOS	0.54/0.18	M5-NMOS	1.8/0.18	M5-NMOS	0.54/0.18
M6-NMOS	1.44/0.18	M6-NMOS	0.18/0.18	M6-NMOS	0.54/0.18	M6-NMOS	1.8/0.18	M6-NMOS	0.54/0.18

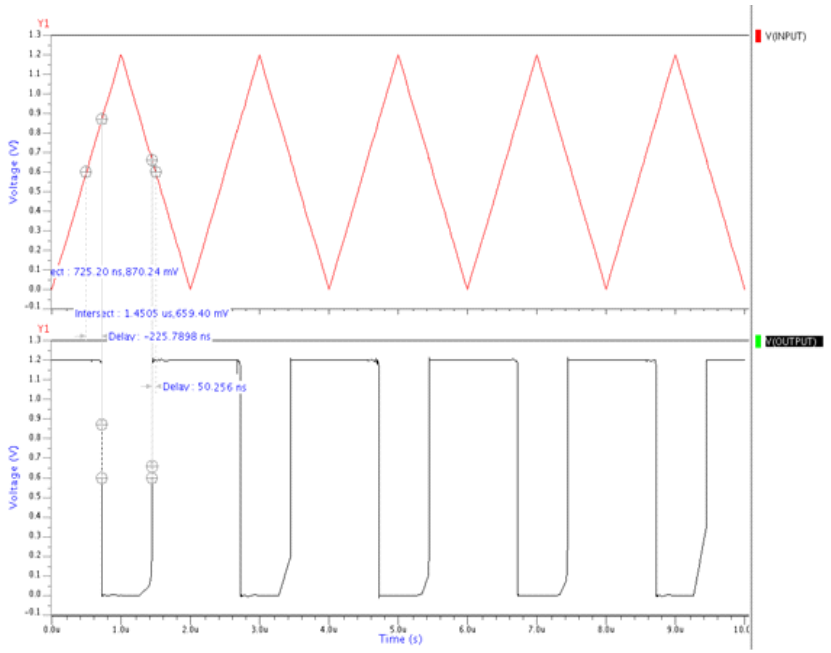
To determine the propagation and hysteresis width of the proposed Schmitt trigger, the pulse voltage is set to 0.8 -1.5 V, rise time to 1 ms, fall time to 1 ms, period to 2 ms and load capacitor to 0 pF. The input and output waveform are shown in Fig. 10.



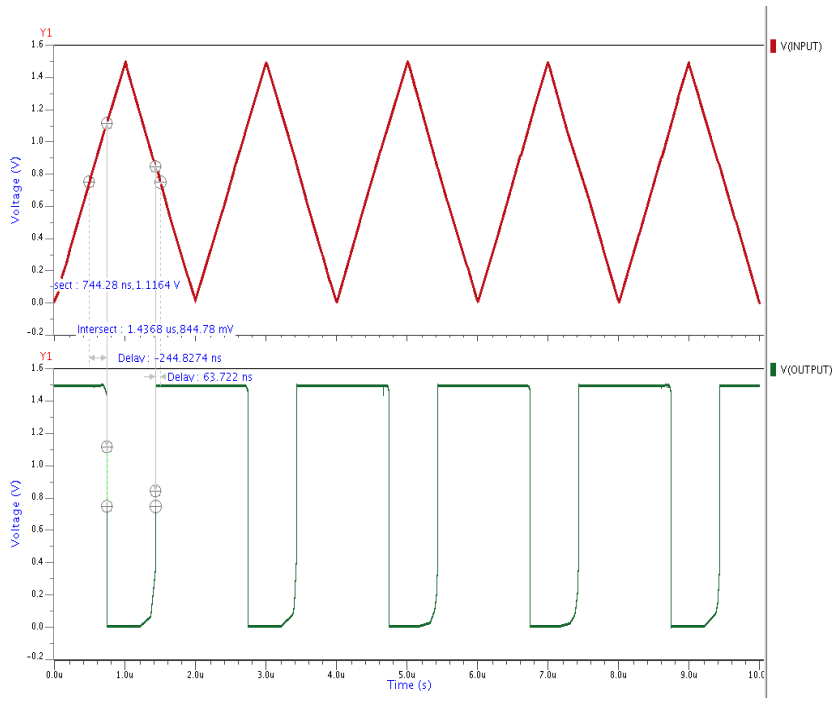
(a)



(b)



(c)



(d)

Figure 10: Input and output waveforms of proposed Schmitt trigger circuit without load for different voltage sources: (a) 0.8 V, (b) 1.0 V, (c) 1.2V, and (d) 1.5V.

It is discerned from Fig. 10 that the proposed Schmitt trigger produces better output waveform at voltage source ranging from 1.0 V to 1.5 V. The results of V_{IH}, V_{IL}, hysteresis width, $t_{PLH,}$ t_{PHL} and Propagation Delay for operating voltage over the range of 0.8V to 1.5V (without load) are shown in Table 2 and Table 3.

Table no 2: The results of V_{IH}, V_{IL} and Hysteresis width.

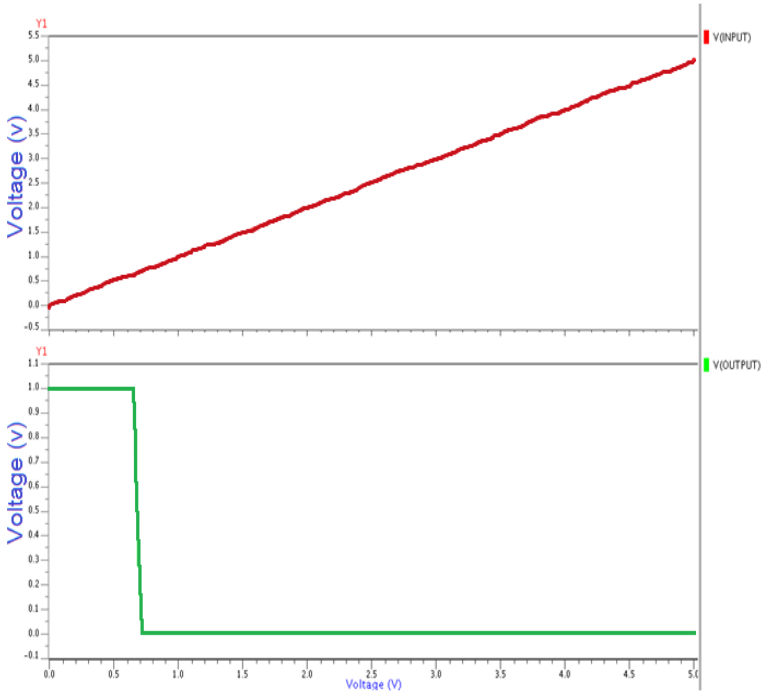
Voltage source (V)	V_{IH} (mV)	V_{IL} (mV)	Hysteresis width (mV)
0.8	573.21	419.88	153.33
1.0	714.75	539.09	175.66

1.2	870.25	659.4	210.85
1.5	1116.4	844.78	271.62

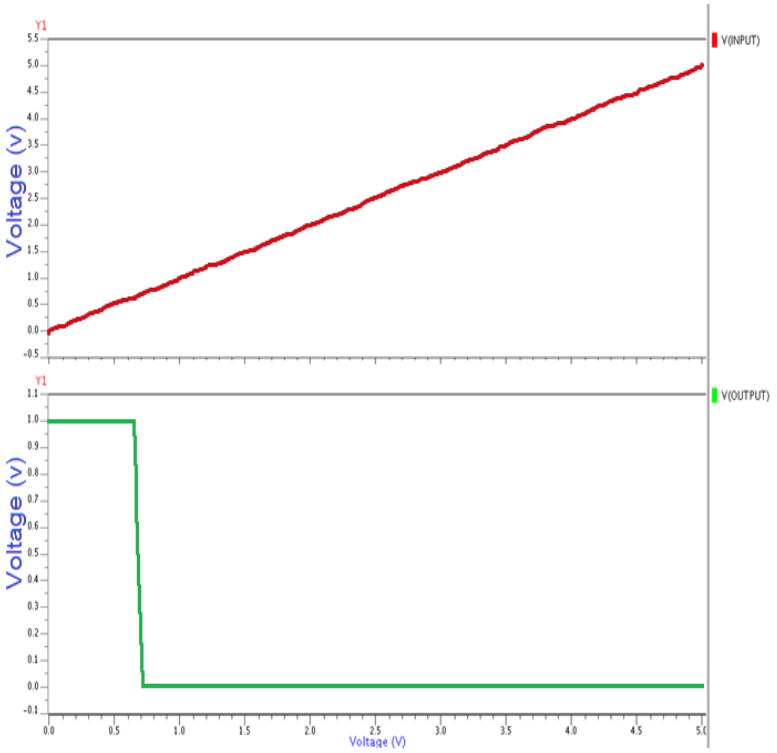
Table no 3: The results of V_{IH}, V_{IL} and Hysteresis width.

Voltage source (V)	t_{PLH} (ns)	t_{PHL} (ns)	Propagation Delay (ns)
0.8	217.715	25.825	191.89
1.0	215.425	39.805	175.62
1.2	225.79	50.256	175.534
1.5	244.827	63.722	181.105

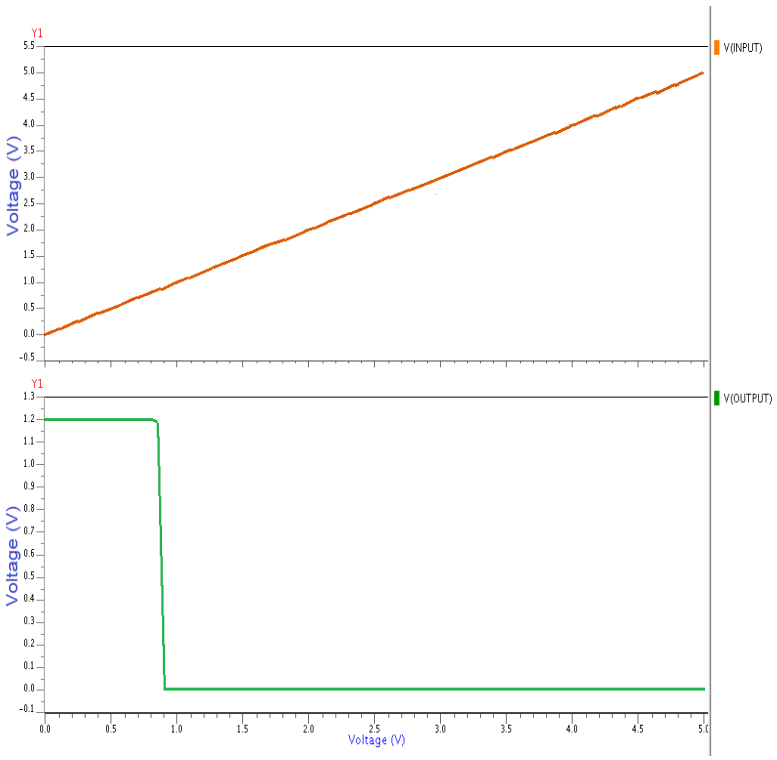
To analyse the effect of the DC transfer curve of the proposed Schmitt trigger, the V_{DD} voltage is set to 0.8V-1.5 V and load capacitor to 0 pF. The input and output waveforms are shown in Fig. 11. The waveform DC transfer is found smooth for all V_{DD} voltages and it reveals that the suggested Schmitt trigger is able to function properly for 0.8 V to 1.5 V.



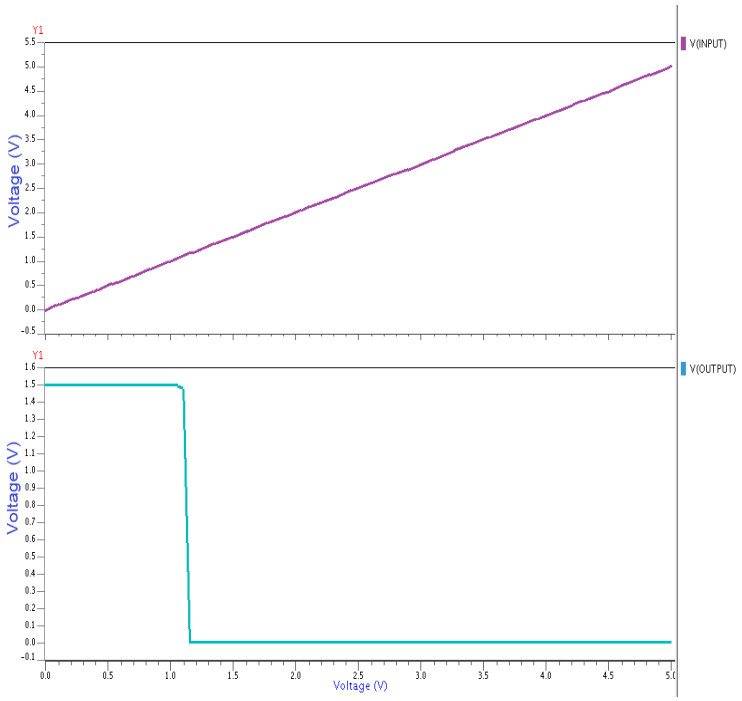
(a)


Y1
V(INPUT)
Voltage (V)
Y1
V(OUTPUT)
Voltage (V)
Voltage (V)

(b)


Y1
V(INPUT)
Voltage (V)
Y1
V(OUTPUT)
Voltage (V)
Voltage (V)

(c)



(d)

Figure 11: Input and output DC transfer curve waveforms of proposed Schmitt trigger circuit without load for different V_{DD} voltages: (a) 0.8 V_{DD}, (b) 1.0 V_{DD}, (c) 1.2 V_{DD} and, (d) 1.5 V_{DD}.

Propagation Delay

The delay times of these analyses are measured in terms of the average of the response time of the gate for rising and falling wave output transitions. As shown in Fig. 12, the propagation delay is increased when the source voltage is decreased. At voltage 1.0-1.5 V and for all the values of the load capacitance ranging from 0.00-0.015 pF, the second (2^{nd}) design exhibits better performance than those of the other four designs. Meanwhile, for lower voltage and reduced load capacitance, the first design shows satisfactory performance. The fourth (4^{th}) and fifth (5^{th}) designs depict improved t_{PLH} but poor t_{PHL} owing to the enhanced stray capacitance. The performance of propagation delay for 5th design is observed 10% larger than that of the 2^{nd} design but it is still acceptable.

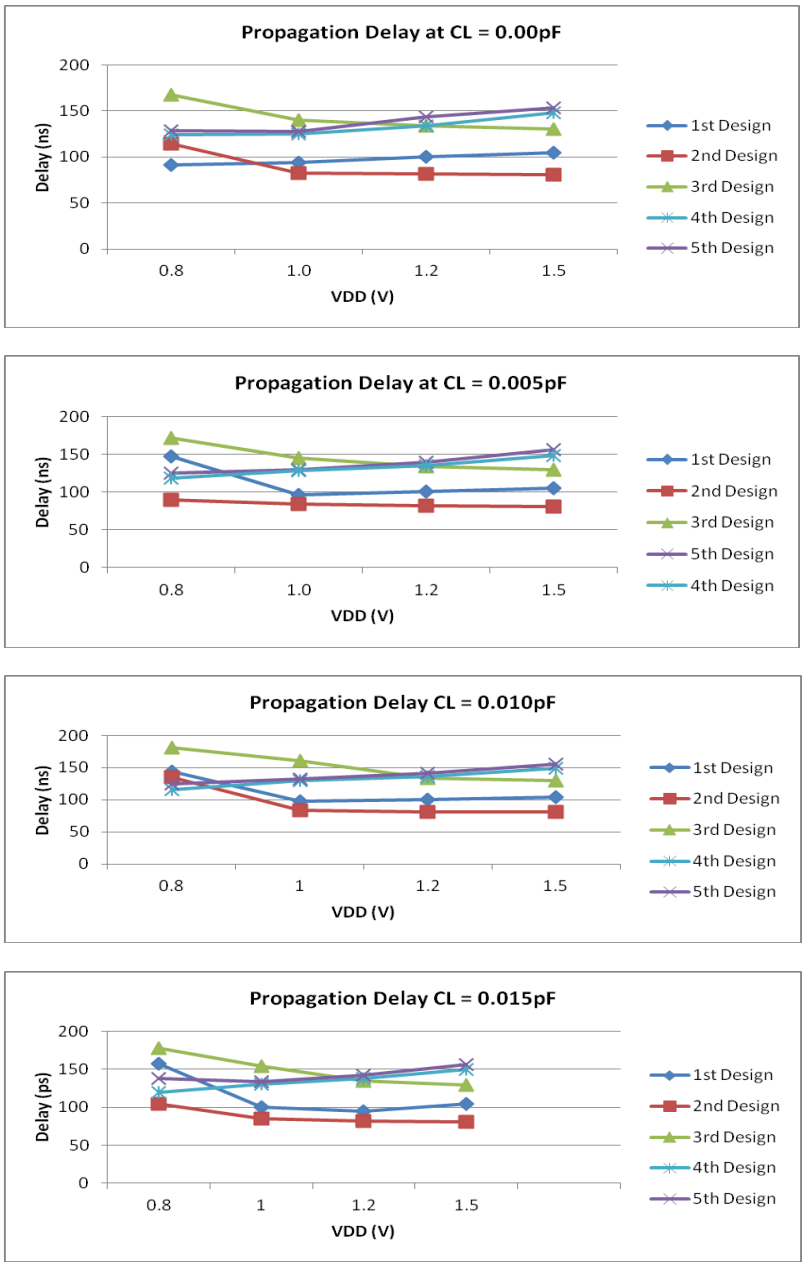


Figure 12: Propagation delay versus V_{DD} for variable load capacitance.

Hysteresis Width

It is observed from Fig. 13 that the hysteresis width is increased insignificantly for all designs except for third design when the load capacitance is increased. For all these designs the hysteresis width almost remains stable with the variation of load capacitance.

An overall observation for the fifth design is that it renders the maximum hysteresis width for V_{DD} of 0.8 V to 1.5 V. It is also found from Fig. 13 that the hysteresis performance of 4th design follows almost the same trend as 5th design. It may be noticed that all the three designs (2^{nd}, 4^{th} and 5^{th}) have achieved the almost same hysteresis width at the V_{DD} of 0.8V.

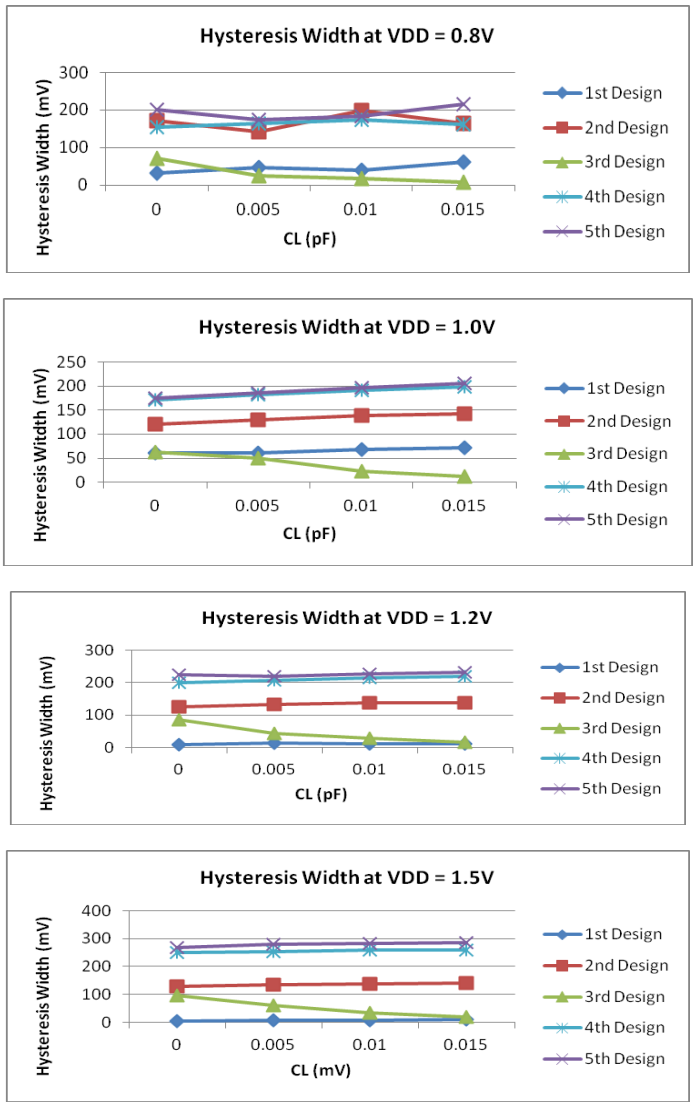


Figure 13: Hysteresis width versus load capacitance for variable V_{DD}.

Power Dissipation

In terms of power dissipation, the 2nd design attains the smallest power dissipation followed by the 4th and 5th design. All designs are simulated with varying V_{DD} so as to analyse the effect of the variation of voltage supply to power dissipation. The power dissipation is found to be increased when the V_{DD} voltage is increased. The value of power dissipation is shown in Table 4.

The power dissipation of proposed Schmitt trigger is observed lower compared to the circuits projected in references[2] and[6]. The area of the layout is reduced approximately by 30% compared to the circuits reported by Chen et al[18]. The hysteresis width is seen large when compared to the circuits of preceding reports which uses lower voltages of 0.8 V to 1.5 V. The propagation delay for proposed Schmitt trigger is perceived high compared to the circuits projected by Sapawi et al.[7] whereas it is spotted lower as compared to the circuit described by kumar et al.[6]

Table no 4: Summary of the values of power dissipation.

Design Type	V_{DD} (V)			
	0.8	1	1.2	1.5
1st Design	4.3165µW	12.0144µW	24.473µW	53.013µW
2nd Design	13.593pW	19.5911pW	26.733pW	39.126pW
3rd Design	3.6309µW	10.2538µW	21.057µW	45.985µW
4th Design	11.911pW	17.193pW	23.452pW	35.582pW
5th Design	16.729pW	22.951pW	31.252pW	47.241pW

Table no 5: Summary of the performance parameters for proposed Schmitt trigger.

Parameters	Values in relevant units
Technology	0.18 µm CMOS
Number of transistor	9
Supply Voltage	0.8 V - 1.5 V
Power Dissipation	16.7295 pW
Hysteresis width	172.68 mV-286.77 mV
Propagation Delay	124.71 ns-156.5 ns
Area	$10.80 \times 10.65\ \mu m^2$

Table no 6: Summary of comparison among proposed Schmitt trigger and previous works.

Mode	Ref. [18]	Ref. [19]	Ref. [2]	Ref. [6]	Ref. [7]	This work
Technology (µm)	0.13	0.5	0.18	0.18	0.35	0.18
Number of Transistor	1	6	15	10	6	9
Supply Voltage (V)	3.3	3.3	0.8-1.5	0.8-1.5	0.8-1.5	0.8-1.5
Hysteresis width (mV)	1500	790	-	100	200	286.77
Power dissipation	-	-	189µW	45.984µW	39.126pW	47.241pW
Propagation Delay	-	-	-	65ns-180ns	80ns-135ns	124.71ns-156.5ns
Area (μm^2)	(8.7 × 19)	-	-	-	-	(10.80×10.65)
Year	2005	2005	2013	2012	2008	-

IV. Conclusion

In this paper, a low voltage, large hysteresis width Schmitt trigger is proposed and it is analysed over a wider range of pertinent parameters as appropriate. Our investigation reveals that the proposed designs have advantages of low power dissipation, large hysteresis width and may be operated with lower voltage (0.8-1.5 V). The power dissipation and propagation delay of one of the proposed circuit are attained as 47.24 pW and 124.71-156.5 ns, respectively. The total area of this proposed Schmitt trigger is $10.80 \times 10.65\ \mu m^2$. It is expected that our proposed circuit would be suitable where large hysteresis width is required to ameliorate the noise margin.

References

[1]. V. Katyal, R. L. Geiger, D. J. Chen, "Adjustable hysteresis CMOS Schmitt triggers," IEEE International Symposium on Circuits and Systems, Seattle, WA, 1938–1941, 2008, doi:10.1109/ISCAS.2008.4541823.

[2]. H. Rashid, M. Mamun, M. S. Amin; and H. Husain, "Design of a Low Voltage Schmitt Trigger in 0.18um CMOS Process With Tunable Hysteresis", Modern Applied Science, **7**(4), 47–54, 2013, doi:10.5539/mas.v7n4p47.

[3]. J. B. Kuang and C. T. Chuang, "PD/SOI CMOS Schmitt trigger circuits with controllable hysteresis," 2001 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers (Cat. No.01TH8517), 283–286, 2001, doi: 10.1109/VTSA.2001.934540.

[4]. N. H. E. Weste, D. Harris, and A. Bannerjee, CMOS VLSI Design: A Circuits and Systems Perspective (3rd Edition). Pearson Education Inc., 2006.

[5]. M. Stayaert, and W. Sansen, "Novel CMOS Schmitt trigger", Electronic Letters, **22**(4), 203–204. 1986.

[6]. M. Kumar, P. Kaur, and S. Thapar, "Design of CMOS Schmitt Trigger", International Journal of Engineering and Innovative Technology (IJEIT), **2**(1), 252–255. 2012.

[7]. R. Sapawi, R. L. S. Chee, S. K. Sahari, and N. Julai, "Performance of CMOS Schmitt Trigger", International Conference on Computer and Communication Engineering, Kuala Lumpur, Malaysia, 1317–1320, 2008, doi: 10.1109/ICCCE.2008.4580818.

[8]. A. Moshovos, B. Falsafi, F. N.Najm, and N. Azizi, "A case for asymmetric-cell cache memories", IEEE Transaction on very large scale integration (VLSI) systems, **13**(7), 155–162, 2005, doi: 10.1109/TVLSI.2005.850127.

[9]. S. Heo, K. Barr, M. Hampton, and K. Asanovic, "Dynamic fine-grain leakage reduction using leakage-biased bitlines", Proc. 29th Annual International Symposium on Computer Architecture, Anchorage, AK, 137–147, 2002, doi: 10.1109/ISCA.2002.1003571.

[10]. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective. (2nd edition), Prentice Hall series in electronics and VLSI, Prentice Hall, Inc. 2003.

[11]. S. -M. Kang, and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw Hill Corporation, Inc., New York, NY10020, 2003.

[12]. Y. Nakagome, M. Horiguchi, T. Kawahara, and K. Itoh, Review and prospect of low-voltage RAM circuits. IBM Journal of Research and Development, **47**(5.6), 525–552, 2003, doi: 10.1147/rd.475.0525.

[13]. B. Majumdar, and S. Basu, "Low Power Single Bitline 6T SRAM Cell With High Read Stability", International Conference on Recent Trends in Information Systems (ReTIS), Kolkata, India, 169–174, 2011, doi: 10.1109/ReTIS.2011.6146862.

[14]. P. Singhanath, A. Suadet, A. Kanjanop, T. Thongleam, S. Kuankid, and V. Kasemsuwan, "Low Voltage Adjustable CMOS Schmitt Trigger", 2011 Fourth International Conference on Modeling, Simulation and Applied Optimization, 1–4, 2011, doi: 10.1109/ICMSAO.2011.5775531.

[15]. A. P. Shah, N. Yadav, A. Beohar, S. K. Vishvakarma, "NMOS only Schmitt trigger circuit for NBTI resilient CMOS circuits", Electronics Letters, **54**(14), 868–870, 2018, doi: 10.1049/el.2018.0546.

[16]. M. Hosseinnejad, A. Erfanian, and M. Azim Karami, "On the Design of Low Power CMOS Schmitt Trigger for Biomedical Application", 27th Iranian Conference on Electrical Engineering (ICEE), 1756–1760, 2019, doi: 10.1109/IranianCEE.2019.8786613.

[17]. Y. Bastan, and P. Amiri, "A Digital-Based Ultra-Low-Voltage Pseudo-Differential CMOS Schmitt Trigger", Journal of Circuits, Systems and Computers, **29**(4), p. 2020002, 2020, doi: 10.1142/S0218126620200029.

[18]. S. -L. Chen, and M. -D. Ker, "A New Schmitt Trigger Circuit in a 0.13- µm/2.5-V CMOS Process to Receive 3.3-V Input Signals", IEEE Transactions on Circuits and Systems- II: Express Briefs, **52**(7), 361–365, 2005, doi: 10.1109/TCSII.2005.850409.
[19]. V. A. Pedroni, "Low-voltage high-speed Schmitt trigger and compact window comparator", Electronics Letter, **41**(22), 1213–1214, 2005, doi: 10.1049/el:20052799.
[20]. F. Yuan, "Differential CMOS Schmitt trigger with tunable hysteresis", Analog Integrated Circuit and Signal Processing, **62** (2), 245–248, 2010, https://doi.org/10.1007/s10470-009-9366-y.
[21]. M. A. Sobhan Bhuiyan, M. Bin Ibne Reaz, M. Binti Omar, M. T. Islam Badal, N. A. Jahan, "Advances in Active Inductor Based CMOS Band-pass Filter," Micro and Nanosystems, **10** (1), 3-10, 2018. doi: 10.2174/1876402910666180524121649