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Design, Simulation and Comparative Analysis of Performance Parameters of a 4-bit CMOS based Full Adder Circuit using Microwind and DSch at Various Technology Nodes

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Abstract:
For any kind of digital circuit, decreasing surface area is one of the crucial factors. Very Large Scale Integration (VLSI) technology is used to diminish the chip area to increase packing density as well as to increase performances. A full adder circuit is a digital circuit that is one of the important components in a computer or any kind of processor for arithmetic operation. Now 64-bit arithmetic operations are being performed. Therefore, we need a huge amount of area to perform this operation. Not only that, we need to reduce power consumption, noise margin but at the same time to increase the speed of operation. Reducing the transistor size can provide us such benefits even we increase the number of bits to be handled in parallel. In this paper, the design and simulation of a 4-bit CMOS based full adder circuit at various technology nodes using Microwind and DSch are presented. After that performances are compared to see how the reduction of transistor size can help to achieve those benefits. The designed circuit is used for the addition of 4-bit binary numbers. To design a 4-bit full adder fully automatic CMOS design process is used. In the first fully CMOS design, schematic and layout of a 4-bit full adder are developed. The layouts are designed and simulated at 90 nm, 65 nm, and 45 nm technology nodes. It has been observed from the simulated results and various outputs that the reduction of node sizes improves the performances of the digital integrated circuit.

Key Word*: CMOS; Full Adder; Technology Node; VLSI; Area; Power Consumption; Noise; Delay.*

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I. Introduction

A binary adder circuit is one of the essential constituents of a digital computer or any kind of microprocessor circuit for use in computing and mobile devices [1]. These digital circuits are widely used in many applications as the principal functioning element. In the VLSI circuits, arithmetic operations, such as addition, subtraction, multiplication, and division can be executed by the binary adder circuit [2]. Hence, the performance of any digital system relies highly on the adder circuits being used. A great deal of arithmetic operations is being done in various types of VLSI, digital signal processing, microcontroller, and microprocessor-based applications. Adder is the basic circuit for all these functions in the integrated circuit. A 1-bit full adder circuit is the basic building block for all of these actions [3]. Using this basic building block 8, 16, 32, and 64-bit adder circuits are generated. However, as the number of bits increases, the area, power, and delay of the circuit increase [4-9]. Therefore, to keep these parameters the same or even to decrease further, the size of the transistor is being curtailed. Hence packing density can be increased and thereby improvements of those parameters can also be obtained [10].

The fundamental binary arithmetic operation in the digital circuits is the binary addition. There are several types of binary adder circuits being used in this regard with some conditions to be fulfilled, such as technology nodes, design techniques, power dissipation, occupied surface area, noise margin, propagation delay, the maximum current is drawn, maximum clock frequency to be applied, etc. When an adder circuit performs the addition operation of two numbers called augend and addend, it yields two numbers called sum and carry. The sum has an equal number of bits to that of the augend and addend but the carry output is of a single bit only. It is to be noted that each bit position of an augend must be added with the corresponding bit position of an addend and the carry out from the position as the carry-in of the current bit position. The result of the addition at a particular bit position produces a bit of the corresponding sum bit and a carry output for the next bit position of the augend and addend [11].

A fast, effective and reliable adder is possible if we can scale down the feature size of the transistor. However, this increases the complexity in the adder circuit design but in many cases, it can enhance the performance of the circuit. Binary adders can be designed and implemented using different types of logic

families, such as Transistor-Transistor Logic (TTL), Complementary Metal Oxide Semiconductor (CMOS) logic [12], High Threshold Logic (HTL), Gate Diffusion Input (GDI) logic, Transmission Gate Logic (TGL), Bipolar CMOS (BiCMOS) logic [13-14], CMOS/BiCMOS logic [15], Emitter Coupled Logic (ECL) circuit [16] and so on. Adders may be implemented at different levels of architectures employing diverse types of logic circuits and are technologies. Of these different types of available technologies, CMOS is the most widely used technology due to its high speed, low power consumption, and compactness [12, 17]. Besides, the CMOS technology node can be scaled down further to improve the circuit performance further [10]. Therefore, to design a high-speed and reliable adder circuit, we have chosen CMOS based logic circuit and a basic transistor. This is the prime objective of our work. Moreover, we want to have a comparative picture of various parameters of a 4-bit full adder circuit as its technology node is scaled down from 90 nm to 45 nm.

The value of the MOS transistor size at which it is scaled down is called a technology node. At present, the available technology nodes are 90 nm, 65 nm, 45 nm, 32 nm, 22 nm, 14 nm, and so on [10, 18]. CMOS based full adders for being employed in energy-efficient circuits to perform arithmetic operations [2, 6-7] as well as to manufacture communication and multi-media based processors [19]. In this paper, we designed a 4-bit full adder circuit at three technology nodes, such as 90 nm, 65 nm, and 45 nm, and then simulated the circuit to get various outputs for several input combinations and compare the results. We found out the area, power consumption, and delay of the circuit at these three nodes and then compare the results to observe the improvement due to the reduction of the transistor size. The paper provides an overview of adder circuit design steps in Microwind [20] and DSch [21] and then layouts are presented with the area required at these three nodes. Finally, several other parameters, such as power dissipation, maximum and average current drawn by the circuit, propagation delay, etc. are calculated to observe the improvement of the circuits due to the node reduction.

II. Literature Review and Problem Statement

High-performance computers with low area occupation and low power consumption are the crucial need for all the designers working in the world's semiconductor industries [10]. In CMOS technology, high packing density and high performances can be achieved by scaling down the device dimensions, supply voltage and threshold voltage continuously and aggressively [10, 18]. Due to this reduction of feature size, channel length becomes shorter and this causes a decrease in threshold voltage and an increase in the sub-threshold leakage current of a transistor during its off condition [22-24]. As such, the static or leakage power intake escalates considerably as compared to the total power consumption by the circuit [25]. However, leakage current reduction techniques have also evolved [26]. Already, considerable research works have been carried out to design and analyze CMOS based full adder circuits in the past. A. U. Alam *et al*. designed a 2-bit parallel binary adder using CMOS NAND gates in Microwind and DSch environment [27]. In 2019, K. M. Priyadarshini *et al*., investigated that the challenges remain in designing the fast and accurate adders while scrutinizing and reasoning on VLSI binary adder circuits and architectures for the improvement of speed and consumption of the least amount of power [28].

R. Uma *et al*. analyzed various adder topologies like ripple carry adder, carry look-ahead adder, carry skip adder, carry select adder, carry increment adder, carry-save adder, and carry bypass adder on their functionalities and performance parameters, such as area, power dissipation, and propagation delay only at 0.12 µm technology node and considering 6 metal layer CMOS using Microwind tool [29].

In 2015, A. Yadav designed an area-efficient 4-bit full adder using CMOS 90 nm technology. He has observed through his simulation results that the semi-custom layout design yields a 72% reduction of silicon area as compared to full automatic CMOS design [30]. On the other hand, M. Sivakumar *et al*. proposed the multi-valued half adder circuit using the Gate Diffusion Input (GDI) logic. They have demonstrated that the power can be reduced using either circuit or logical level optimization techniques. In the circuit level optimization technique, they tried to reduce the area and power consumption. In the logic level optimization technique, Modified Gate Diffusion Input (GDI) logic is used in their proposed Parallel Asynchronous Self-Time Adder (PASTA) technique. The structure of the XOR gate and half adder was reduced to attain the lower amount of area and power requirements. In another approach, they have designed the digital logic circuit using multi-valued logic. For this purpose, they have raised the domain from the two levels ($N = 2$) switching algebra to more than two ($N > 2$) levels [31].

V. R. Tirumalasetty and M. R. Machupalli presented two hybrid 1-bit full adder cells based on both pass transistor and transmission gate logic designs aiming to curtail the power dissipation, use of several transistors, and signal transmission delay of the circuit [32].

A. Shrivastava *et al*. investigated 4 types of Parallel Prefix Adders (PPA), for example, Kogge Stone Adder (KSA), Spanning Tree Adder (STA), Brent Kung Adder (BKA), and Sparse Kogge Stone Adder (SKSA), and conventional three other adders, such as Ripple Carry Adder (RCA), Carry Lookahead Adder (CLA) and Carry Skip Adder (CSA). They simulated these adders in Verilog Hardware Description Language (HDL) in

Xilinx environment and then implemented in Xilinx Spartan 6 Field Programmable Gate Arrays (FPGA). They also measured the circuit's power consumption, propagation delay, and surface area by using an XPower analyzer and compared these parameters among those seven types of adders [33].

C. K. Ray and K. Srinivasarao have designed an XOR gate based on Transmission Gate (TG) logic, which is then applied to device a Carry Select Adder (CSA) circuit and compare it with the CMOS based logic. They replicated the circuit in SPICE simulator at 180 nm technology node with 1.8 V supply voltage. They have verified that a substantial amount of power up to 60% can be saved if TG logic is used instead of CMOS logic to design a CSA within 10-100 MHz transition frequency range [34]. However, R. K. Anand *et al*. used the transmission gate logic to diminish the power and surface area of a half adder circuit by 55.35 % and 40.269% respectively through DSch simulation though the layouts were designed in Microwind [35].

III. Full Adder Design

A full adder is used to execute adding two single-bit data and one-bit input carry to produce two single-bit outputs called sum and output carry. That is, it has three 1-bit inputs *A, B,* $C_{in,}$ and has two 1-bit outputs *S* and C_{out}. The expression for a 1-bit full adder digital circuit is given by-

$S = (A \oplus B) \oplus C_{in}$

$C_{out} = AB + C_{in}(A \oplus B)$

The schematic diagram of a full adder circuit is shown in Fig. 1. It consists of two XOR, two AND, and one OR gate. However, AND and OR gates are basic logic gates but the XOR gate is derived.

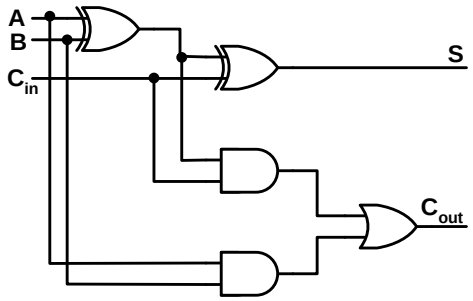

Figure 1. A single bit full adder circuit using logic gates

From this logic circuit diagram, it is clear that the sum (*S*) output is produced in the 2 level gate delay of XOR gates, and output carry (C_{out}) is produced in the 2 level gate delays of the AND and OR gates. The propagation delay of each logic gate is not the same and hence the circuit delay wouldn't be the same. Here, we used 2 XOR gates, 1 OR gate, and 2 AND gates. This circuit diagram may be regarded as a single cell to generate multiple bit circuit by repeating this single cell as many times as many bits are in the multi-bit adder circuit.

However, if we want to design a 4-bit full adder circuit then the inputs *A* and *B* will consist of 4 bits, such as A_0, A_1, A_2, $A_{3,}$ and B_0, B_1, B_2, $B_{3,}$ and carry input will be a single bit, i.e., C_{in}. Similarly, the summation output bits will also contain 4 bits such as S_0, S_1, S_2, S_3 and the carry output bit will be C_{out}. A block diagram of a 4-bit full adder circuit is presented in Fig. 2. There are four blocks in this diagram where each block contains a logic circuit given as in Fig. 1. The truth table of the 4-bit full adder circuit is shown in Table 1. Here *i* means integer number, such as 0, 1, 2, and 3.

Table 1. The truth table of the 4-bit full adder circuit

C_{i-1}	A_i	B_i	S_i	C_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

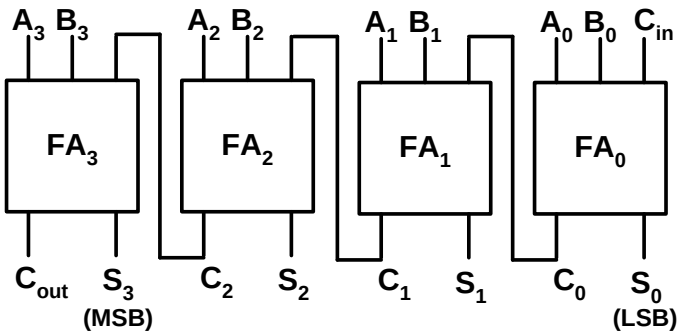

Figure 2. Block diagram of a 4-bit full adder circuit

In the first block of the full adder circuit (FA_0), A_0, B_0, and C_{in} are the input bits and they produce S_0 and C_0 as the output bits. S_0 is the least significant bit (LSB) of the 4-bit sum output. The carry output of the first block is propagated to the input carry position of the second block (FA_1), where A_1, B_1, and C_0 are the input bits and they produce S_1 and C_1 as the output bits. The carry output of the second block is propagated to the input carry position of the third block (FA_2) and in a similar fashion S_2 and C_2 as well as S_3 and C_{out} are generated as the output bits of the third and fourth block respectively. S_3 is the most significant bit (MSB) of the 4-bit output.

Now for each logic gate, we need to design a transistor level diagram. We see that that there are three types of gates, such as XOR, AND, and OR gates. However, the XOR gate is a compound gate derived using AND, OR, and NOT gates. Therefore, if we generate three basic logic gates (AND, OR, and NOT) then combining these gates, we can have a complete circuit diagram of the full adder circuit. The transistor-level circuits of three basic logic gates (AND, OR, and NOT) can be based designed using CMOS technology. However, if we use MOSFETs (both NMOS and PMOS) then we can get NOT gates but NAND and NOR gates instead of AND and OR gates respectively. Of course, using NOT gate in front of NAND and NOR gates, we can obtain AND and OR gates respectively. In Figs. 3 (a), (b), and (c), we have shown such transistor-level circuits. Repetitive use of these transistors can be combined to generate the whole 4-bit CMOS based full adder circuits. Therefore, the MOS transistor is a unit constituent of any kind of digital circuitry.

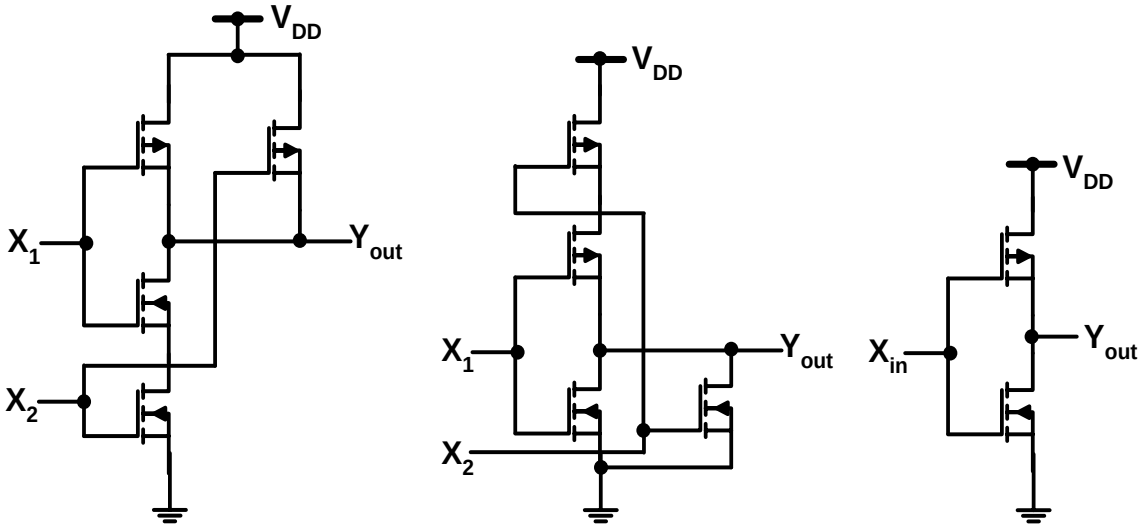

Figure 3. MOS transistor-level circuit diagram of the logic gates (a) NAND gate, (b) NOR gate, (c) NOT gate

IV. Results and Discussions

The transistor-level design layout of the 4-bit adder circuit is shown in Fig. 4 using 45 nm technology nodes. However, the actual length is 50 nm. The total length (L) of the designed layout of the circuit is 50λ, that is 50×25= 1250 nm = 1.25 μm (considering λ = L/2). We used a total of 56 NMOS and 56 PMOS transistors. Since this is a CMOS based circuit, therefore, an equal number of NMOS and PMOS transistors should be utilized in the design.

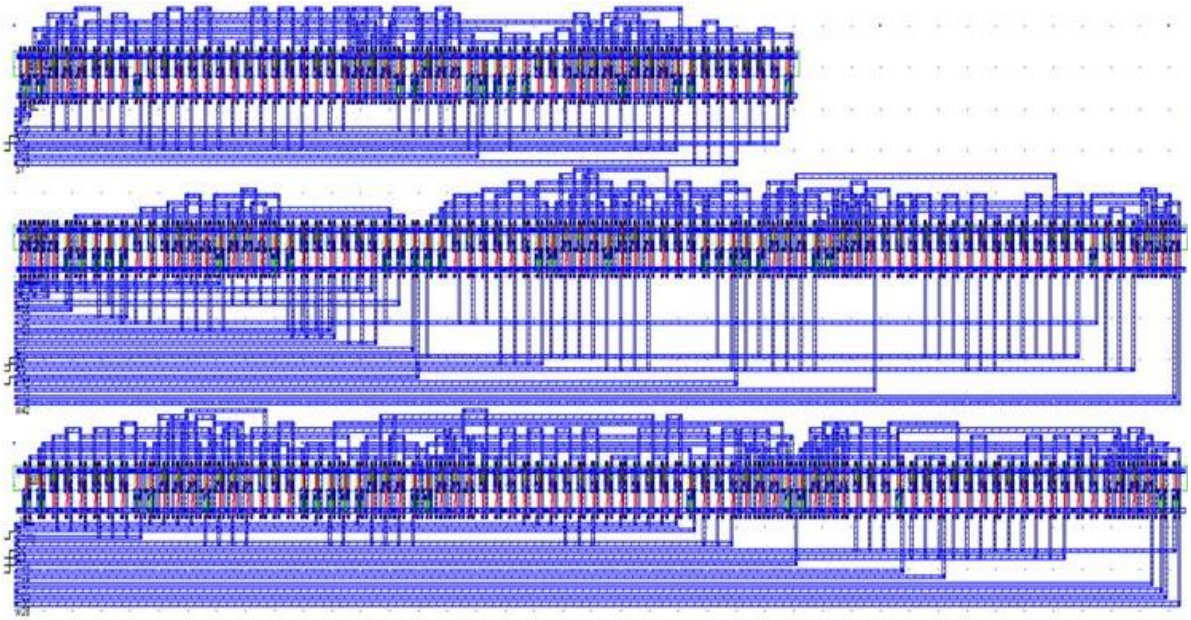

Figure 4. CMOS full adder circuit designed at 45 nm technology node

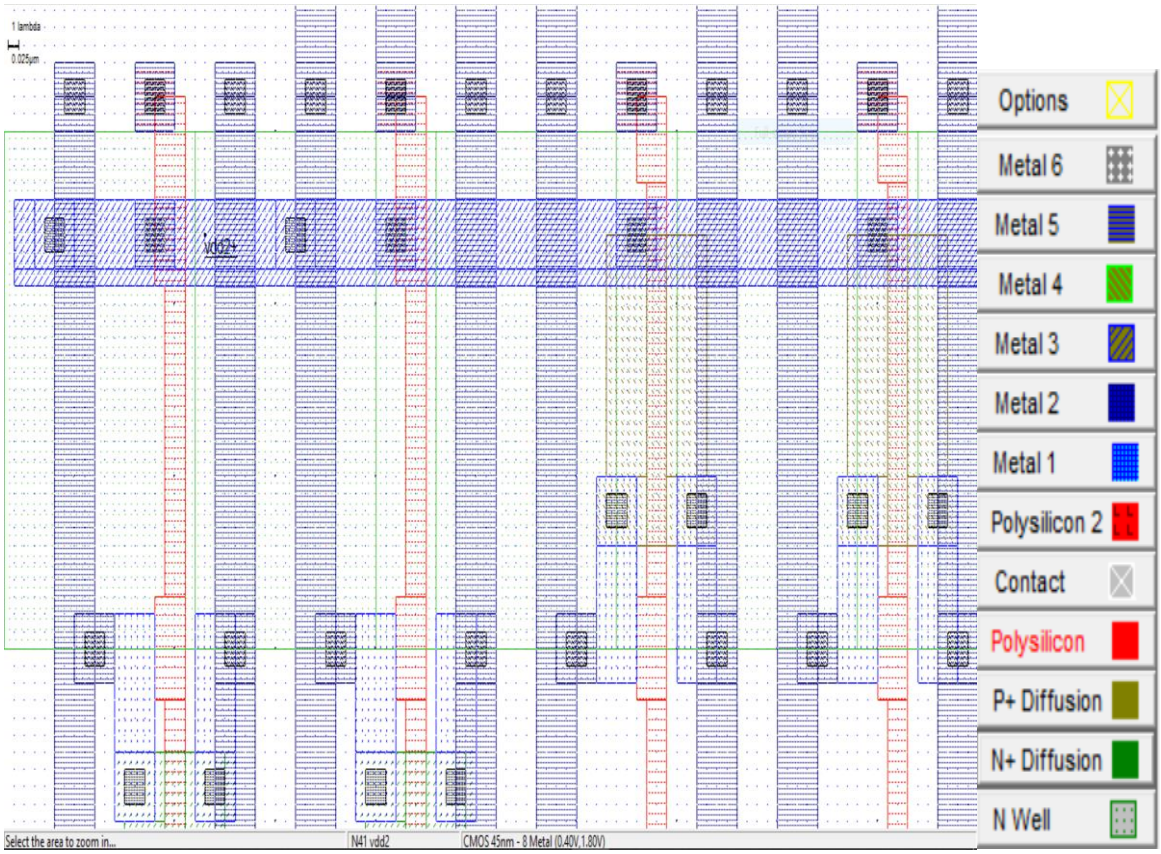

Figure 5. A portion of CMOS layout design for a 4-bit full adder circuit at 45 nm technology node

A portion of the designed layout of the adder circuit using CMOS 45 nm technology is shown in Fig. 5 to understand the design clearly. On the right side, it is shown that there are 8 types of metal, 2 types of polysilicon, one type of p^+ diffusion, and one type of n^+ diffusion as well as an n-well. Using these available symbols we have drawn the full layout. The simulation parameters are 0.4 V and 1.8 V for binary 0 and 1 for low and high-level voltages respectively. The operating temperature is 27°C and the noise input is 0.1 V (rms).

To see whether the designed transistor is at 45 nm node works properly or not characteristics curves of each transistor are simulated. One of these curves (I_{ds}-V_{ds} output characteristics) for the NMOS transistor are

shown in Fig. 6. The threshold voltage (V_{th}) of this transistor is 0.2 V, width (W) is 450 nm and oxide thickness (t_{ox}) is 1.8 nm. We computed the simulation time and propagation delay also, and it was only 7 s and 5 ns respectively. The maximum current drawn by the circuit is $I_{dd,max}$ = 0.519 mA but the average current drawn by the circuit is $I_{dd,avg}$ = 0.116 mA.

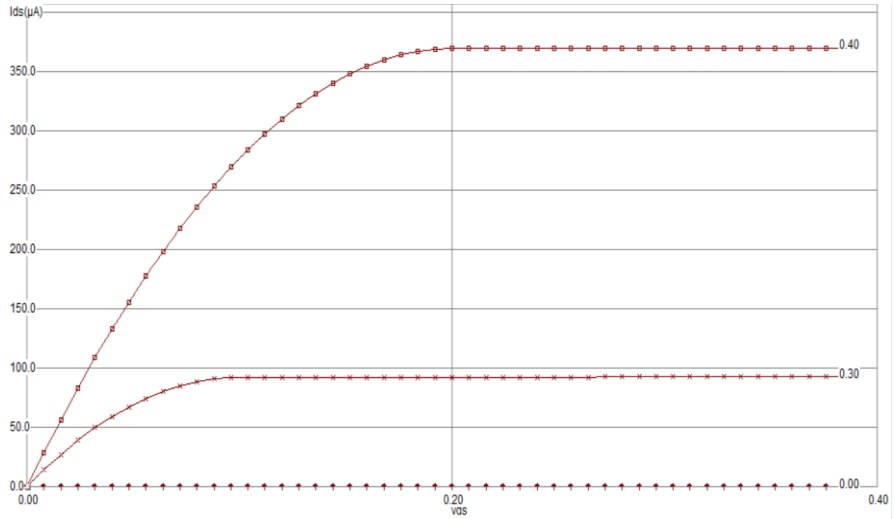

Figure 6. Output characteristics curves for an NMOS transistor at 45 nm technology node

A part of the 3-D CMOS based layout design of our 4-bit full adder circuit is shown in Fig. 7.

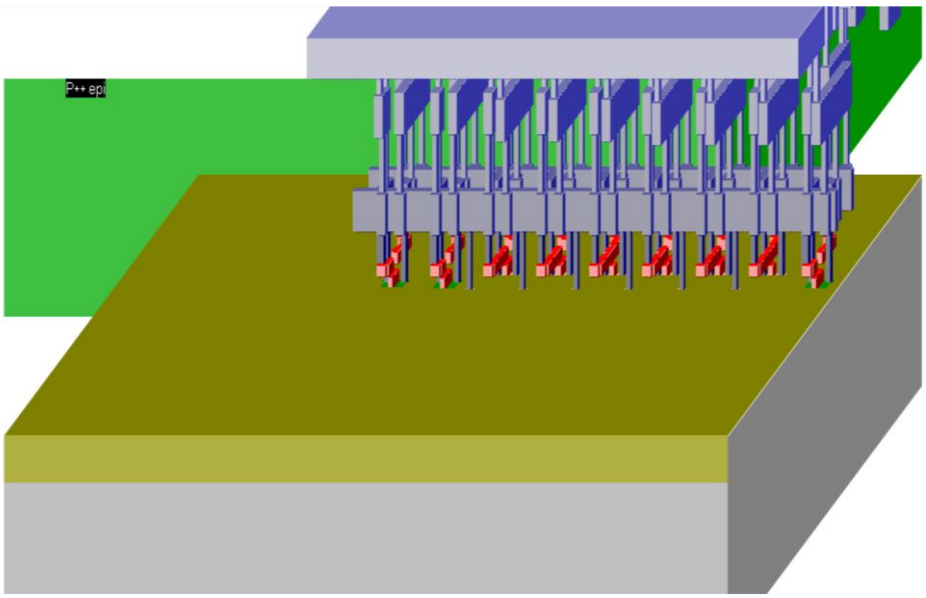

Figure 7. 3-D CMOS based layout 4-bit CMOS full adder

We have also calculated the inductance and capacitance of the layout and found out 5 nH and 1 pF respectively. From here we computed the value of resonant frequency as-

$$f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{5\times10^{-9}\times10^{-12}}} = 2.2508 \text{ GHz}$$

At this frequency, we computed the intrinsic, inductive, and capacitive impedances respectively as-

$$Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{5\times10^{-9}}{10^{-12}}} = 70.71\Omega$$

$$Z_L = 2\pi fL = 2\pi \times 2.2508 \times 10^9 \times 5 \times 10^{-9} = 70.71\Omega$$

$$Z_C = \frac{1}{2\pi fC} = \frac{1}{2\pi\times2.2508\times10^9\times1\times10^{-12}} = 70.71\Omega$$

We know that at the resonant frequency, the values of these three parameters will be the same. That is, as per our calculation, the layout design is correct. In Table 2, a comparative report of various parameters of the design at three technology nodes of 45 nm, 65 nm, and 90 nm is presented.

Table 2. Various parameter values of the layout designed at 45 nm, 65 nm, and 90 nm technology nodes

Technology Nodes (nm)	Capacitance (fF)	Inductance (nH)	Rise Time Delay (ns)	Fall Time Delay (ns)	Area Required (μm^2)	Power Consumption (μW)	Maximum Current Drawn (mA)	Average Current Drawn (mA)
45	37.25	0.20	0.031	0.012	20.736	0.522	0.519	0.116
65	9.64	0.08	0.017	0.008	43.264	2.781	1.752	0.746
90	5.73	0.05	0.000	0.001	82.944	3.297	16.249	2.317

Area Calculation Of CMOS 1-bit Full Adder Cell

Width of the layout = $16\times8\lambda = 128\lambda$ nm

Length of the layout = $10\times8\lambda = 80\ \lambda$ nm

Therefore, the amount of area required by a CMOS 1-bit full adder cell = $128\lambda\times80\lambda = 1024\lambda^2$ nm^2

Hence, the total area of CMOS 4-bit full adder circuit = $4\times1024\lambda^2 = 40960\lambda^2$ nm^2

From the above formula, now we can calculate the total area of a 4-bit CMOS full adder circuit required at each technology node. Since we know that λ = feature size/2.

At 45 nm technology node, $\lambda = 45/2 = 22.5$ nm and therefore, the total area required by the CMOS 4-bit full adder circuit = $40960\times22.5^2 = 20736000$ $nm^2 = 20.736$ μm^2.

Similarly, areas required at the other two technology nodes are computed and are presented in Table 2. Various simulation parameters for different technology nodes are presented in Table 3.

Table 3. Simulation parameter comparison of 3 different technology nodes

Technology Node (nm)	Supply Voltage (V)	I/O Supply (V)	Temperature (°C)	Simulation Time (ns)	Number of Simulation Steps
45	0.40	1.80	27.00	20	2
65	0.70	2.50	27.00	10	2
90	1.20	2.50	27.00	10	2

Interconnect parameters, such as capacitance, inductance, and resistance are also calculated for 3 various technology nodes and are shown in Table 4. It has been observed that as the feature size goes down, the value of inductance decreases but the capacitance increases. However, the resistance remains the same as it decreases the length and area of the circuit in the same proportion.

Table 4. Interconnect parameter comparison at 3 different technology nodes

Technology Node (nm)	Interconnect Capacitance (fF/mm)	Interconnect Metal Capacitance (fF/mm)	Interconnect Inductance (nH/mm)	Interconnect Resistance (Ω/mm^2)
45	92.79	5.664	0.446	0.049
65	86.74	5.025	0.516	0.049
90	76.36	4.425	0.591	0.049

V. Conclusion

In this work, we have discussed the design process of a 4-bit CMOS based full adder architecture in DSch environment and then simulated the architectures at three CMOS technology nodes of 45 nm, 65 nm, and 90 nm in Microwind environment. Based on the performance comparison of various nodes, we have demonstrated that the surface area occupied at the 45 nm technology node is the lowest. Besides, at this node, the power consumption, maximum and average current drawn by the circuit is also the lowest. However, resistance doesn't change though inductance decreases and capacitance increases. In the future, more such analysis may be done for various other digital circuit architectures. This type of study can be applied in the basic understanding of the VLSI circuit design course and laboratory-based simulation works.

References

[1]. S. Purohit and M. Margala, "Investigating the Impact of Logic and Circuit Implementation on Full Adder Performance" IEEE Transaction Very Large Scale Integration (VLSI) Systems, Vol. 20, no.7, pp.1327-1331, July 2012.

[2]. B. R. Zeydel, D. Baran, V. G. Oklobdzija, "Energy -Efficient Design Methodologies: High-Performance VLSI Adders" IEEE Journal of solid-state circuits, Vol. 45, no. 6, pp.1220-1233, June 2010.

[3]. R. Yousuf and Najeeb-ud-din, "Synthesis of Carry Select Adder in 65 nm FPGA" IEEE Region 10 conference, pp.1-6, 2008.

[4]. A. M. Shams, T. W. Darwish, and M. A. Bayomui, "Performance analysis of low power 1 -bit CMOS full adder cells," IEEE Transactions on Very Large Scale Integration (VLSI) Systems," Vol. 10, Issue 1, February 2002.

[5]. C. Senthilpari, S. Kavitha and J. Joseph, "Lower Delay and Area Efficient Non-Restoring Array Divider by Using Shannon Based Adder Technique," Proc. of ICSE 2010, Melaka, Malaysia, pp.140-144, 2010.

[6]. M. A.-Hernandez and M. L.-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol.19, No. 4, April 2011.

[7]. Y. Kim, Y. Zhang and P. Li "An Energy-Efficient Approximate Adder with Carry Skip for Error Resilient Neuromorphic VLSI Systems," IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp.130-137, 2013.

[8]. A. Gangwar and R. Mehra, "CMOS Design and Low Power Full Adder Using .12 Micron Technology," International Journal of research in computer applications and robotics ISSN 2320-7345 Vol.1, Issue.2, pp. 1-6, March-April 2013.

[9]. P. Saini and R. Mehra "Leakage Power Reduction in CMOS VLSI Circuits," International Journal of Computer Applications (0975 – 8887), Vol. 55, No. 8, pp. 42-48, October 2012.

[10]. M. H. Bhuyan, "History and Evolution of CMOS Technology and its Application in Semiconductor Industry," Southeast University Journal of Science and Engineering (SEUJSE), 1999-1630, vol. 11, no. 1, June 2017, pp. 28-42.

[11]. T. L. Floyd, "Digital Fundamentals," Eleventh Edition, Prentice-Hall, 2011.

[12]. R. H. Krembec, C. M. Lee, H. S. Law, "High-Speed compact circuits with CMOS", IEEE Journal of Solid-State Circuits, vol. 17, pp. 614-619, June 1982.

[13]. J. B. Kuo, S. S. Chen, C. S. Chiang, K. W. Su and J. H. Lou, "A 1.5 V BiCMOS dynamic logic circuit using a "BiPMOS pull-down" structure for VLSI implementation of full adders," in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 41, no. 4, pp. 329-332, April 1994.

[14]. J. B. Kuo, H. J. Liao, H. P. Chen, "A BiCMOS dynamic carry look-ahead adder circuit for VLSI implementation of high-speed arithmetic unit", IEEE J. Solid-State Circ., vol. 28, no. 3, pp. 375-378, Mar. 1993.

[15]. T. Hayashi, T. Doi, M. Asai, K. Ishibashi, S. Shukuri, A. Watanabe, M. Suzuki, "The SDC cell—A novel design methodology for high-speed arithmetic modules using CMOS/BiCMOS precharged circuits", IEEE J. Solid-State Circ., vol. 25, no. 2, pp. 430-409, April 1990.

[16]. D. L. Harame, E. F. Crabbe, J. D. Cressler, J. H. Comfort, J. Y. C. Sunj, "A high-performance epitaxial single-base ECL BiCMOS technology", Digest of IEDM, pp. 19-22, 1992.

[17]. J. Yuan, C. Sevensson, "High-speed CMOS circuit techniques", IEEE Journal of Solid-State Circuits, vol. 24, no. 1, pp. 62, Feb. 1989.

[18]. M. H. Bhuyan, "Analytical Modeling of the Pocket Implanted Nano Scale n-MOSFETs," PhD Thesis, EEE Department, BUET, Dhaka, Bangladesh, 2011.

[19]. M. C. Parameshwara and H. C. Srinivasaiah, "Choice of Adders for Multimedia Processing Applications: Comparison of Various Existing and a Novel 1-Bit Full Adder," IOSR Journal of Electronics and Communication Engineering, e-ISSN: 2278-2834, p-ISSN: 2278-8735. Vol. 10, Issue 3, Ver. IV, May-June 2015, pp. 69-73.

[20]. S. M. Aziz, E. Sicard and S. B. Dhia "Effective Teaching of the Physical Design of Integrated Circuits Using Educational Tools," IEEE Transactions on Education, Vol. 53, No. 4, pp. 517-531, November 2010.

[21]. https://www.microwind.net/dsch, retrieved on 10 December 2019.

[22]. M. H. Bhuyan, "RF Semiconductor Devices Technology: History and Evolution, Prospects and Opportunities, Current and the Future," Southeast University Journal of Science and Engineering (SEUJSE), 1999-1630, vol. 12, no. 2, December 2018, pp. 28-39.

[23]. M. H. Bhuyan and Q. D. M. Khosru, "Linear Pocket Profile Based Threshold Voltage Model for Sub-100 nm n-MOSFET," International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering, p: 2010-376X, e: 2010-3778, vol. 4, no. 8, 2010, pp. 1187-1192.

[24]. M. H. Bhuyan and Q. D. M. Khosru, "An Analytical Subthreshold Drain Current Model for Pocket Implanted Nano Scale n-MOSFET," Journal of Electron Devices, France, 1682-3427, vol. 8, October 2010, pp. 263-267.

[25]. V. K. Madasu and B. Kedharnath, "Leakage power reduction by using sleep methods," International Journal of Engineering and Computer Science, Vol. 2, No.9, 2013.

[26]. K. Roy, S. Mukhopadhyay, H. Manmoodi-Meimand, "Leakage current mechanism and leakage reduction techniques in deep sub micrometer CMOS circuits," Proceedings of the IEEE, Vol. 91, 2003.

[27]. A. U. Alam, N. Majid and S. K. Aditya, "Layout Design of a 2-bit Binary Parallel Ripple Carry Adder Using CMOS NAND Gates with Microwind," Dhaka University Journal of Science, vol. 60, no. 1 pp. 103-108, January 2012.

[28]. K. M. Priyadarshini, R. S. E. Ravindran and P. R. Bhaskar, "A Detailed Scrutiny and Reasoning on VLSI Binary Adder Circuits and Architectures," International Journal of Innovative Technology and Exploring Engineering (IJITEE), ISSN: 2278-3075, Vol. 8 Issue 7, May 2019.

[29]. R. Uma, V. Vijayan, M. Mohanapriya and S. Paul, "Area, Delay and Power Comparison of Adder Topologies," International Journal of VLSI Design and Communication Systems, Vol. 3, No. 1, February 2012.

[30]. A. Yadav, "Area Efficient 4-Bit Full Adder Design using CMOS 90 nm Technology," International Journal of Electrical and Electronics Engineering, e-ISSN: 1694-2310, p-ISSN: 1694-2426, Vol. 2, Special Issue 1, pp. 45-48, 2015.

[31]. M. Sivakumar and S. Omkumar, "Implementation of Area & Power Optimized VLSI Circuits Using Logic Techniques," IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), e-ISSN: 2319-4200, p-ISSN: 2319-4197, Vol. 7, Issue 4, Ver. I, pp. 15-23, July-August 2017.

[32]. V. R. Tirumalasetty and M. R. Machupalli, "Design and analysis of low power high-speed 1-bit full adder cells for VLSI applications," International Journal of Electronics, vol. 106, no.4, pp. 521-536, 2019. DOI: 10.1080/00207217.2018.1545256.

[33]. A. Shrivastava, S. Churhe, H. Bhagat and R. Wamankar, "Design and estimation of delay, power and area for parallel prefix adders," International Journal of Engineering Research and Application, ISSN: 2248-9622, Vol. 7, Issue 4, Part 5, , pp. 01-08, April 2017.

[34]. C. K. Ray and K. Srinivasarao, "Design and Implementation of Low power Carry Select Adder Using Transmission Gate Logic," IOSR Journal of VLSI and Signal Processing (IOSR-JVSP), e-ISSN: 2319–4200, p-ISSN: 2319–4197, Vol. 5, Issue 3, Ver. I, pp. 28-32, May-June 2015.

[35]. R. K. Anand, K. Singh, P. Verma and A. Thakur, "Design of Area and Power Efficient Half Adder Using Transmission Gate," International Journal of Research in Engineering and Technology, e-ISSN: 2319-1163, p-ISSN: 2321-7308, Vol. 04, Issue 4, pp. 122-127, April 2015.