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Basic Topologies of MOS Single-Stage Amplifiers. DC Analysis For Maximum Input-Voltage Swing And Amplification

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Abstract: *Review basic MOS single-stage amplifier topologies and perform comparative DC analysis in order to determine for each topology the pair: (maximum input voltage swing, amplification). The results will be used in following works for the design of more advanced circuits such as differential amplifiers, current sources and operational amplifiers.*
Keywords: *integrated analog design, single-stage amplifier, dc-analysis, voltage-swing, amplification*

I. Introduction

The aim of the current work is to give a didactic review to the design of the most basic MOS single-stage amplifiers [1,2]. The aim is on creating appropriate single-stage amplifier designs delivering maximum input voltage swing and maximum amplification.

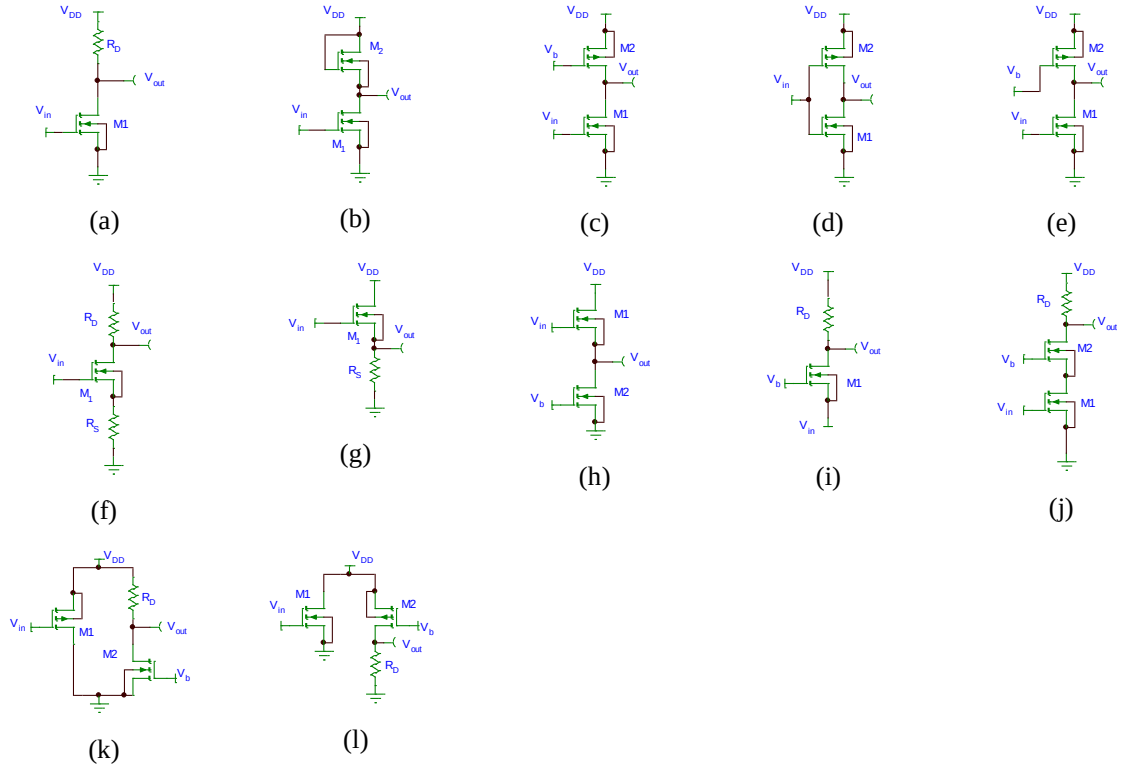
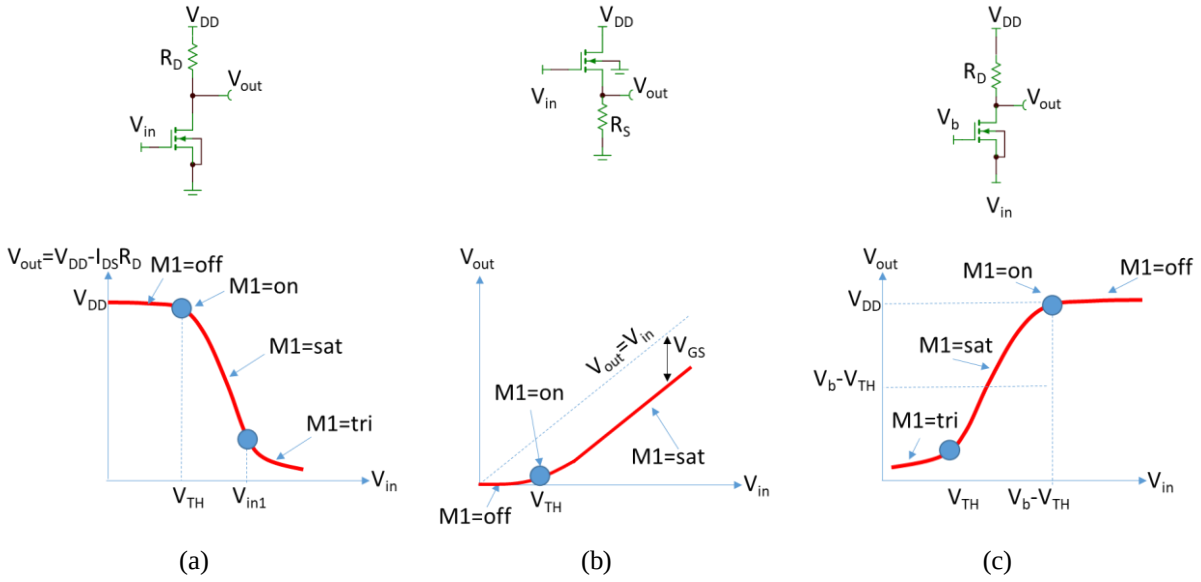


Figure 1. MOS single stage topologies. (a) Common-source stage with resistive load, (b) Common-source stage with diode-connected load, (c) Common-source stage with current-source load, (d) Common-source stage with active load, (e) Common-source stage with triode load, (f) Common-source stage with source degeneration, (g) Source follower, (h) Source-follower with nMOS as current source, (i) Common-gate stage, (j) Cascode-stage, (k) Simple folded cascode, (l) Simple folded cascode with nMOS input.

Figure 1 shows the topologies that will be studied, specifically the: (a) Common-source stage with resistive load, (b) Common-source stage with diode-connected load, (c) Common-source stage with current-source load, (d) Common-source (CS) stage with active load, (e) Common-source stage with triode load, (f) Common-source stage with source degeneration, (g) Source follower (CD), (h) Source-follower with nMOS as current source, (i) Common-gate (CG) stage, (j) Cascode-stage, (k) Simple folded cascode, (l) Simple folded cascode with nMOS input.

Figure 2 shows qualitatively the standard DC characteristic of common-source stage (with resistive load), the common-drain stage (source-follower) and the common-gate stage. Section II presents the basic assumptions followed by all designs.

Section III presents the DC analysis results for the proper transistor sizing for all the topologies. Section IV presents the DC comparison of the standard (CS, CD, and CG) topologies, Section V presents the DC comparison of all the CS topologies. Section VI presents the DC comparison of the CD topologies. Finally, section VII presents the quantification of the CG topology DC curve.

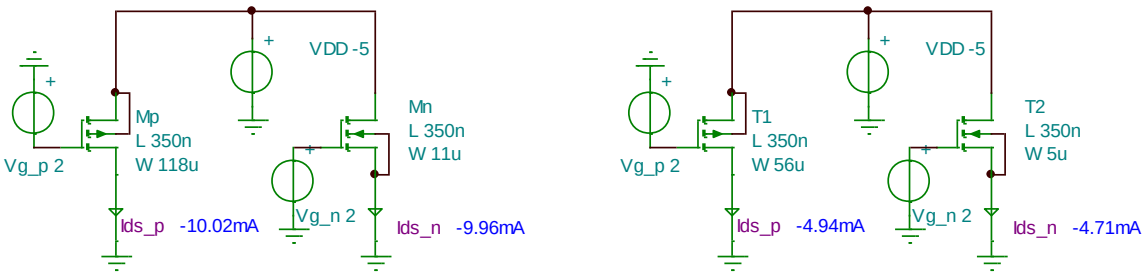


(a) (b) (c)

Figure 2. Basic topologies of single-stage amplifiers and corresponding DC characteristics. (a) Common-source, (b) Common-drain (source-follower), (c) Common-gate. (V_{TH} is the threshold voltage)

II. Design And Simulation Considerations

In the following simulations, enhancement MOSFETs with 4 terminals are used. The simulation are performed using TINA Pro 9 design suite [3]. The MOS model used is the built-in TINA's BSIM3 version of SPICE, with transistor parameters for nMOS and pMOS shown in Table 1 and Table 2, respectively.In all topologies the pMOSback-gate electrode is connected to $V_{DD}$and thenMOS back-gate electrode in the ground. The simple folded-cascode and simple folded-cascode with nMOS input, will use biasing current sources and Fig. 3 shows appropriate biasing of nMOS and pMOS that can be used as current-sources for 10mA and 5mA.



(a) (b)

Figure 3. Appropriate bias and sizing to obtain approximately (a) 10mA and (b) 5mA constant current-sources with a pMOS and annMOS. These are used to bias devices when necessary.

Table 1. nMOS-BSIM3 SPICE parameters.

vth0 [V]	700m	pclm [-]	1.3	Wwl [m]	0
k1 [V^½]	500m	pdiblc1 [-]	390m	Ll [m]	0
k2 [-]	0	pdiblc2 [-]	8.6m	Lln [-]	1
k3 [-]	80	pdiblcb [1/V]	0	Lw [m]	0
k3b [1/V]	0	drout [-]	560m	Lwn [-]	1
w0 [m]	2.5u	pscbe1 [V/m]	424M	Lwl [m]	0
nlx [m]	174n	pscbe2 [m/V]	10u	ute [-]	-1.5
vbm [V]	-3	pvag [-]	0	kt1 [V]	-110m
dvt0 [-]	2.2	delta [V]	10m	kt1l [Vm]	0
dvt1 [-]	530m	ngate [1/cm²]	0	kt2 [-]	22m
dvt2 [1/V]	-32m	alpha0 [m/V]	0	ua1 [m/V]	4.31n
dvt0w [1/m]	0	beta0 [V]	30	ub1 [(m/V)²]	-7.61E-18
dvt1w [1/m]	5.3M	rsh [Ohm/square]	0	uc1 [m/V²[1/V]	-56p
dvt2w [1/V]	-32m	js [A/m²]	100u	at [m/s]	33k
u0 [m²/V/s]	67m	jsw [A/m]	0	prt [Ohm-µm]	0
ua [m/V]	2.25n	xpart [-]	0	tox [m]	15n
ub [(m/V)²]	5.87E-19	cgso [F/m]	0	xj [m]	150n
uc [m/V²[1/V]	-46.5p	cgdo [F/m]	0	gamma1 [V^½]	0
vsat [m/s]	80k	cgbo [F/m]	0	gamma2 [V^½]	0
a0 [-]	1	cj [F/m²]	500u	npeak [1/cm³]	1.7E+17
ags [1/V]	0	cjsw [F/m]	500p	nsub [1/cm³]	6.0E+16
b0 [m]	0	cjswg [F/m]	500p	vbx [V]	0
b1 [m]	0	mj [-]	500m	xt [m]	155n
keta [1/V]	-47m	mjsw [-]	330m	vfbcv [V]	-1
a1 [1/V]	0	mjswg [-]	330m	Lmin [m]	0
a2 [-]	1	pb [V]	1	Lmax [m]	1
rdsw [Ohm-µm]	0	pbsw [V]	1	Wmin [m]	0
prwb [V^(-½)]	0	pbswg [V]	1	Wmax [m]	1
prwg [1/V]	0	nj [-]	1	NoiA [-]	1.0E+20
wr [-]	1	xti [-]	3	NoiB [-]	50k
Wint [m]	0	cgsl [F/m]	0	NoiC [-]	-1.4p
Lint [m]	0	cgdl [F/m]	0	em [V/m]	41M
dwg [m/V]	0	ckappa [F/m]	600m	af [-]	1
dwb [m/(V^½)]	0	cf [F/m]	0	ef [-]	1
voff [V]	-80m	clc [m]	100n	kf [-]	0
nfactor [-]	1	cle [-]	600m	tnom [°C]	27
eta0 [-]	80m	dlc [m]	0	l [m]	10u
etab [1/V]	-70m	dwc [m]	0	w [m]	10u
dsub [-]	560m	elm [-]	5	mobMod [-(flag)]	1
cit [F/m²]	0	Wl [m]	0	capMod [-(flag)]	2
cdsc [F/m²]	240u	Wln [-]	1	nqsMod [-(flag)]	0
cdscb [F/(Vm²)]	0	Ww [m]	0	noiMod [-(flag)]	1
cdscd [F/(Vm²)]	0	Wwn [-]	1	binUnit [-(flag)]	1

Table 2. pMOS-BSIM3 SPICE parameters.

vth0 [V]	-700m	pclm [-]	1.3	Wwl [m]	0
k1 [V^½]	500m	pdiblc1 [-]	390m	Ll [m]	0
k2 [-]	0	pdiblc2 [-]	8.6m	Lln [-]	1
k3 [-]	80	pdiblcb [1/V]	0	Lw [m]	0
k3b [1/V]	0	drout [-]	560m	Lwn [-]	1
w0 [m]	2.5u	pscbe1 [V/m]	424M	Lwl [m]	0
nlx [m]	174n	pscbe2 [m/V]	10u	ute [-]	-1.5
vbm [V]	-3	pvag [-]	0	kt1 [V]	-110m
dvt0 [-]	2.2	delta [V]	10m	kt1l [Vm]	0
dvt1 [-]	530m	ngate [1/cm²]	0	kt2 [-]	22m
dvt2 [1/V]	-32m	alpha0 [m/V]	0	ua1 [m/V]	4.31n
dvt0w [1/m]	0	beta0 [V]	30	ub1 [(m/V)²]	-7.61E-18
dvt1w [1/m]	5.3M	rsh [Ohm/square]	0	uc1 [m/V²[1/V]	-56p
dvt2w [1/V]	-32m	js [A/m²]	100u	at [m/s]	33k
u0 [m²/V/s]	25m	jsw [A/m]	0	prt [Ohm-µm]	0
ua [m/V]	2.25n	xpart [-]	0	tox [m]	15n
ub [(m/V)²]	5.87E-19	cgso [F/m]	0	xj [m]	150n
uc [m/V²[1/V]	-46.5p	cgdo [F/m]	0	gamma1 [V^½]	0
vsat [m/s]	80k	cgbo [F/m]	0	gamma2 [V^½]	0
a0 [-]	1	cj [F/m²]	500u	npeak [1/cm³]	1.7E+17
ags [1/V]	0	cjsw [F/m]	500p	nsub [1/cm³]	6.0E+16
b0 [m]	0	cjswg [F/m]	500p	vbx [V]	0
b1 [m]	0	mj [-]	500m	xt [m]	155n
keta [1/V]	-47m	mjsw [-]	330m	vfbcv [V]	-1
a1 [1/V]	0	mjswg [-]	330m	Lmin [m]	0
a2 [-]	1	pb [V]	1	Lmax [m]	1
rdsw [Ohm-µm]	0	pbsw [V]	1	Wmin [m]	0
prwb [V^(-½)]	0	pbswg [V]	1	Wmax [m]	1
prwg [1/V]	0	nj [-]	1	NoiA [-]	9.9E+18
wr [-]	1	xti [-]	3	NoiB [-]	2.4k
Wint [m]	0	cgsl [F/m]	0	NoiC [-]	1.4p
Lint [m]	0	cgdl [F/m]	0	em [V/m]	41M
dwg [m/V]	0	ckappa [F/m]	600m	af [-]	1
dwb [m/(V^½)]	0	cf [F/m]	0	ef [-]	1
voff [V]	-80m	clc [m]	100n	kf [-]	0
nfactor [-]	1	cle [-]	600m	tnom [°C]	27
eta0 [-]	80m	dlc [m]	0	l [m]	10u
etab [1/V]	-70m	dwc [m]	0	w [m]	10u
dsub [-]	560m	elm [-]	5	mobMod [-(flag)]	1
cit [F/m²]	0	Wl [m]	0	capMod [-(flag)]	2
cdsc [F/m²]	240u	Wln [-]	1	nqsMod [-(flag)]	0
cdscb [F/(Vm²)]	0	Ww [m]	0	noiMod [-(flag)]	1
cdscd [F/(Vm²)]	0	Wwn [-]	1	binUnit [-(flag)]	1

III. DC Analysis For Transistor Sizing

The following subsections consider each topology in detail, simulating mainly the transistor width *W* and the external resistances R_D and R_S, in order to get anappropriate DC V_{in}-V_{out} curve, capable of allowing high input- voltage swing and high amplification if the circuit is biased properly. In all cases, V_{DD}=5V,V_{in}=0-5V, L=0.35μm.

A. COMMON-SOURCE STAGE WITH RESISTIVE LOAD

Figure 4 considers the common-source stage topology for various *W*s. The $W=100\mu m$and $R_D=1kOhm$are considered as acceptable values for this topology, for the overall stage comparison that will follow.

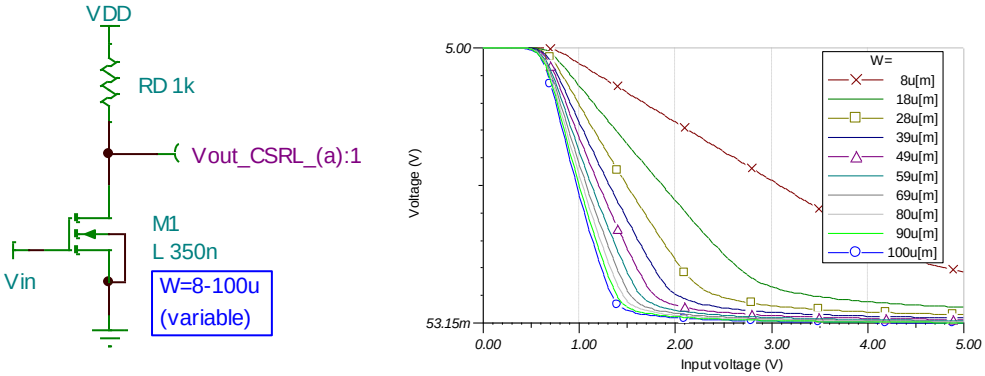


Figure 4.DC analysis of common-stage with resistive load amplifier for various *W*s, and $R_D=1kOhm$.

B. COMMON-SOURCE STAGE WITH DIODE-CONNECTED LOAD

Figure 5 considers the common-source stage with diode-connected load topology for various *W*s for transistor *M3*. The $W_3=1\mu m$and $W_2=5\mu m$are considered as acceptable values for this topology, for the overall stage comparison that will follow.

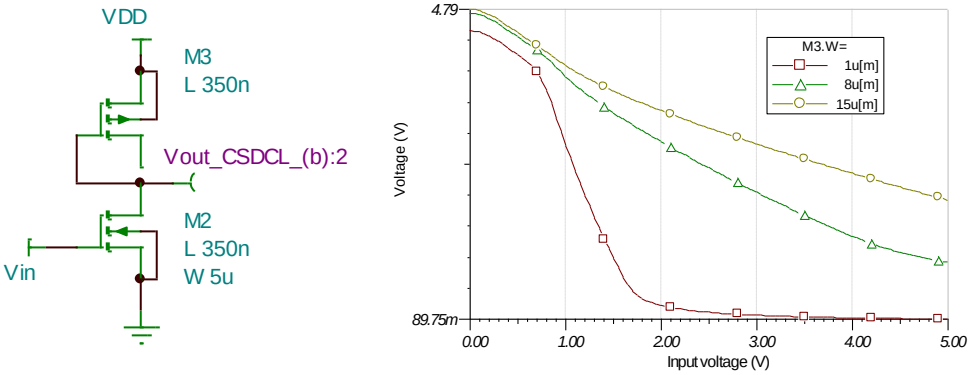


Figure 5. DC analysis for the common-source stage with diode-connected load, for various values of W_3. In all cases, $W_2=5\mu m$.

C. COMMON-SOURCE STAGE WITH CURRENT-SOURCE LOAD

Figure 6 shows the simulation results for the common-source stage with current-source load topology, for $W_4=1\mu m$, $V_{bp}=-2V$ and various W_3. The $W_3=100\mu m$will be used for the for the overall stage comparison that will follow.

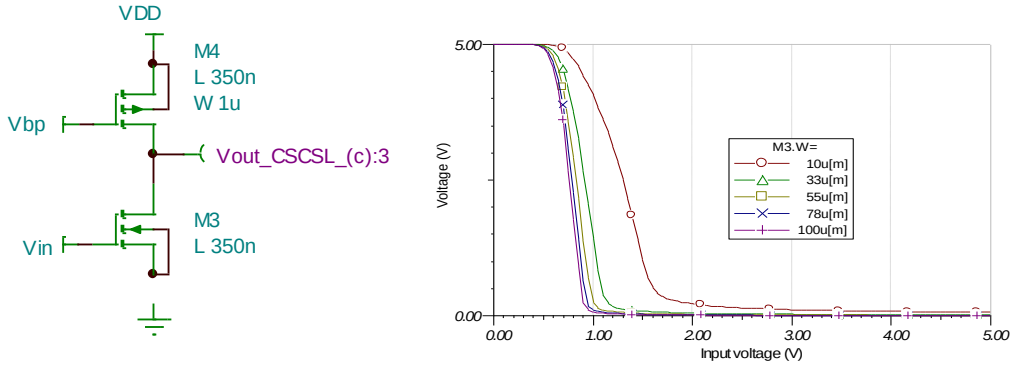


Figure 6.DC analysis for common-source stage with current-source load topology for various values of W_3. In all cases, $W_4=1\mu m$ and $V_{bp}=-2V$.

D. COMMON-SOURCE STAGE WITH ACTIVE LOAD

Figure 7 shows the DC analysis of the common-source stage with active load topology, for $W_6=5\mu m$ and various W_7. The $W_7=W_6=5\mu m$ is selected as the appropriate value for the following comparison of all stages.

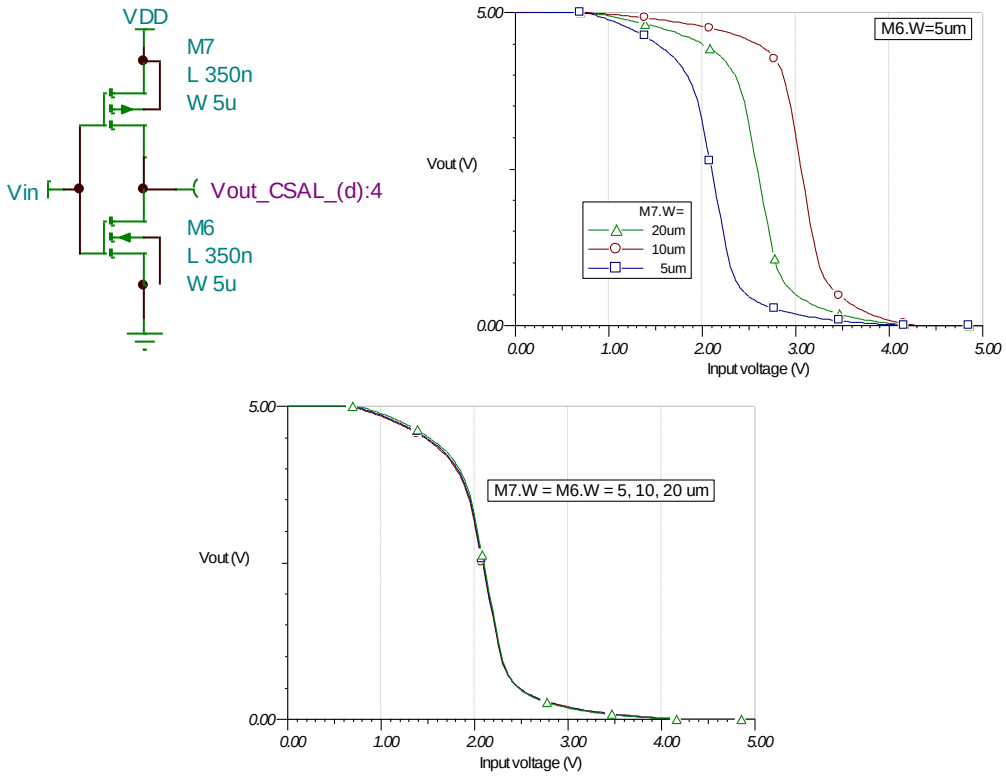


Figure 7. DC analysis for the common-source stage with active load for various W_7. In all cases $W_6=5\mu m$. The curve remains practically unaffected if $W_7=W_6$.

E. COMMON-SOURCE STAGE WITH TRIODE LOAD

Figure 8 shows the DC analysis for the common-source stage with triode load topology for various combinations of W_8 and W_9. The finally used values are the $W_8=5\mu m$and $W_9=1\mu m$. In all cases $V_{bp}=-2V$.

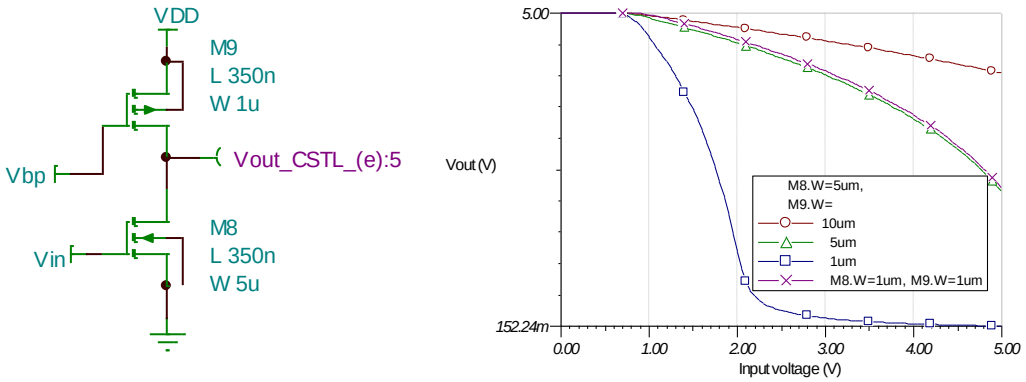


Figure 8. DC analysis of the common-source stage with triode load topology, for various values of W_8 and W_9. In all cases $V_{bp}=-2V$.

F. COMMON-SOURCE STAGE WITH SOURCE DEGENERATION

Figure 9 shows the various simulation scenarios with the common-source stage with source degeneration topology. Finally, $R_D=1kOhm$, $R_S=100Ohm$ and $W=60\mu m$are the appropriate values that are used in the all stage comparisons in the following section.

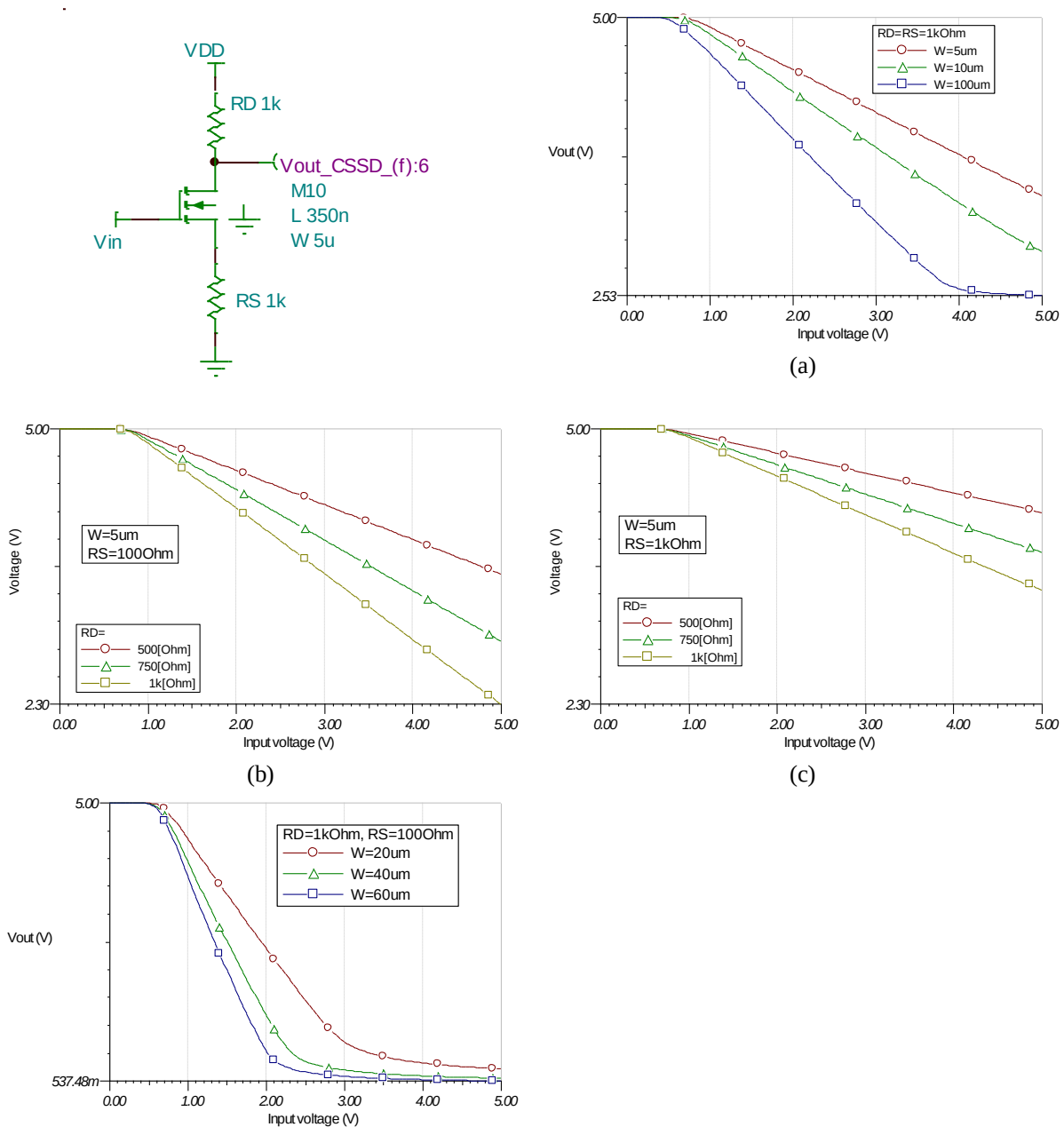


Figure 9. DC analysis of the common-source stage with source regeneration. (a) Testing various *W*s for $R_D=R_S=1kOhm$. (b) Testing various R_Ds for $W=5\mu m$and$R_S=100Ohm$. (c)Testing various R_Ds for W= 5µmand $R_S=1kOhm$. (d)Testing various *W*s for $R_D=1kOhm$ and $R_S=100Ohm$.

G. SOURCE-FOLLOWER

Figure 10 shows the DC analysis for the source-follower topology. The selected values are $R_S=100Ohm$ and $W=500\mu m$.

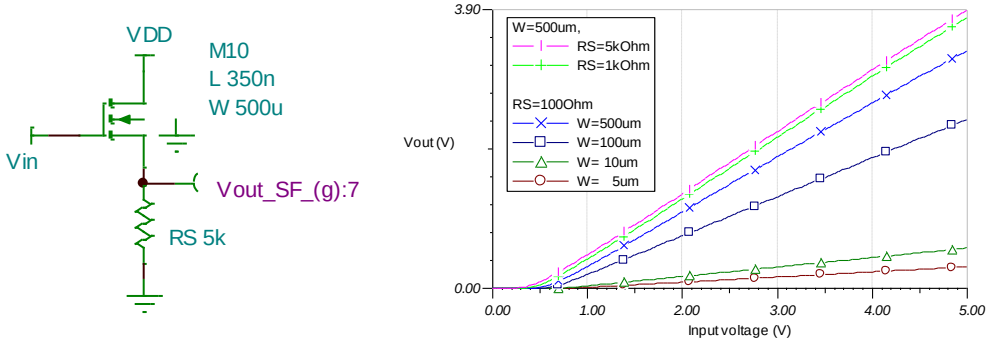


Figure 10.DC analysis of source-follower topology for $W=500\mu m$and various R_S values and for $R_S=100Ohm$ and various W values.

H. SOURCE-FOLLOWER WITH NMOS AS CURRENT SOURCE

Figure 11 shows the DC analysis for the source-follower with nMOS as current-source topology. The selected values $W_{13}=500\mu m$ and $W_{12}=1\mu m$.

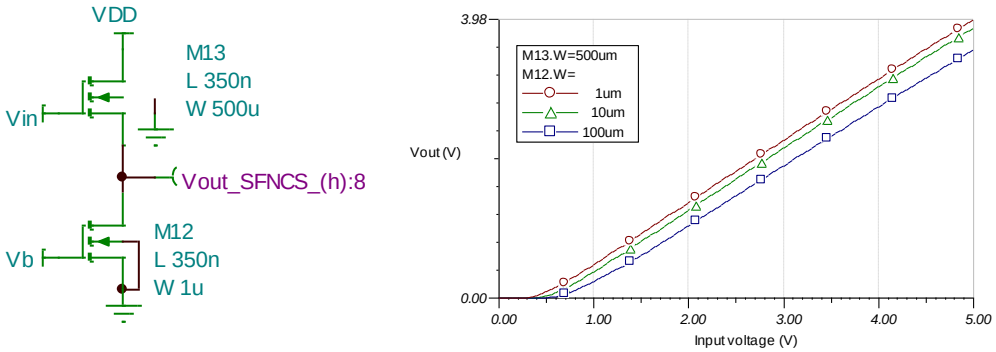


Figure 11.DC analysis of source-follower with nMOS as current-source topology for $W_{13}=500\mu m$, and various W_{12}. In all case $V_b=2V$.

I. COMMON-GATE STAGE

Figure 12 shows the DC analysis of the common-gate stage topology. Selected values are $W_{14}=100\mu m$and $R_D=10kOhm$.

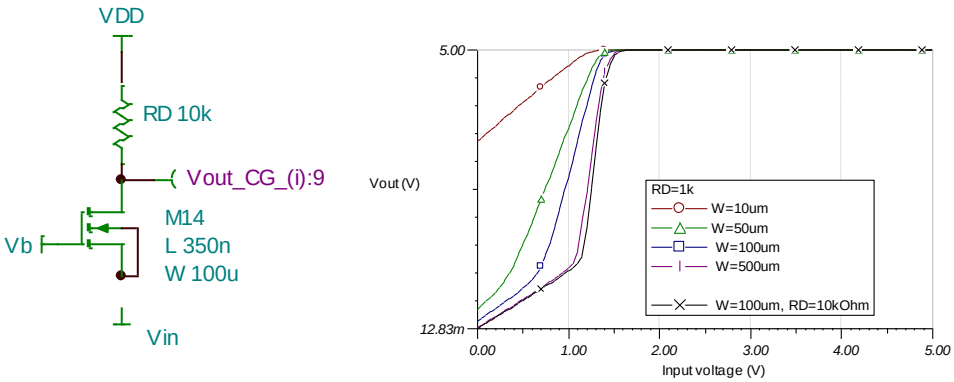


Figure 12.DC analysis of common-gate stage topology for $R_D=1kOhm$ and various Ws and then for $W_{14}=100\mu m$ and $R_D=10kOhm$.

J. CASCODE STAGE

Figure 13 shows the DC analysis of the cascode-stage topology and the appropriate values obtained after various simulations: $R_D=5kOhm$, $W_{16}=W_{15}=100\mu m$.

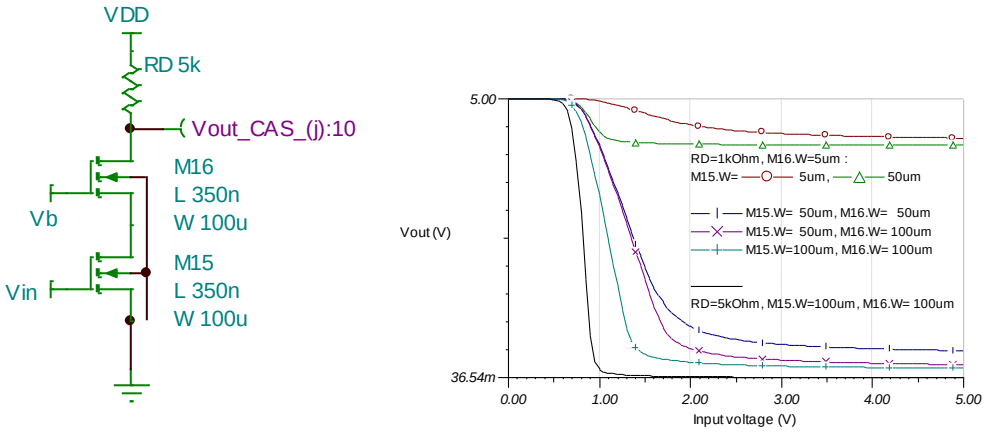


Figure 13.DC analysis of cascode-stage topology for various R_Ds, W_{15}s, W_{16}s.

K. SIMPLE FOLDED CASCODE STAGE

Figure 14 shows the DC analysis for the simple-cascode stage and the simple folded-cascode stage with nMOS input, for $R_D=1kOhm$, $W_{nMOS}=11\mu m$ and $W_{pMOS}=118\mu m$.

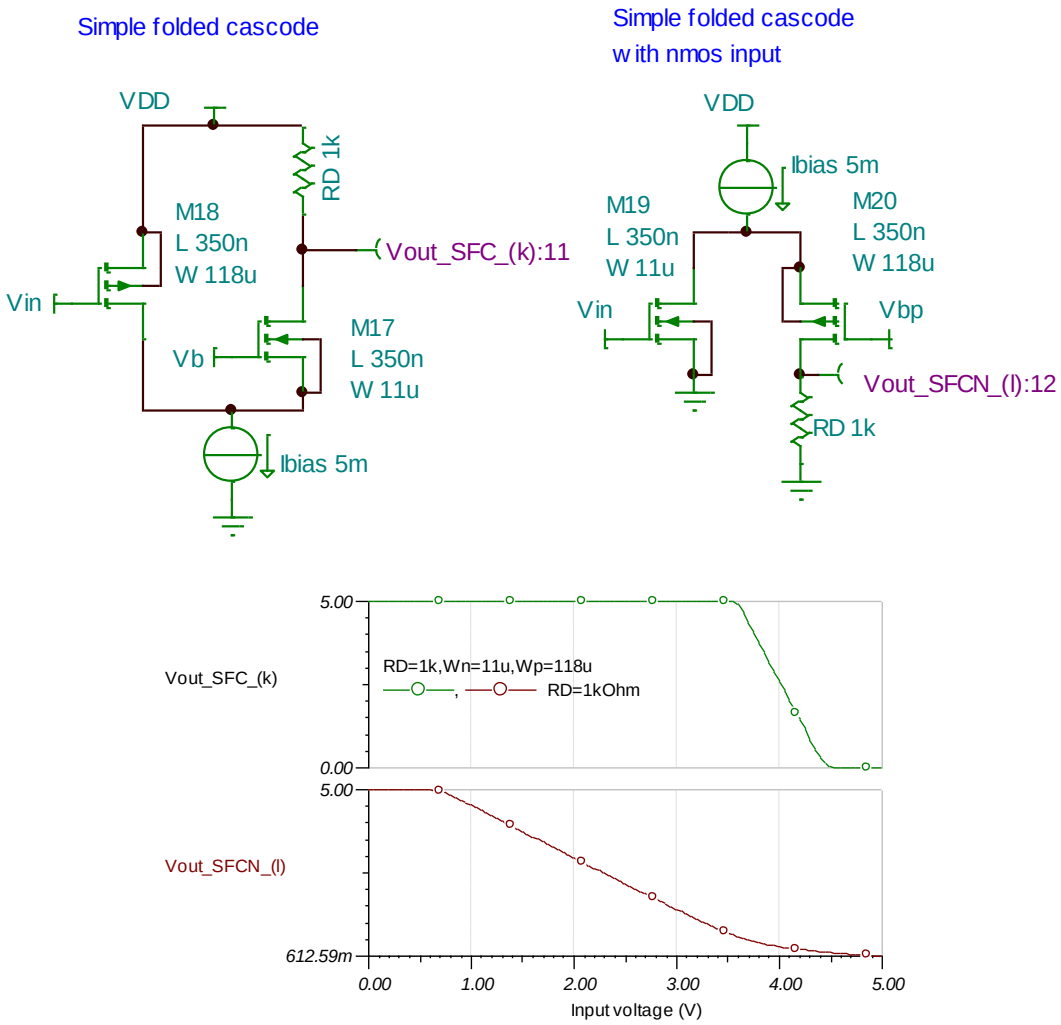


Figure 14. DC analysis for the simple-cascode stage and the simple folded-cascode stage with nMOS input, for $R_D=1kOhm$, $W_{nMOS}=W_{17}=W_{19}=11\mu m$ and $W_{pMOS}=W_{18}=W_{20}=118\mu m$.

IV. DC Comparison Of Standard Topologies

The DC V_{in}-V_{out} curves of the basic topologies (CS, CD, and CG) with the design values obtained from the previous section, are compared in Fig. 15. The appropriate device and bias values are seen the figure.

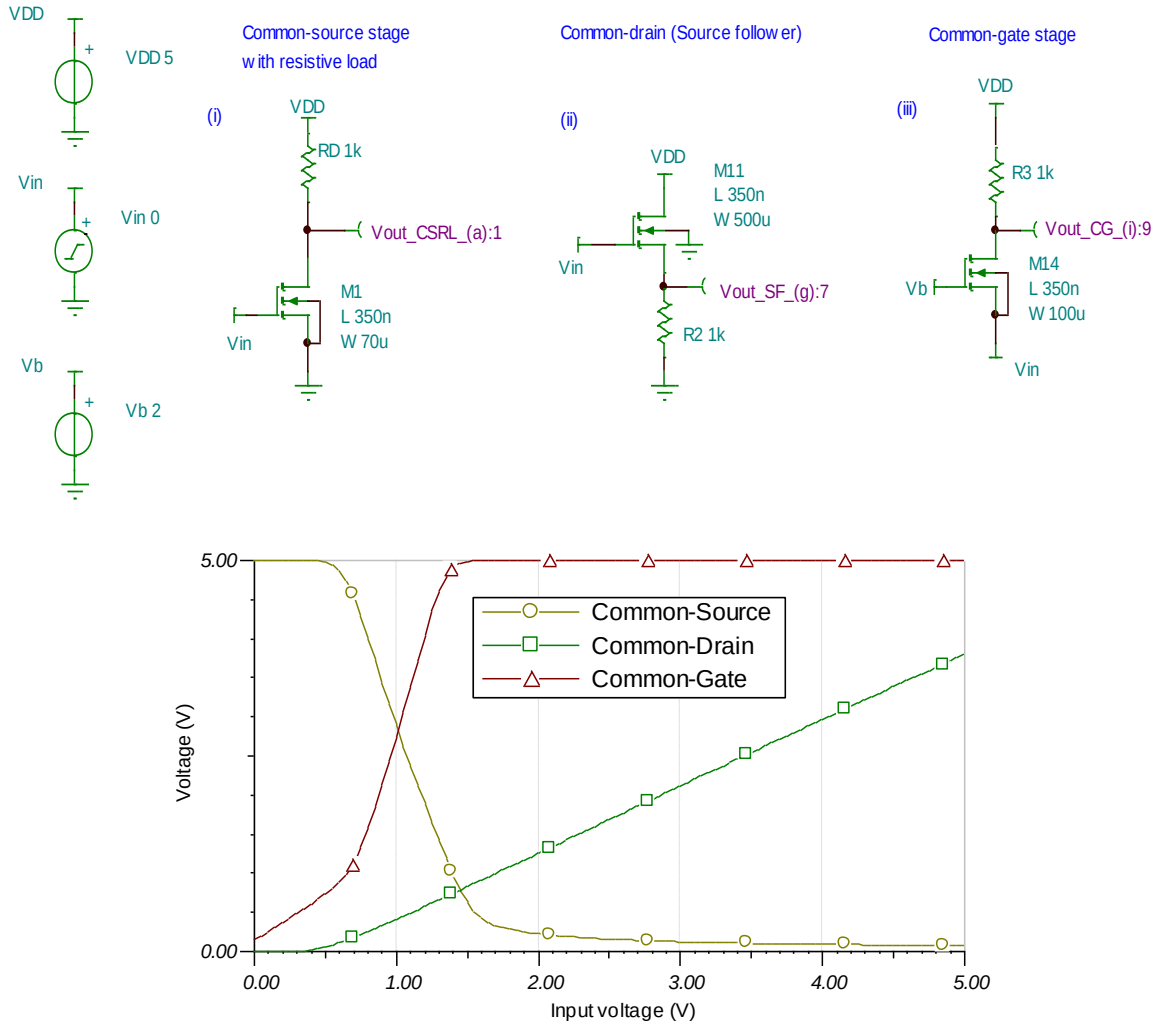


Figure 15. Common simulation of the three basic topologies: of the common-source, common-drain, and common-gate for the device parameters selected in the previous section.

V. DC Comparison Of Common-Source Topologies

Figure 16, shows the design for the simulation of all the CS topologies studied in the current work and their corresponding DC V_{in}-V_{out} curves. From each these curves, in Fig. 17, the appropriate DC bias voltage is determined along with the maximum allowed input-voltage swing and the corresponding amplification. Table 3 lists all the quantifiable results.

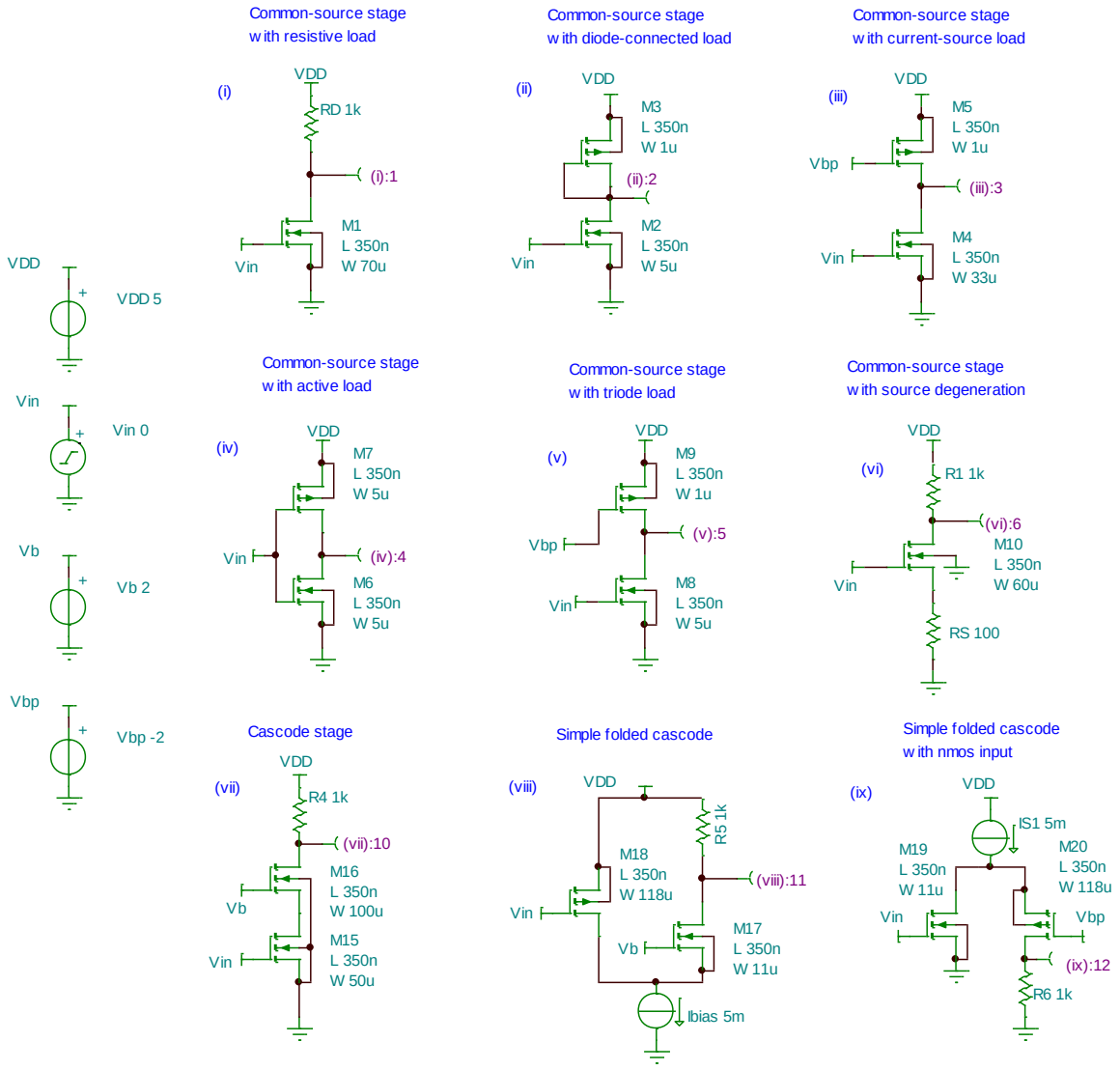


Figure 16.DC analysis of all the common-source topologies.

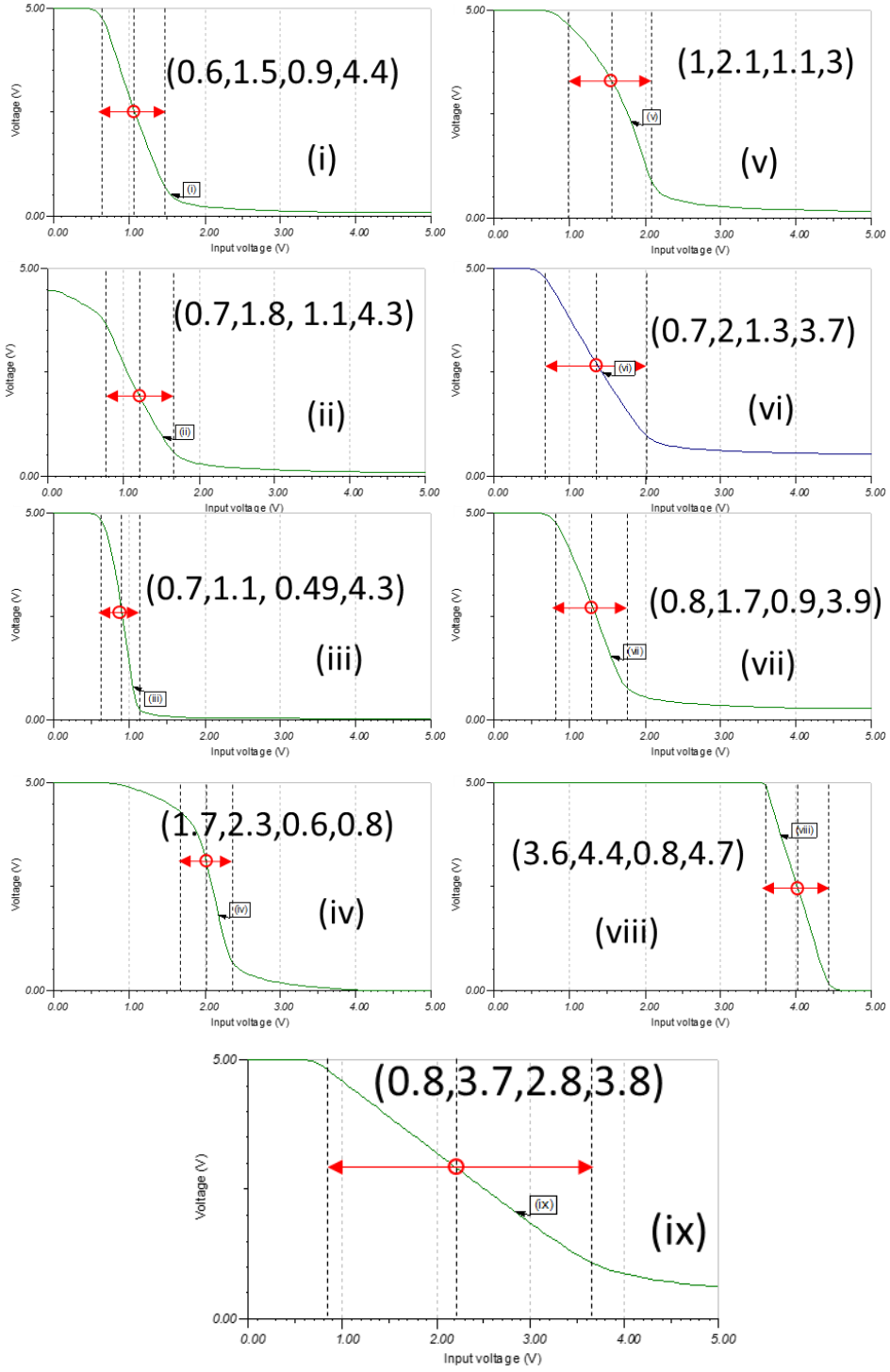


Figure 17. Quantification of $V_{in,bias}$ and gain $A_v=\Delta V_{out}/\Delta V_{in}$ in the saturation region of the IV-characteristics. The values in parenthesis are: (left voltage edge$V_{in,L}$, right voltage edge$V_{in,R}$, ΔV_{in}, ΔV_{out}).

Table3. Common-sourcetopology DC analysis results.

Topology	**(i)**	**(ii)**	**(iii)**	**(iv)**	**(v)**	**(vi)**	**(vii)**	**(viii)**	**(ix)**
$V_{in,L}(V)$	0.6	0.7	0.7	1.7	1.0	0.7	0.8	3.6	0.8
$V_{in,R}(V)$	1.5	1.8	1.1	2.3	2.1	2.0	1.7	4.4	3.7
$\Delta V_{in}(V)$	0.9	1.1	0.4	0.6	1.1	1.3	0.9	0.8	2.9
$V_{in,bias}(V)$	1.1	1.3	0.9	2.0	1.6	1.4	1.3	4.0	2.2
$\Delta V_{out}(V)$	4.4	4.3	4.3	0.8	3.0	3.7	3.9	4.7	3.8
A_v	4.9	3.9	10.8	1.3	2.7	2.9	4.3	5.7	1.3

VI. DC Comparison Of Common-Drain Topologies

Figure 18, shows the design for the simulation of all the CD topologies studied in the current work and their corresponding DC V_{in}-V_{out} curves. From each these curves, in Fig. 18, the appropriate DC bias voltage is determined along with the maximum allowed input-voltage swing and the corresponding amplification. Table 4 lists all the quantifiable results.

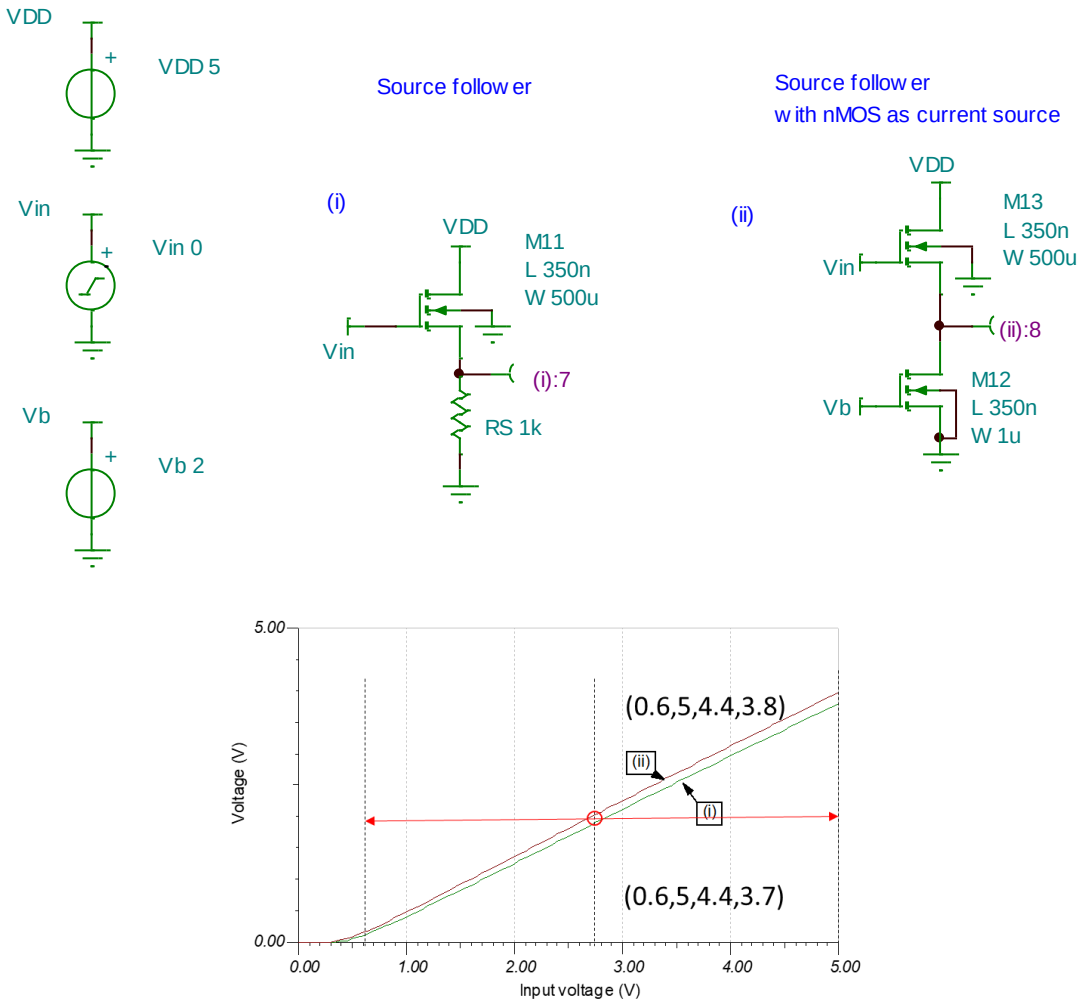


Figure 18.DC analysis of all the source-follower topologies and quantifications for maximum input voltage swing and amplification. The values in parenthesis are: (left voltage edge$V_{in,L}$, right voltage edge$V_{in,R}$,ΔV_{in}, ΔV_{out}).

Table4. Source-followertopology DC analysis results.

Topology	**(i)**	**(ii)**
$V_{in,L}$**(V)**	0.6	0.6
$V_{in,R}$**(V)**	5.4	5.4
ΔV_{in}**(V)**	4.4	4.4
$V_{in,bias}$**(V)**	2.8	2.8
ΔV_{out}**(V)**	3.7	3.8
A_v	0.8	0.9

VII. DC Results Of Common-Gate Topology

Finally, Fig. 19 shows the analysis of the CG DC for determination of maximum input voltage swing and amplification and Table 5 lists the analysis data.

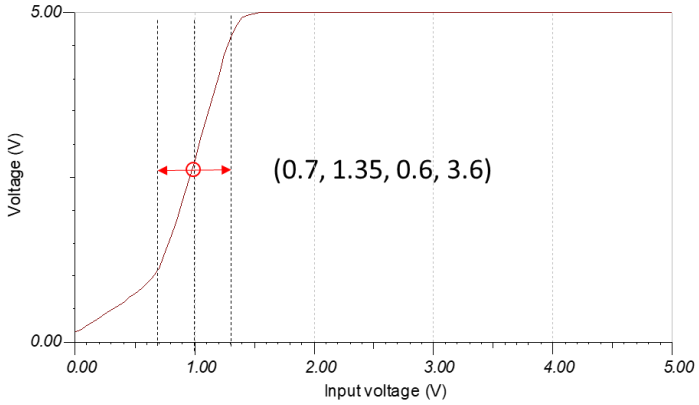


Figure 19. Analysis of common-gate DC curve for determination of maximum input voltage swing and amplification. The values in parenthesis are: (left voltage edge $V_{in,L}$, right voltage edge $V_{in,R}$,ΔV_{in}, ΔV_{out}).

Table5. Common-gatetopology DC analysis results.

Topology	**(i)**
$V_{in,L}$**(V)**	0.6
$V_{in,R}$**(V)**	1.4
ΔV_{in}**(V)**	0.6
$V_{in,bias}$**(V)**	0.9
ΔV_{out}**(V)**	3.6
A_v	6.0

VIII. Conclusions

The overall comparison is seen in Table 6. The interest is on the input voltage swing (ΔV_{in}) and on the amplification (A_v). Red color marks the lower value, and green the maximum value. Orange color marks intermediate "good" results, i.e., with both high input-voltage swing and amplification. The CS stage with current-source load has the highest amplification but the lower input-voltage swing, while the CD stage the maximum input voltage swing with the lowest amplification. Intermediate "good" choices are the CS stage with source degeneration and simple folded cascode stage with nMOS input. The results of the current analysis will be used in following works related to the design of more advanced circuits such as differential amplifiers, current sources and operational amplifiers.

Table 6. Overall comparison for determination of maximum input voltage swing and amplification.

		ΔV_{in}**(V)**	A_v
CS	**(i)**	0.9	4.9
	(ii)	1.1	3.9
	(iii)	0.4	10.8
	(iv)	0.6	1.3
	(v)	1.1	2.7
	(vi)	1.3	2.9
	(vii)	0.9	4.3
	(viii)	0.8	5.7
	(ix)	2.9	1.3
SF	**(i)**	4.4	0.8
	(ii)	4.4	0.9
CG	**(i)**	0.6	6.0

References

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