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Investigating the Effectiveness of Current Monitoring Methods to Detect Bridging and Stuck-Open Faults in CMOS Circuits

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Abstract: *In this paper, I_{DDQ} and I_{DDT} testing methods are analyzed for bridging and stuck-open (SOP) faults in complementary metal-oxide semiconductor (CMOS) circuits. Two test circuits (one digital and one analog) are chosen and faults are injected at particular locations. Simulation is carried out in 90 nm technology using the Cadence Virtuoso platform to observe the current waveforms and detect faults. With reference to the test circuits, simulation results show that the I_{DDQ} testing method is effective in detecting bridging fault for both digital and analog circuits, and SOP fault in analog circuits. On the other hand, the I_{DDT} testing method successfully detects only SOP faults in digital circuits.*

Keywords: *I_{DDQ}; I_{DDT}; bridging fault; stuck-open; CMOS*

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I. Introduction

Recent development in CMOS nanometer technology has increased the number of defects in ICs and introduced new defects which are difficult to be detected through conventional testing methods [1]. Current monitoring is an alternate testing technique for low cost and high speed testing process [2]. Current monitoring based testing has proved effective for bridging, transistor stuck-on (TSON) and stuck-open (SOP) faults in digital and analog CMOS circuits [3,4].

The quiescent power supply current, I_{DDQ} testing has become a popular test method since it was proposed [5,6]. A CMOS circuit consumes negligible current at standby mode, but at the present of any short faults, this current increases significantly as a path is completed from supply to ground. However, the efficiency of I_{DDQ} testing is decreasing due to the increased leakage current for submicron and nanometer feature sizes, long wait time for steady current, and increased area and power requirement for current sensing equipment [7]. Moreover, I_{DDQ} testing is ineffective for SOP fault as it does not lead to increased quiescent current [8]. As a result, the I_{DDT} testing was proposed to increase the effectiveness of fault detection [9,10]. The transient power supply current, I_{DDT} testing monitors the instantaneous current during the switching stage in CMOS circuits. The presence of a fault can be indicated by different parameters of the dynamic current waveform such as the maximum/minimum peaks and the width or delay [11]. The transient current curve of a CMOS inverter is shown in Fig. 1 for 2 different input frequencies. Open defects usually cause a slow rise in node voltage which consequently causes a delay in the transient current.

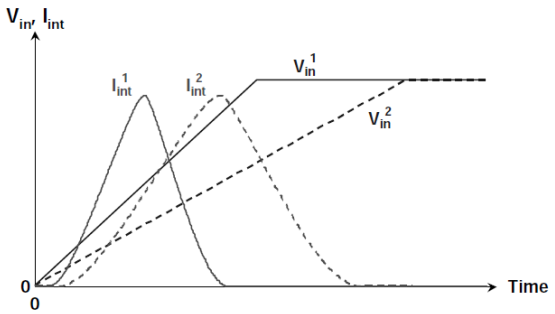


Figure no. 1: Transient current curve of a CMOS inverter

Several works in literature have analyzed the effectiveness of I_{DDQ} and I_{DDT} testing in digital circuits for TSON/bridging faults and SOP faults, respectively [3,8,12,13]. However, only a few works have analyzed on analog circuits for such cases [11,14].In this paper, we analyze the effectiveness of I_{DDQ} and I_{DDT} testing in digital and analog circuits for detecting bridging and SOP faults. A circuit under test (CUT) is selected for both

cases. The faults are inserted and output currents are simulated using Cadence Virtuoso in 90 nm technology. The paper is organized as follows: section 2 briefly describes the test methodology, section 3 presents the CUTs and discusses the fault conditions, section 4 presents the simulation results and performance analysis. Finally, section 5 concludes the paper.

II. Test Methodology

The overall test methodology to determine the effectiveness of the two test techniques for digital and analog circuits is briefly presented as a flow chart in Fig. 2. At first, the fault types are selected and inserted at a certain position of the circuit. The two fault types analyzed in the circuits are bridging and SOP faults. The corresponding input combination is applied which will cause two different current values for fault-free and faulty cases. This input combination is called the test vector (TV). The testing method (I_{DDQ}/I_{DDT}) is then selected to observe the change in current waveforms and determine whether the faults have been detected effectively.

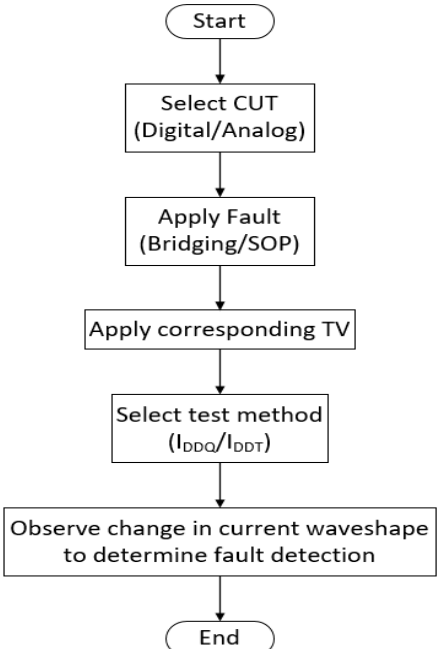


Figure no. 2: Test Methodology

Bridging Fault:

A bridging or short fault occurs when two terminals in a circuit are shorted. It can occur at the inter-gate or intra-gate level of ICs. Bridging fault occurring between the drain and source terminals of a transistor are also called TSON fault. An example of a bridging fault between the outputs of two different NOR gates is shown in Fig. 3.

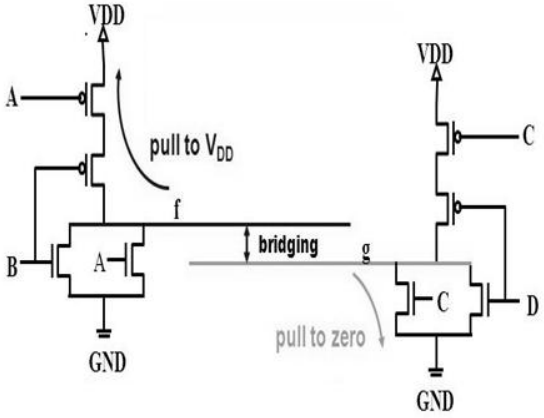


Figure no. 3: Bridging fault

Stuck-Open Fault:

A SOP fault creates a high impedance between two points in a circuit which allows negligible or no current flow. At transistor level, a SOP fault means that the transistor never conducts any current. Testing of a SOP fault requires a two pattern test, where the output is first set at a logic level through the initialization vector (IV) and then the TV is applied to propagate the fault to the output node. An example of a transistor SOP fault is shown in Fig. 4, where transistor P_1 is SOP and disconnects a connection between V_{DD} and source of P_2. First, the IV <10> is applied to set the output at logic 0. In the next step, the TV <00> is applied which will result to an output logic 1 for fault-free, but an indeterminate logic or floating node during faulty case. Therefore, it becomes difficult for SOP faults to be detected by logic level.

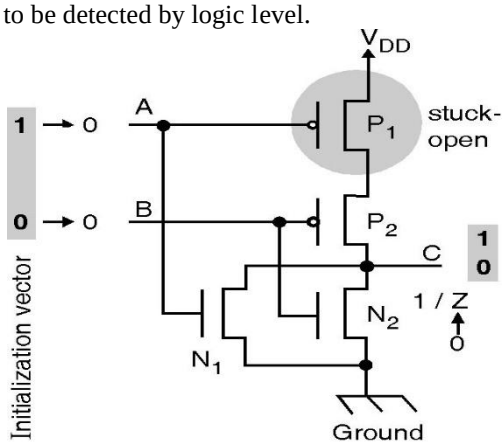


Figure no. 4: Stuck-open fault

Test Circuits:

The digital combinational circuit selected for the analysis is based on the following Boolean functions given by equations (1-3). The overall test circuit with fault locations is shown in Fig. 5 which consists of an inverter and two NAND gates. The current I_{DDQ} in the circuit is the steady-state current for a fixed input combination and the current I_{DDT} is the transient current during switching state between any two consecutive input combinations.

$$f_3 = \overline{f_1 f_2} \quad (1)$$

$$f_1 = \overline{x_1} \quad (2)$$

$$f_2 = \overline{x_1 x_2} \quad (3)$$

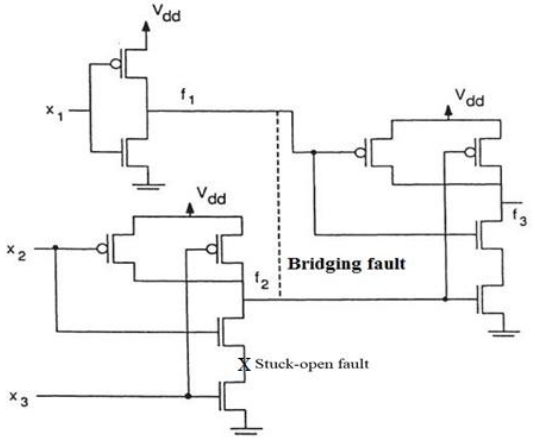


Figure no. 5: Digital CUT

The analog circuit chosen for the analysis is a basic single stage CMOS operational amplifier which is operated as a comparator. The SOP and bridging fault locations are shown in Fig. 6. The I_{DDQ} current in an amplifier circuit is the steady-stage sinusoidal current which flows during the normal amplifying operation of the circuit. The I_{DDT} current in the circuit is defined as the transient current which occurs when the inputs V+ or V- are switched on.

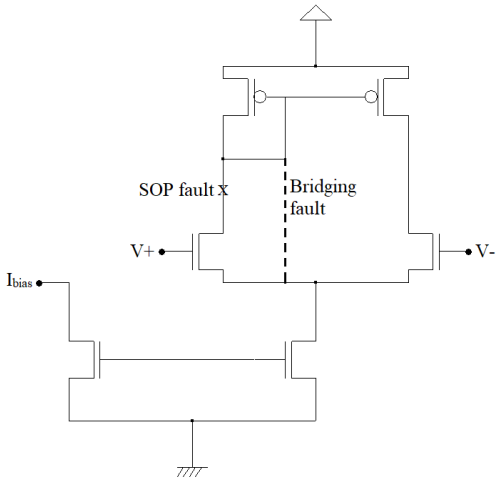


Figure no. 6: Analog CUT

III. Simulation Results and Discussions

The simulation of the circuits are carried out in 90 nm technology using Cadence Virtuoso platform. The supply voltage is 1.2V and the width of all transistors are 120 nm for both circuits.The digital circuit is first analyzed. Figure 7 shows the input signals and fault-free output voltage of the digital CUT. The bridging fault is applied as shown in Fig. 5 and the output voltage and current are observed. For the fault to propagate to the output logic, the outputs f_1 and f_2 should be different i.e. if f_1 = 1, then f_2 = 0 and vice-versa. The corresponding input combinations required and the resultant output voltage for fault-free and faulty cases are shown in Table 1. During the fault, the shorted f_1-f_2 node holds an intermediate voltage level below 0.5V for all TVs and is interpreted as logic 0 by the second NAND gate. Therefore, the output logic is same for both fault-free and faulty cases and the fault remains undetected through the voltage method.

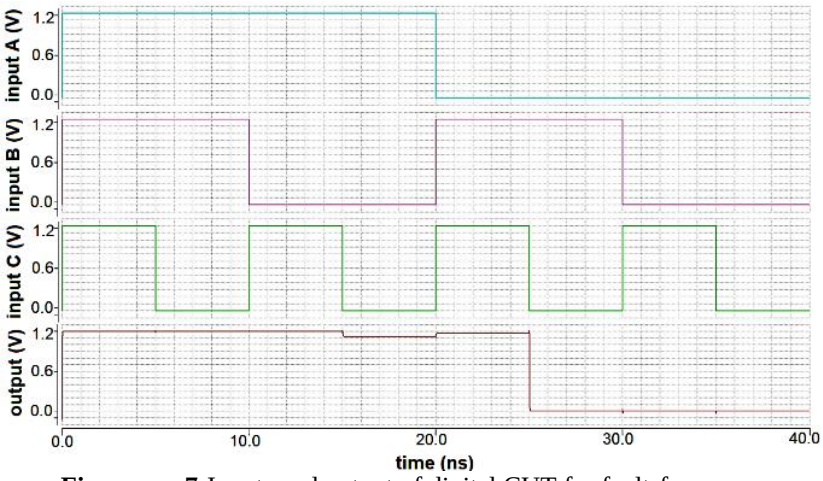
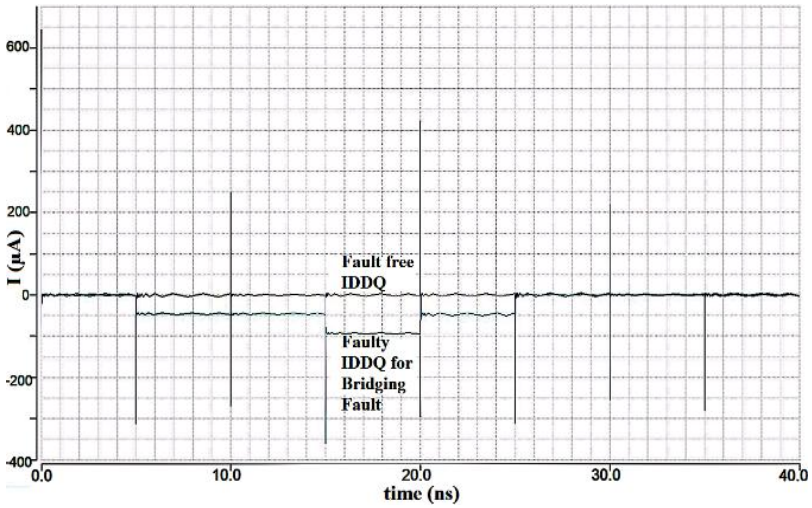


Figure no. 7: Inputs and output of digital CUT for fault-free case

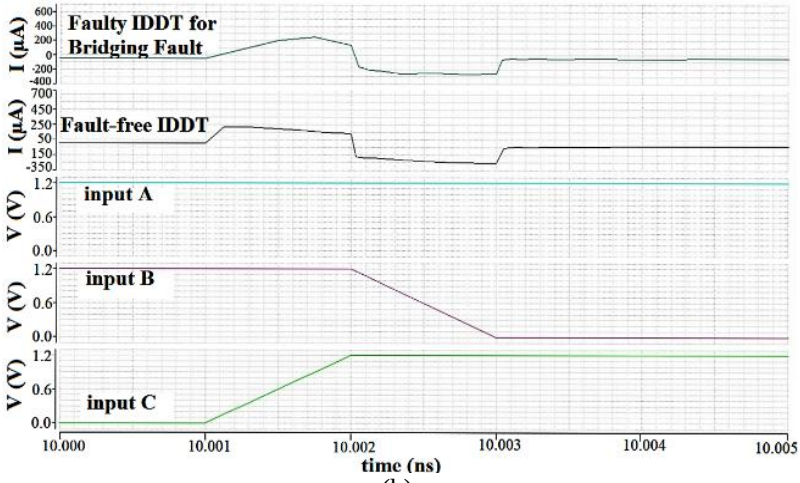
Table no 1: Test vectors and corresponding output logic for bridging fault

Intermediate node		Inputs			Outputs	
F_1	F_2	X_1	X_2	X_3	Fault-free	Faulty
0	1	1	0	0	1	1
		1	0	1	1	1
		1	1	0	1	1
1	0	0	1	1	1	1

The I_{DDQ} and I_{DDT} current curves for fault-free and faulty cases are shown in Fig. 8. The I_{DDQ} curve clearly indicates the presence of a fault by the increased magnitude in the quiescent current level for the faulty state compared to the fault-free state. For the I_{DDT} testing method, although the fault can be detected from the decreased slope of the transient current during the input switching, the fault-free and faulty I_{DDT} current curves are difficult to compare.



(a)



(b)

Figure no. 8: (a) I_{DDQ} and (b) I_{DDT} current curves for the digital CUT with bridging fault

After the circuit is tested for bridging fault, the SOP fault is injected and the IV $<x_1\ x_2\ x_3>$= <010> is applied for the two pattern test. This input combination sets the nodes f1 and f2 at logic 1 and the output at logic 0. The TV $<x_1\ x_2\ x_3>$= <011> is then applied to propagate the fault which will result to an output logic of 1 for fault-free case and 0 for faulty case. The voltage and I_{DDT} current outputs in Fig. 9 and 10 shows that the SOP fault can be successfully detected from both logic and current testing methods. The I_{DDT} testing method indicates the fault by a delayed rise of the transient current during the switching state. Since there is no significant change in quiescent current for a SOP fault, the I_{DDQ} testing method is ineffective for SOP fault detection in digital circuits.

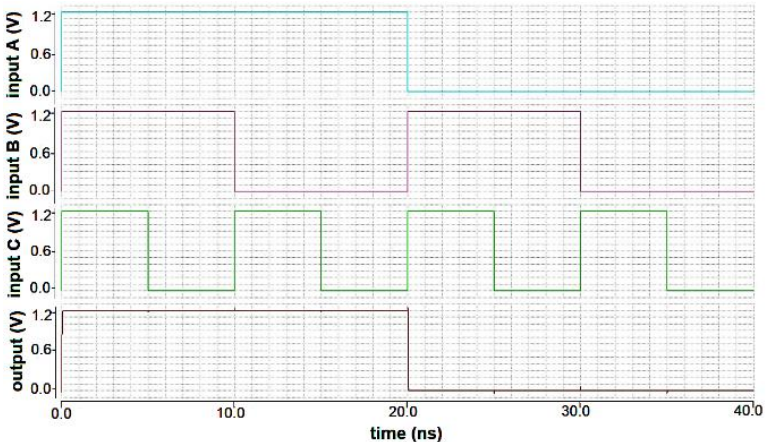


Figure no. 9: Faulty output voltage of the digital CUT for SOP fault

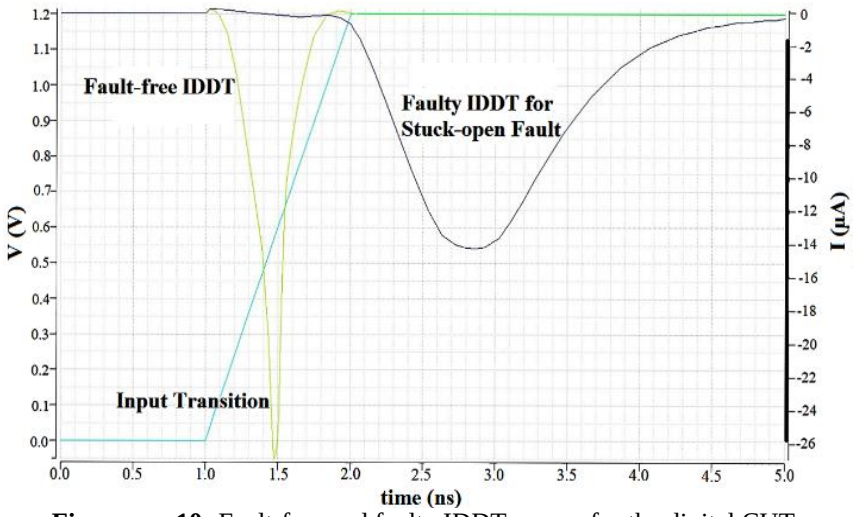
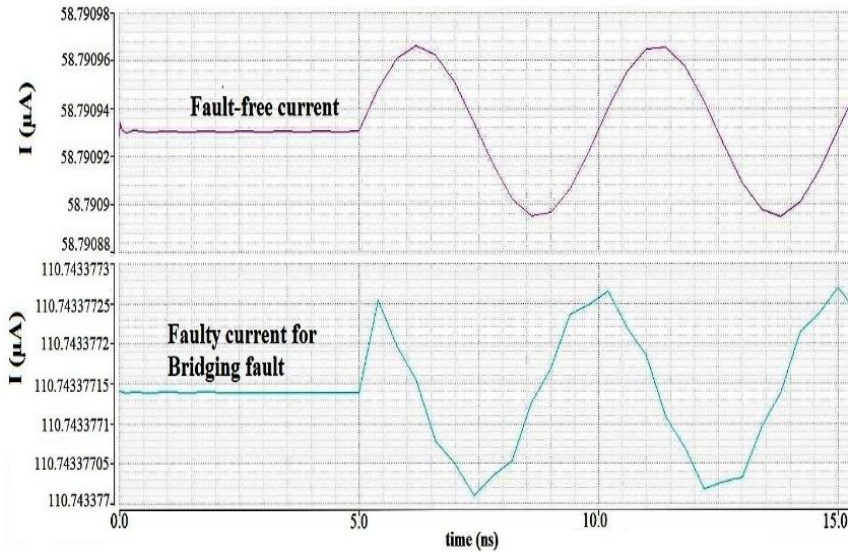
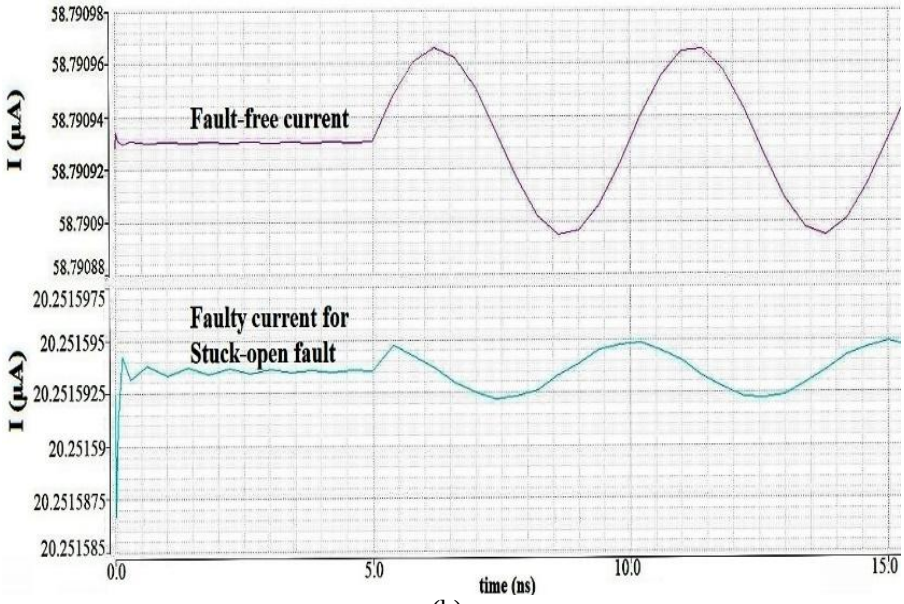


Figure no. 10: Fault-free and faulty IDDT curves for the digital CUT

Next, the effectiveness of the two methods in analog circuits for the two fault types are analyzed with a CMOS operational amplifier. Both faults are individually applied and the instantaneous current curves are observed. Two input signals of 200 MHz with different amplitudes at V+ and V- are applied after a certain time to observe both I_{DDQ} and I_{DDT} currents in the circuit. Figure 11 shows the current curves of the amplifier for both faults. It can be observed that for both types of fault, the overall DC offset value of the sinusoidal steady-state current changes. For a bridging fault, the quiescent current increases, whereas it decreases for a SOP fault. The peak-peak amplitude of the current also decreases significantly for the SOP fault. Therefore, it can be concluded that the IDDQ testing method successfully detects both faults in the amplifier. However, the transient switching currents when the inputs are applied, for both fault-free and faulty cases, cannot be differentiated to effectively identify the presence of a fault. This indicates that the IDDT testing method is ineffective for bridging or SOP fault detections in analog circuits.



(a)



(b)

Figure no. 11: Current curves of analog CUT for (a) bridging and (b) SOP faults

IV. Conclusions

In this paper, the effectiveness of I_{DDQ} and I_{DDT} testing has been studied to detect bridging and SOP faults in CMOS digital and analog circuits. Results show that in the digital CUT, the bridging fault can be clearly detected by I_{DDQ} testing as the current waveform shows an increase in magnitude. Although the I_{DDT} waveform also shows a decrease in the slope for a bridging fault, it is not very decisive to detect the fault. For an SOP fault, I_{DDT} testing affirms the presence of the fault by a delay in the waveform. However, I_{DDQ} testing is not effective in this case as there is no significant change in steady-state current. In the case of the analog CUT, I_{DDQ} testing effectively detects both types of faults mentioned by observing changes in the magnitude of the sinusoidal steady-state current; increases for bridging fault and decreases for an SOP fault. The I_{DDT} testing method proves to be ineffective in the analog CUT to detect faults as the transient switching currents for both fault-free and faulty cases cannot be differentiated.

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