Design and Analysis of Johnson Counter Using Finfet Technology

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Abstract : *Conventional CMOS technology's performance deteriorates due to increased short channel effects. Double-gate (DG) FinFETs has better short channel effects performance compared to the conventional CMOS and stimulates technology scaling. The main drawback of using CMOS transistors are high power consumption and high leakage current. Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS in nano- scale circuits.FinFET, which is a double-gate field effect transistor (DGFET), is more versatile than traditional single-gate field effect transistors because it has two gates that can be controlled independently. Usually, the second gate of FinFET transistors is used to dynamically control the threshold voltage of the first gate in order to improve the performance and reduce leakage power. In this paper, we proposes a synchronous johnson counter by using FinFET Technology.FinFET logic implementation has significant advantages over static CMOS logic in terms of power consumption. The proposed counter was fabricated in 16nm FinFET technology in HSPICE.*
Keywords – *CMOS, Scaling, FinFET, Low Power Design, SET*

I.   Introduction

Steady miniaturization of transistors with each new generation of bulk CMOS technology has yielded continual improvement in the performance of digital circuits.In the case of non portable devices, power consumption is also very important because of the increased in packaging density and cooling costs as well as potential reliability problems. Thus, power efficiency has increased importance, to meet the performance requirements of VLSI.The scaling of bulk CMOS, in fact faces significant challenges in the future due to fundamental material and process technology limits [1].Short channel effects such as sub-threshold and gate-dielectric leakages in conventional CMOS devices are primary limiters for scaling. Novel device architectures are therefore, necessary to continue reaping the benefits of scaling to very short gate lengths beyond 10nm. Double-gate CMOS (DGCMOS) devices offer an attractive alternative to other structures such as ultra-thin body (UTB) or conventional bulk CMOS in terms of performance and control of short-channel effects.

The emergence of FinFET provides a promising solution. FinFET, a double-gate device in which a second gate is added opposite to the traditional (first) gate, has long been recognized for its potential to better control short-channel effects.The additional back gate of FinFETs gives circuit designers many options. It can serve as a secondary gate that enhances the performance of the front (first) gate. For example, if the front gate voltage is VDD (transistor is ON) the back gate can be biased to VDD to provide bigger current drive, which reduces transistor delay. If the front gate voltage is 0 (transistor is OFF), the back gate can be biased to 0, which raises the threshold voltage of the front gate and reduces the leakage current. This can be achieved by simply tying the front gate and the back gate together[3]. Fin-FETs are predicted as one of the best possible candidates to replace the bulk MOSFETs beyond 32nm regime due to their improved subthreshold slope, reduced leakage current, better short-channel performance, and Compatible process flow with existing CMOS technologies.It has been shown that such a device has a very high potential for analog applications due to its high value of early voltage and, hence, a large intrinsic gain [4].

II.   FinFET Structure

Double-gate devices have been used in a variety of innovative ways in digital and analog circuit designs. DG devices with independent gates (separate contacts to back and front gates) have been recently developed. In the context of digital logic design, the ability to independently control the two gates of a DG-FET has been utilized chiefly in two ways: by merging pairs of parallel transistors to reduce circuit area and capacitance, and the next way through the use of a back-gate voltage bias to modulate transistor threshold voltage. A parallel transistor pair consists of two transistors with their source and drain terminals tied together. In Double-gate (DG) FinFETs, the second gate is added opposite the traditional (first) gate, which have been recognized for their potential to better control short-channel effects (SCEs) and as well as to control leakage current.The structure of the FinFET is shown in the Fig.1.
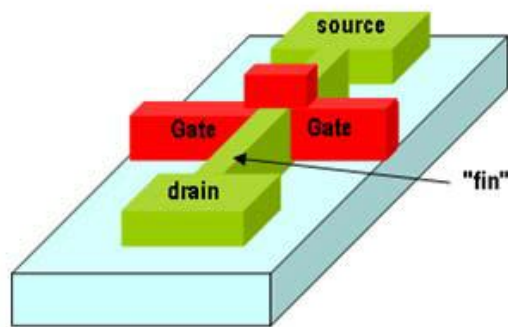
Fig 1.FINFET Structure

The two gates for FinFETs provide effective control of the short-channel effects without aggressively scaling down the gate-oxide thickness and increasing the channel doping density. The separate biasing in DG device easily provides multiple threshold voltages. It can also be exploited to reduce the number of transistors for implementing logic functions [5].
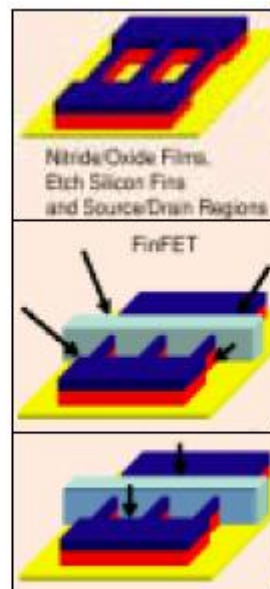

Fig 2. FinFET manufacturing process flow

1.1 Process Flow
   The process flow is summarized in Figure 2. It involves the following basic steps: (i) Etching of Si fins out of the silicon layer of an SOI wafer, (ii) Gate formation around the fin, forming the front and back gates and (iii) spacer formation followed by S/D implantation. As we can see from Figure 1, the height of the silicon fin defines the transistor width. The thickness of the fin,on the other hand, defines the control of the back gate on the channel and hence the short channel behavior of the device.Silicon films on SOI wafers are used to define the fins and hence,the height of the fin is effectively constant for all transistors [2].

1.2 Device-Width Quantization
   Each fin provides 2H of device width, where H is the height of the fin. The size of each fin also determines the increments in device widths available to the circuit designer. In planar devices, the device width quanta are dictated by the grid step size in the design database employed. This relatively unconstrained selection of device width allows designers to choose appropriate ratios of N-MOSFET and P-MOSFETdevices to achieve desired tradeoffs in performance, power, and robustness. Owing to the quantization constraint, it is much more difficult to achieve the required beta ratios in FinFETs [2].

III.   SET D Flip flop

The proposed SET D flip-flop is illustrated in figure 3. When the clock is high, CLK signal is at logic level high and CLKB is at logic level low. In this state, the Master latch consisting of one pass transistor PT1 and inverter I1 is functional and the inverse of data at input D is stored to an intermediate node. When the clock is at logic level low, CLK signal is at logic level low and CLKB is at logic level high. In this state, the Slave latch consisting of pass transistor PT2 and a regenerative feedback loop consists of one pass transistor PT3 becomes functional and produces Q and QB after two inversions.The flip-flop as shown above in figure 3 is a negative edge triggered SETFF.
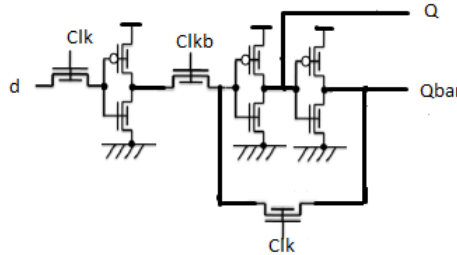

Fig 3.SG-FINFET SET D Flip flop implementation

The regenerative feedback loop that used in the design advantageously serves as even if the clock is stopped (permanently grounded) the proposed circuit is able to maintain the logic levels at Q and QB which proves the fact that the proposed SET is static in nature. The main advantage of the circuit is the reduced transistor count, which is only nine that is less than existing flip flop.So power is also reduced merely. Hence, it can be used to increase the chip density while maintaining a lower manufacturing cost at the same time. Moreover, the circuit can be made to function dynamically by merely removing the pass transistor from the regenerative feedback loop of the proposed design with only eight transistors. Since, we have used only N type FINFET transistors in the forward path, the design can be suitably used for high frequency applications and is easily portable to lower technologies.

IV.   Design of Johnson Counter

Counters are usually suffer problem of power consumption because they are designed with conventional D,T or JK flip flops. They are not only increase power consumption but also design complexity is more. By choosing the flip flop with low power consumption makes the design power efficient. The johnson counter consists of four stages of cascaded D registers. The D register design has been implemented using CMOS inverter and two D latch with one clock and one input. Since it is synchronous counter clock input is applied to all flip flops simultaneously. A Johnson counter or switch tail ring counter, is a counter, where the inverted output from the last flip flop is fed back as an input to the first flip flop. Johnson counter, whose sequence length is equal to twice the length of the d flip flops in the counter. These counters find different applications like decoding, phase waveform generation etc. They can be implemented easily using D- or JK-type flip-flops. The 4 bit synchronous Johnson counter i.e shown in figure 2 is designed by using four SET D flip flops represented in figure 1 and figure 2.
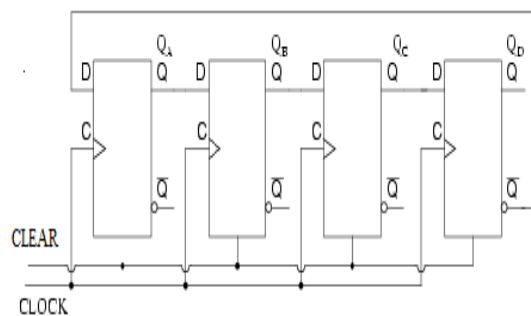

Fig 4.Johnson counter

In this counter, inversion of Q is fed back to input D causes the counter to "count" in a different way. Generally 4-bit Johnson counter passes four logic 0s and then four logic 1s thereby producing an 8-bit sequence pattern i.e., 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000 and this is shown in the following table1 below.

Table1. Truth Table for a 4-bit Johnson Counter

Clock Pulse No	FFA	FFB	FFC	FFD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

To enable the counter according to desired Sequence shown in table 1, first it is necessary to clear all the flipflops.Initially QD is '0 and QDbar is '1'.The first clock shifts three 0s from (QA QB QC) to the right into (QB QC QD).After three clock pulses we have all 1s.So the output of last flip flop i.e QD is '1' and QDbar is '0'.Thus we start shifting 1s to that right, replacing the zeros. Because of implementing the Johnson counter with proposed SET D Flip flop the power consumption is substantially reduced, the comparison results shown in section V.

V. Simulation Results

The design is implemented using HSPICE and the circuits are simulated using 16nm technology. The waveform of the SET DFF and Johnson counter using SET DFF are shown in fig 5 and fig 6.
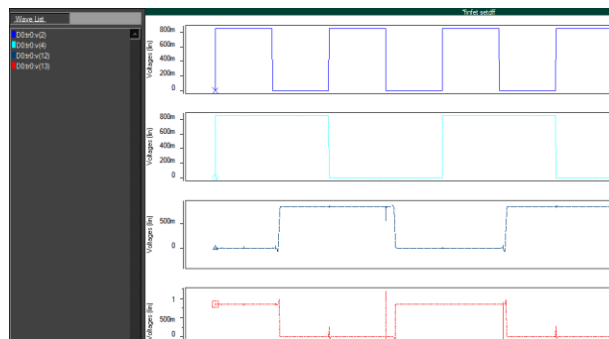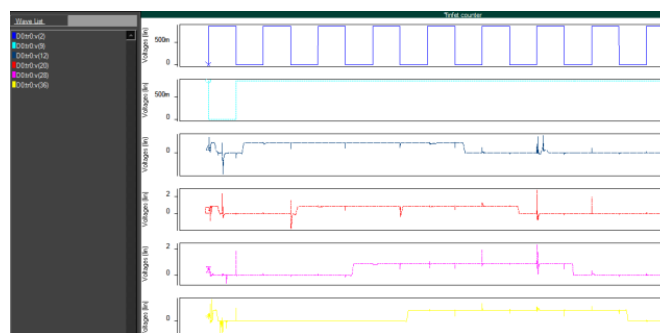

Fig 5. SG-Finfet SET D Flip flop

Fig 6.Johnson counter

Table 2.Comparison Table

Design	Parameters		No of Transistors	Avg Power (μW)
	Operating Frequency	Operating Voltage		
Flip flop	500MHz	0.85V	9	0.065
Counter	500MHz	0.85V	60	0.201

VI.   Conclusion

This paper concludes that synchronous Johnson counter is implemented by FINFET 16nm technology using HSPICE . FinFET not only has superior performance over bulk silicon MOSFET, but also it is novel technology over bulk silicon MOSFET as the dominant transistor choice for sub micron technology. FinFET is equivalent to two MOSFETs operating in parallel. FinFET logic circuits achieve significant area and power reduction without transistor scaling.

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