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Optimized Routing Methods for VLSI Placement Design

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Abstract: *The VLSI placement problem is to place the objects into fixed die such that there are no overlaps among the objects and some cost metric such as wire length and routability is optimized. For this purpose A new routing method is used - called , A Deep sub-wavelength lithography, (using the 193nm lithography to print 45nm, 32nm, and possibly 22nm integrated circuits), is one of the most fundamental limitations for the continuous VLSI scaling,. Lithography printability is strongly layout dependent, thus routing plays an important role in addressing the overall circuit manufacturability and product yield since it is the last major physical design step before tape out. This paper will discuss some recent advancement of lithography friendly routing from post-routing hotspot fixing (construct by- correction) to during-routing hotspot avoidance (correct-by construction) guided by various lithography metrics.*

Keywords: *cost metric, hotspot avoidance , hotspot fixing, LFR routing, routing congestion, subwavelength lithography*

I. Introduction

Nanometer VLSI design is facing increasing challenges from manufacturing limitations. These include the printability issues due to sub-wavelength lithography, the topography variations due to chemical-mechanical polishing (CMP) , the random defects due to missing/extra material , the via failure , and so on. Among these, lithography is one of the most critical challenges in advanced technology nodes.

A fundamental limitation for the *sub-wavelength optical lithography* is WYSINWYG, i.e., "what you see (at design) is not what you get (at fab)". The printability issue arises between neighboring wires/vias due to sub-wavelength effects and process variations. As of now, the 193nm (wavelength) optical lithography is still the dominant integrated circuit (IC) manufacturing process for 65nm and 45nm nodes, and next generation lithographies (e.g., EUV lithography, 157nm wavelength lithography, e-beam direct write, nanoimprint, and so on) are not yet in the mainstream in the near future. Accordingly, major IC manufacturers are expected to continue to use 193nm lithography to print 32nm features, heavily relying on resolution enhancement techniques (RET) such as optical proximity correction (OPC), immersion lithography, and probably double patterning.

OPC which modifies GDSII for better printability as a post tape out mask synthesis is a crucial step in manufacturing, but at a cost of high computational complexity as well as mask cost overhead. Nevertheless, OPC may be too late to make all the necessary corrections due to restricted design flexibility. If the initial design is very lithography unfriendly, even aggressive RET may not be able to solve the printability problem. These limitations demand more lithography friendly design such that the downstream lithography and OPC effects can be abstracted and estimated for better design decisions in terms of manufacturability.

As a result, there are many manufacturability aware efforts in earlier design stages such as logic synthesis, placement, and routing . Routing is a critical physical design stage to address the lithography issues as: **(a)** lower routing layers for sub-65nm designs pose tremendous lithography/printability challenges due to wrong-way routing (jogs), complex pin access, etc. **(b)** routing is the last major VLSI physical design step before manufacturing, thus has more comprehensive and accurate layout information for printability estimation, **(c)** routing still has considerable design flexibility to find reasonable tradeoff between printability and conventional design objectives (e.g., timing, noise, power). These factors lead to a lot of recent academic and industrial efforts in *lithography friendly routing* or LFR, especially detailed routing due to small influence window of optical lithography (e.g., 1-2 μm 2).

One easy approach for LFR is to introduce more and more manufacturability aware rules, but such rule-based approach suffers from exploding number of rules, expensive rule-checking, and large area/timing overhead due to over guard-band . Moreover, these rules may still not be able to capture all lithography problems due to complicated 2D interactions. This leads to model-based approaches, which run some lithography simulators/models to guide routing. However, one has to be very conscious about the runtime as the lithography simulators could take prohibitive CPU. In terms of which routing stage to apply lithography correction, there are two main paradigms, i.e., construct-by-correction and correct-by-construction. In the construct-by-correction paradigm, the design is first routed as usual, then the litho-hotspots are detected (e.g., by

some rules of thumbs or lithography simulations/models) and fixed as a post-routing optimization. The correct-by-construction approach, on the other hand, is more proactive by incorporating lithography cost function or constraint directly during routing.

II. LFR Through Construct-By-Correction

Construct-by-correction can be regarded as a *find-and fix* approach, which basically consists of hotspot detection and removal through post-routing optimization. LFR through construct-by-correction starts from a conventionally routed layout which may contain DRC-clean but undesirable layout configurations for lithography printability. Then, the hotspots are detected by either rule-based or model-based methods. Finally, it performs ripup/rerouting, wire spreading/widening and so on, to remove the identified hotspots.

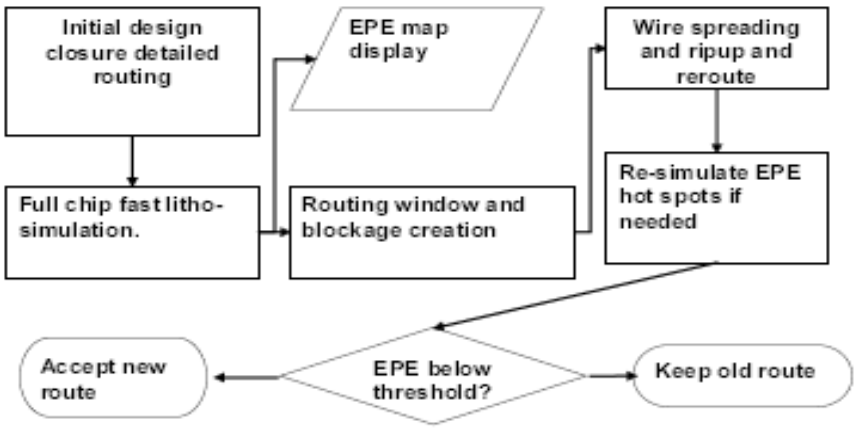

Fig. 1. EPE based construct-by-correction in the model-based method [4].

Hotspot detection is a critical step because it identifies the litho-prone layouts in the design, and provides some guidelines to make the original layout robust. There are mainly two types of litho-hotspots: 1) bridging, where distinct shapes become too close or merged, resulting in a short; 2) notching, where a shape narrows or collapses, resulting in an open. Significant efforts for hotspot detection have been reported. In the rule-based approaches, a set of rules made from fab data are applied to layout in the form of 1D geometric measurements such as minimum line width, minimum space, forbidden pitches, and so on. However, while aggressive RET and OPC models are well defined for simple 1D geometry rules, complex interactions of 2D geometries are difficult to capture and analyze. This leads to 2D pattern matching techniques where pre-defined hotspot-prone patterns are applied in order to supplement 1D rule-based detections. However, as technology moves to 65nm and beyond, the number of rules and hotspot-prone patterns quickly explodes and the rules no longer guarantee acceptable accuracy. To capture all possible hotspots more accurately, model based approaches are proposed with various lithography simulation engines. It should be noted that lithography simulations could be very CPU intensive. The general concept of the litho-hotspot map, edge placement error (EPE) map to measure the overall printability and manufacturing/OPC effort. Given an initial routing, a fast full-chip lithography simulation through kernel decomposition and table-look-up is performed to generate an EPE map. A user defined EPE threshold is then applied to identify the EPE hotspots which are later corrected by wire spreading and ripup/rerouting. Such procedure can be repeated for all litho-hotspots until there is no further improvement. Kong et al. [5] proposed a hybrid method to combine a rule-based approach for fast pre-detection and a model-based approach for post-optimization. They use a conservative rule based filter to detect potential hotspots. The router is then able to fix these potential hotspots with moderate efforts.

All detected hotspots are corrected in the post-optimization step. As a simple guide, it pushes the two offending shapes away for bridging hotspots, while it puts more room around the shape for notching hotspots. There are various post-routing optimization techniques which can be used to fix the hotspots,e.g., wire spreading and fattening within or across layers , rip-up and re-route, via duplication, via shifting and widening, improvement of via metal overlap, wire and jog widening , simultaneous wire spreading widening- filling and more. Usually these post routing optimizations are applied in an iterative manner until there is no improvement. Fig. 1 shows the overall flow of a construct-by-correction lithography friendly detailed routing.

Construct-by-correction is an easy and straightforward way to improve printability, and it does not require major overhaul of an existing routing system. However, if there are too many of these litho-hotspots, its effectiveness will be limited. The major drawbacks include: **(a)** it requires many iterations between routing and hotspot detection/correction if post-rerouted layout keeps creating new hotspots, and there is no guarantee of

convergence **(b)** lithography simulations over large areas can be very computational expensive, especially if the analysis is expanded to various exposure dose, focus, and other process variations, **(c)** post-optimization inherently cannot make radical changes enough to address lithography issue. These motivate LFR through correct-by-construction in Section III.

III. LFR Through Correct-By-Construction

LFR through correct-by-construction is to build a lithography friendly design *during* routing to minimize the number of litho-hotspots, instead of detecting and eliminating them *after* routing. Essentially, some litho-cost functions or constraints need to be incorporated into an existing routing framework to optimize the printability during the routing. The challenge of this approach comes from two parts: **(a)** an effective lithometric, **(b)** efficient integration methodologies of the metric into routing.

The litho-metric plays a key role for a router to be aware of the potential hotspots. It shall have the following properties: **(a)** The post-OPC silicon image should be targeted, as OPC is an essential step in sub 90nm nodes. Some lithohotspots can be easily fixed by OPC, while others cannot be fixed. We should target the real litho-hotspots. **(b)** it should achieve a good balance between accucury/fidelity and runtime.

Actually these two aspects are also important to consider in the construct-by-correction paradigm , but the metric runtime requirement is more stringent here, and the main purpose is *predictive* (before committed layout), versus *detective* (after layout is done).

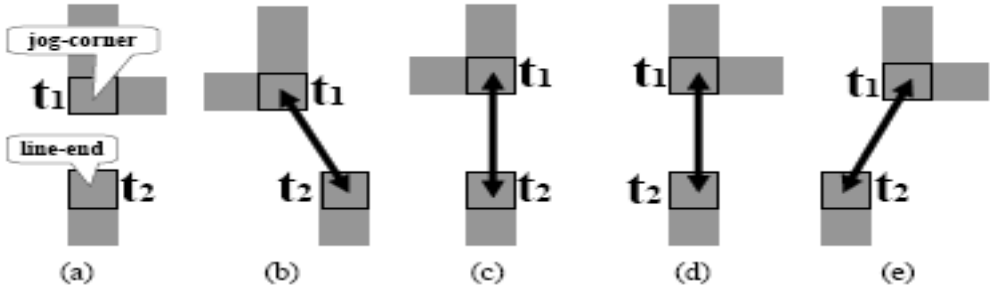

Fig. 2. Characterization for $t1$ jog-corner and $t2$ line-end is shown where (b), (c), (d), and (e) are the cases with the same distance. Thus, the mean EPE will characterize this interaction between $t1$ and $t2$ at this distance.

However, it is not a direct measurement of the printed image to guarantee the printability. Proposed a model-based interference metric for minimizing the litho-cost. They build a lookup table to store the interferences based on optical simulation. Then, the lithocost is evaluated from the table based on the interaction between the patterns within the lithography window. Develop a predictive modeling based on an inverse-like lithographic technique to numerically quantify the OPC cost as a routing guidance. However, these metrics do not show correlation with the post-OPC silicon image fidelity.

A Compact model to predict the post-OPC printability, which directly targets on the post- OPC litho-hotspots. They predefine a number of litho-prone shapes, i.e., weak grids (e.g. line-end, jogs and vias) and obtain the litho-cost between weak-grid interactions at various distances based on post-OPC images. Since multiple patterns exist (Fig. 2) for each weak-grid combination, all possibilities are enumerated using statistical characterizations (e.g., mean EPE). Based on the characterizations, the estimated printability cost can be calculated efficiently as the summation of the lithocost among all weak-grid interactions within the lithography influence and process window. As shown in Fig. 3, this derived metric matches printability from experiments with high fidelity, using extensive industrial-strength OPC runs (such as Calibre). Such model is also very fast to be used within a router to achieve more global optimization in lithography friendly layout.

The litho-cost needs to be incorporated into existing routing algorithms appropriately to prevent potential hotspots. Considering the already heavy burden of routing tools, the optimization strategy should be efficient and provide good trade-off between printability and other traditional objectives. Litho-cost minimization for each net are performed individually without considering the balance between different nets, which may lead to local optimality. Propose a multi-constrained shortest path formulation which can perform the litho-cost optimization over the entire design, but its complexity is proportional to the number of nets, resulting in poor scalability. A similar multi-constrained shortest path formulation, but its approach has the fixed number of constraints regardless of the net number, leading to high scalability for large designs.

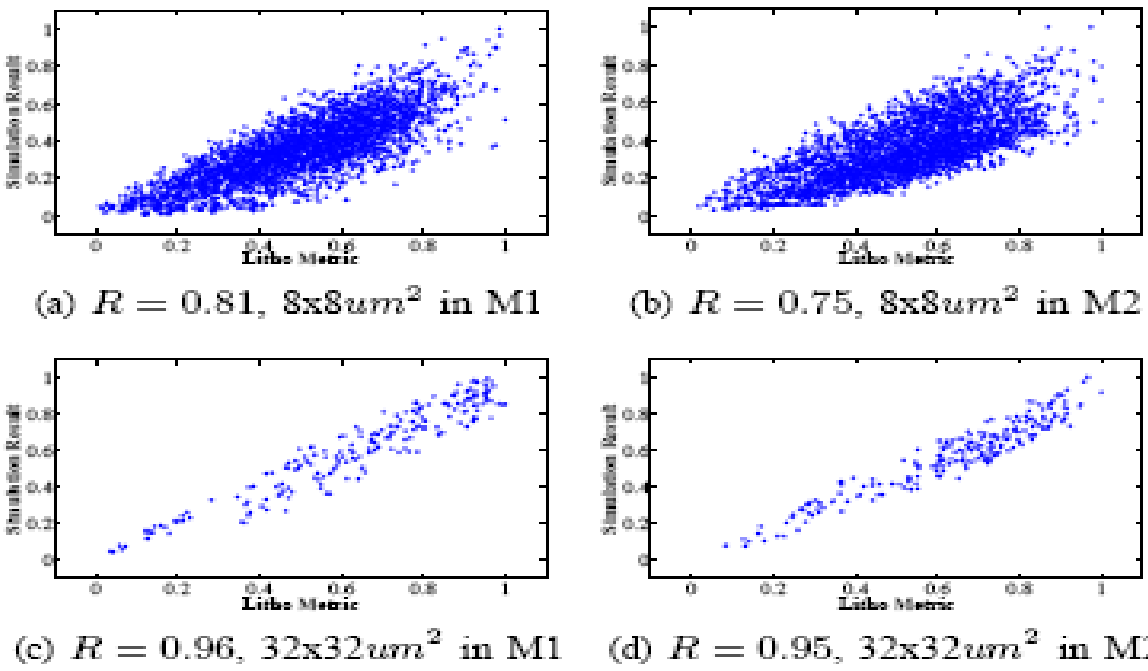

Fig. 3. The litho-metric shows higher fidelity to post-OPC printability in large scale.

Overall, correct-by-construction approach aims at improving printability during design time, which provides more global optimization and more flexibility to prevent litho-hotspots than the post-routing detection and elimination. The authors showed that the proposed correct-by-construction method can achieve 8x litho-hotspot reduction and 12x speedup compared to a construct-by-correction approach [4]. Meanwhile, these two approaches can be combined. That is, correct-by construction approach prevent most problems and provides a good starting point for post-routing correction. Combining these two methodologies can further enhance the overall routing printability.

IV. Conclusion

In this paper, we show two mainstream paradigms to accomplish lithography friendly routing, i.e., construct-by-correction and correct-by-construction. They work together with rules and models of different levels of abstraction, accuracy, fidelity, and runtime, as shown in sections II and III. It shall be noted that LFR is still a relatively new topic, and many techniques are evolving. The consensus of routing regularity (e.g., restrictive design rule) versus flexibility has yet to be fully explored. In addition, there are other manufacturing issues such as critical area, chemical-mechanical-polishing (CMP), redundant via, and so forth. Improving lithography solely may make other aspects (e.g., critical area) worse, and vice verse. Therefore, holistic modeling and optimization of all key manufacturing effects into some "global" yield metric centered by printability will be in great demand.

Looking at future technology nodes, lithography friendly routing needs to support double patterning lithography in 32-22nm nodes, where robust layout decomposition and overlay error are critical issues. Even next-generation-lithographies for sub-22nm nodes still need to consider lithography friendly routing, e.g., to mitigate flare effects for EUV lithography. Lithography friendly routing has to be adaptive to incorporate these new challenges.

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