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Implementation of BIST Test Generation Scheme based on Single and Programmable Twisted Ring Counters

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ABSTRACT:- *Twisted-ring-counters (TRCs) have been used as built-in test pattern generators for high-performance circuits due to their small area overhead and simple control circuitry. When compared to other pattern generators TRC often requires long test time to achieve high fault coverage and large storage space to store required control data and TRC seeds. Programmable Twisted Ring Counter-based on-chip test generation scheme is to minimize both the required test time and test data volume. Programmable Twisted Ring Counter operates on test per clock method to reduce the test time. To reduce the storage data for testing, seed and control vector determination process is used to achieve the less storage data in ROM.*

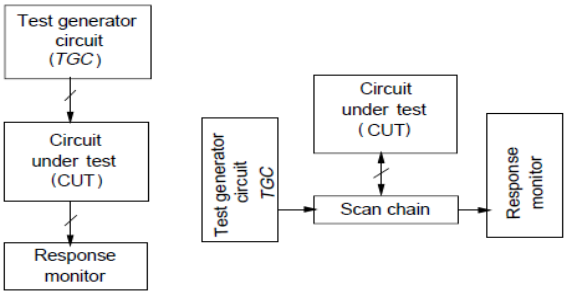
Keywords: *- Programmable Twisted Ring Counter (PTRC), Single Twisted Ring Counter (STRC), Built-In Self Test (BIST), Ring Counter (RC), Circuit under Test (CUT), Test Generation Circuit (TGC).*

I. INTRODUCTION

BIST techniques are the most efficient one for testing any high performance circuits but time taking is long. The fault coverage using BIST techniques is less compared the proposed technique. In general BIST techniques are classified based on test per scan and test per clock. Test per scan is time taking process for fault coverage because while loading the data and while generating patterns these are operated at bit by bit. Hence test time is long.

Test per clock is less time taking process because while loading data in the BIST or while generating patterns these are operated in parallel, for example the CUT is taken as a four input circuit, hence the test per clock technique BIST can able to generate four bits at a time and hence test time is reduced. BIST, based on test per clock technique leads to less test cost. Therefore set of bits are applied directly to CUT.

For generating different patterns input seed is required. Seed is the initial response of the LFSR. But the seed is selected such that it covers maximum number of faults, which includes testable faults and hard-to-detect faults. Testable faults change the output functionality, and hard-to-detect fault doesn't change the output functionality. For example stuck at zero at input of AND gate can be considered as hard-to-detect fault.



(a) **(b)**

Fig .1 (a) Test per clock and (b) Test per scan BIST

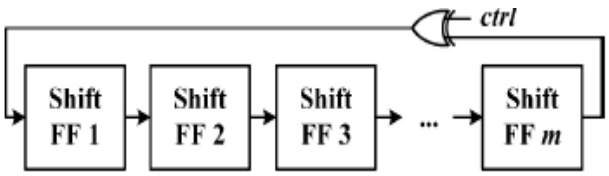


Fig .2 Twisted Ring counter

Twisted ring counter are based on test per clock scheme which covers maximum faults. Using TRC technique the unique seed can be found easily. TRC can be used as single Twisted Ring Counter or programmable Twisted Ring counter. Single twisted ring counter technique is slow process in generating test patterns because the scan registers cannot be divided into multiple segments and no control unit for changing the mode from ring to twisted ring. Using test per clock method scheme the following advantages can be obtain, 1) circuit simplicity, 2) controllability, 3) easy to implement. With these advantages PTRC is more efficient compared to other schemes like Single Twisted ring counter.[1]

A separate control unit is present in the proposed scheme of PTRC to generate the required patterns and same control unit is used to load the seed into scan registers. Control unit is called Reversion logic unit. A ROM is used to store all seeds such that each seeds are stored to get maximum fault coverage. To achieve high fault coverage reseeding technique is used with the help of control unit. Although the number of seeds are less in ROM but the test sequence length is longer for each seed.

In this paper a Programmable TRC based on chip test generation scheme is proposed. In Programmable Twisted Ring Counter, Programmable represents scan register is split into segments according to number of inputs in CUT, hence each segment is converted into one PTRC. With such programmable nature minimal seed is detected using seed and control vector determination process. A simple centralized switching unit is used to load and for TRC operation in PTRC logic unit. Seed is given as input to PTRC from ROM. The test patterns generated from each PTRC are applied to corresponding CUT circuit inputs to detect testable as well as hard-to-detect faults.

To show the efficiency of Programmable Twisted Ring Counter, it is compared with Single Twisted Ring Counter. Single Twisted Ring Counter has fewer features because there is no control unit to generate required patterns in a specified time and no programmability in scan register block. S27 benchmark circuit is used as CUT to detect the induced faults.

The faults include testable and hard to detect faults. In rest of the paper, we describe the proposed on-chip test generation scheme, Single Twisted Ring Counter in section III seed and control vector determination process in section IV, simulation results of PTRC and faults detected from s27 circuit in section V, comparison of PTRC with STRC in section VI.

II. TEST PATTERN GENERATION BASED ON PROGRAMMABLE TWISTED RING COUNTER

The PTRC design proposed in this paper is based on the design shown in Fig. 1(a), which can generate the maximum number of test patterns. The scan segments are represented as n and scan register bits are represented as m. Total 3m different test patterns are generated form PTRC. In addition the PTRC can also be programmed to perform different modes of operations using reversion logic unit. Fig. 3 shows the PTRC scheme consists of reversion logic unit, mode switching logic unit, PTRC logic units [1].

A simple centralized mode switching logic unit is used to count the number of clock cycles for each pattern generation from the test generation circuit. The clock cycles are counted by the variable called k, and k is defined by $k=\log_2 m$ where, m is length of the shift register or the length of the segments. The clock cycles are counted by the k-bit binary counter. The enabling of s counter is done by using AND gate in between 2-bit counter and k-bit binary counter.

The S1,S2 2-bit binary counter is operated in centralized mode switching logic unit for enabling the mode of operation in the test generation circuit, this is denoted by s counter and it is enable by the k-bit counter. The S counter value initially in 00 and incremented only by k-bit counter. The s value (00) is stable until the k value completes its count sequence from 00 to 11. Then s counter value will vary according to K value.

Distributed reversion logic units are developed that take control of various TRC operations to generate the required test patterns based on the seeds. By providing appropriate input control data, the state of each PTRC design can be individually programmed and thus the probability to generate required test patterns can be greatly enhanced. With such a programmable feature, we have developed an efficient procedure that aims to determine a minimal set of seeds and their corresponding PTRC control signals such that both the total number of seeds (storage test data volume) and test sequence length (test application time) can be minimized.

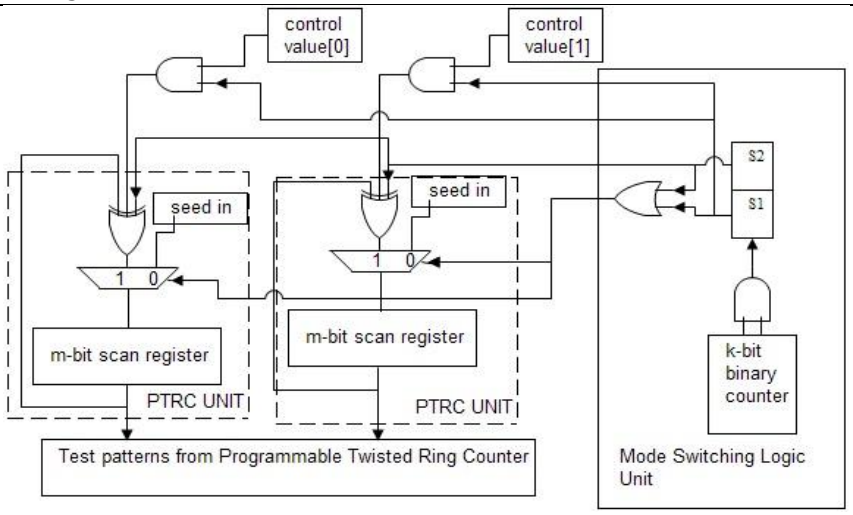


Fig .3 Programmable Twisted Ring Counter with two scan segments.

TABLE I Control signals for different PTRC modes

Control value	S2	S1	PTRC Mode
0	0	0	Shift in
	0	1	Rotate
	1	0	Twist
	1	1	Twist
1	0	0	Shift in
	0	1	Twist
	1	0	Twist
	1	1	Rotate

m-bit scan register is used to generate the patterns, that test the circuit in test mode applied using switching logic unit. When the switching unit is in 00 mode, then the scan register is in shift-in which loads the seed data to all flip-flops. After loading all the seed data according to the mode of operation the patterns are generated with maximum possibility.

III. SINGLE TWISTED RING COUNTER

The set of seeds with their control vectors are stored in ROM. The detail description of seed and control vector determination process is given below. Both PTRC and STRC work on the same principle but PTRC is programmable with any number of segments where as in STRC there is no segment formation and STRC depends on m-bit scan register.

The single Twisted Ring Counter is based on Test per clock basis. In this scheme also all the seeds are stored in ROM for generating test patterns. The TGC operates in two modes namely Twist and Rotate [2].

A single 4:1 MUX is to control the two modes of operation. K-bit counter is used to know the number of test cycles when test patterns are applied to CUT and faults are detected.

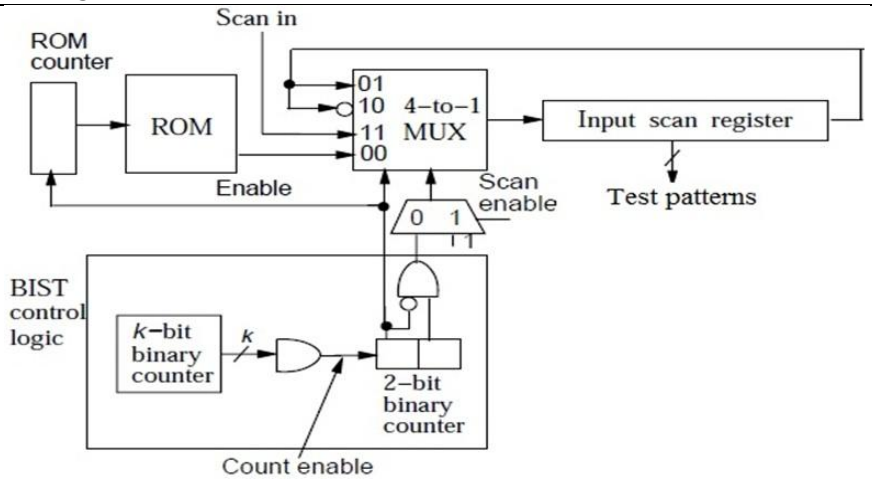


Fig .4 Single Twisted Ring Counter based TGC

Single Twisted ring counter also works based on the TRC technique. The property of TRC defines the generation of test patterns. For example: an n-bit ring counter is connected in a group of n flip flops which looks like shift register. The output of last flip flop is fed back to first flip flop input. It behaves as ring counter with n distinct states [3],[4].

IV. SEED AND CONTROL VECTOR DETERMINATION PROCESS

The seed and control determination process is provided in steps below. The inputs to this process is all possible pre-determined test set T and set of faults that are detected by test set T. The set of faults may contain testable faults(F_t) and hard-to-detect faults(F_{hd}). Based on the test set the different patterns are generated, the initial output of LFSR is called seed, which is given to input of the control vector determination process.
Steps for seed and control vector determination process:

1. Know all the possible number of faults: Fault set.
2. Calculate the weight of each fault.
3. Calculate the pattern weight.
4. The highest pattern weight can get harder to detect faults.
5. Seed is taken as input for test generation scheme and generate nine different patterns to find the remaining faults.
6. Comparing all patterns with the generated patterns.
7. Calculate the seed weight based on matching of patterns.
8. Finally seed is stored in ROM.

The weight of fault is defined by $1/d(f_i)$, where $d(f_i)$ is called detection count i.e., detection count of each fault f_i in fault set. Pattern weight is denoted by pw (t_i), where pattern weight is the sum of the weights of all faults in fault set that are detected by test set. Seed weight can be computed as sum of the pattern weight of t_i. For doing this process initial control vector can be either 0 or 1 [1].

The faults which are detected, those can be removed from the fault set and again the process is repeated by flipping the control vector for generating some other different test patterns. Finally the seed and control vector combination gives maximum fault coverage, it is stored in ROM. The process is repeated until all the fault set is detected.

The total test length of the scheme is in proportion to the number of scan cells in one segment. Using a large number of small-size scan segments in the scheme, the test sequence length is reduced, but for achieving complete testing total number of seeds also required. Hence Test data and Test sequence length reduction procedure is used to reduce the number of seeds.

V. SIMULATION RESULTS OF PTRC

Programmable Twisted Ring Counter is used to generate the patterns which is to test the circuit under fault condition. For the test generation circuit, mode switching logic unit and reversion logic are the important

blocks for change of mode and for generate different combination of patterns. Reversion logic unit is operated with control input 0 or 1 and mode switching logic unit is to stabilize the mode for certain clock cycles. The test patterns are generated with PTRC technique is shown below with seed value 001 010.

The patterns which are generated from Test Generation Circuit can be used for detecting the faults. For seed and control vector determination process all the test vectors of all faults are recorded. In general test vector can be found using Boolean difference, D-algorithm, Fan algorithm and some other techniques. Consider some of the test vectors which can detect some faults as shown in the Table III.

Let the initial seed be T1=110 0X0 and two segments of PTRC each segment having 3 bits, from this seed different patterns are generated using PTRC. The different patterns from the seed T1 is shown in table IV.

TABLE II Responses of PTRC segment

Segment 1 Control value : 1	Segment 2 Control value : 2
Seed → 001	010
000	001
100	100
110	010
111	101
011	010
001	101
100	010
010	101
001	010

TABLE III Test vectors

Notation	Test vectors
T1	110 0X0
T2	011 XX0
T3	101 0XX
T4	001 X1X

TABLE IV Test patters from PTRC for test vector T1

Segment 1 Control value : 0	Segment 2 Control value : 1
110	0X0
011	XX0
101	0XX
110	X0X
111	XX0
011	1XX
001	X1X
000	XX1
100	0XX
110	X0X

From the table it is concluded that the vectors 101 0XX and 001 X1X can merge with the recorded test set. Once all the faults are detected using the steps given the process is terminated. Hence instead of storing two vectors in ROM one vector is enough to store, this one vector can detect few more faults by generating the test patterns using PTRC.

VI. COMPARISON BETWEEN PTRC AND STRC

The table V shows the comparison between STRC and PTRC. From the Table V it is concluded that PTRC is more efficient than STRC. Test time is more in STRC due to constant number of segments.

TABLE V Comparison between PTRC and STRC

Parameters	PTRC	STRC
Number of segments	Variable	Constant
To load 6-bit data	3 clock cycles	6 clock cycles
Power	170.54 uw (for 6 -bit)	236.05uw (for 6-bit)
Time slack	4516 ps	4483 ps
To generate 9-test patterns	3+9 => 12 clock cycles.	6+9 => 15 clock cycles.

VII. CONCLUSION

A Programmable Twisted Ring Counter-based BIST scheme can reduce the test time and total test cost, for digital circuits to obtain maximum fault coverage, this can be seen from Figure 5 and 6 .Experimental results confirmed that Programmable Twisted ring counter has been implemented successfully and used to test a sequential circuit (S27 benchmark circuit). For the S27 benchmark circuit 9 test patterns were used to cover stuck-at faults.

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