Design of Modified Carry Select Adder

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ABSTRACT: *Carry Select adder (CSLA) is an adder which computes n+1 bit sum of two n bit numbers. When compared to earlier Ripple Carry Adder and Carry Look Ahead Adder, Regular SQRT CSLA (R-SQRT CSLA)is observed to provide optimized results in terms of area[1]. From the architecture of Modified SQRT CSLA [2] it is experimental that there is a possibility of reducing the area .Regular CSLA uses dual Ripple Carry Adder to perform addition operation. Modified SQRT CSLA (M-CSLA) uses BEC as add one circuit which reduces the area furthermore, such that the total gate count is reduced subsequently. For 16 bit addition in this paper, it is proposed to simple gate level alteration which expansively reduces the area by 34% when compared with R-SQRT CSLA and 15% when compared to M-SQRT CSLA .It is known as Modified Area Efficient SQRT Carry Select Adder (MA-SQRT CSLA). The premeditated work in MA-SQRT CSLA reduces the area using the modified EX-OR gates. The result investigation shows that the Modified area efficient SQRT CSLA is enhanced than the M-SQRT CSLA for low power applications like digital signal processing, ALU.*

Keywords – *Binary to Excess-1 converter(BEC),Carry Select Adder(CSLA),Field Programmable Gate Array (FPGA), Multiplexer (MUX),Ripple Carry Adder(RCA),Exclusive OR(EX-OR).*

I. INTRODUCTION

In digital circuits the optimization of gates is essential. Area and power efficiency can be achieved by gate level modification. This idea has been incorporated in MA-CSLA. Ripple Carry Adders (RCA) used much less complicated circuits when compared to other adders. However in this elementary Carry Select Adders (CSLA) the speed of addition is limited by the carry that ripples from the least significant bit to the most significant bit. Carry Select Adder (CSLA) is one of the most significant adders to perform faster addition operation when compared to other adders because of the usage of multiplexers [2]. In order to overcome carry propagation delay, the CSLA simultaneously generates carry at different stages and then it selects a carry to generate the sum. Since it uses multiple Ripple Carry Adders it is not that much area efficient. Therefore the Modified SQRT CSLA alleviates this problem by introducing an add one circuit. In regular CSLA, there are two Ripple Carry Adders. They are RCA with (C_{in}=0) and RCA with (C_{in}=1). In Modified SQRT CSLA (M-SQRT CSLA), BEC [2] is used instead of RCA with C_{in}=1.The Modified SQRT CSLA (M-SQRT CSLA) is chosen for comparison with MA- SQRT CSLA as the area is drastically reduced. The FPGA implementation results are discussed in section VII.

II. AREA EVALUATION OF BASIC AND-OR-INVERTER (AOI) GATES

The implementation of EX-OR gate is shown in the Figure 1. The area evaluation is done by the AND, OR and NOT (INVERSION) gate each having an area of 1 unit. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

Table I Area Count of the Basic Blocks of CSLA

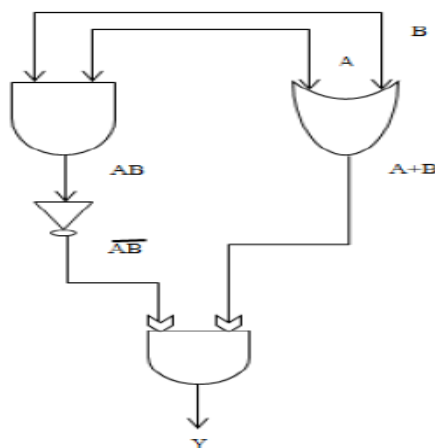| ADDER BLOCKS	AREA
EX-OR	**4**
XOR	5
2 : 1 MUX	4
HALF ADDER	6
FULL ADDER	13

Fig. 1: Area Evaluation of Exclusive Or Gate

III.   EXCLUSIVE OR OF MODIFIED AREA EFFICIENT SQRT CSLA

The main idea of MA- SQRT CSLA is to use 4 gates EX-OR which reduces the total gate count. From the Figure 2 it is clear that there is the possibility of reduction of gates by using the XOR gates which has been proposed in our design. In the Modified SQRT CSLA the total number of XOR gates is 213. In Modified Area Efficient SQRT CSLA (MA - SQRT CSLA) the total number of EX-OR gates is 168.In the Modified Area Efficient SQRT CSLA (MA – SQRT CSLA) the following expression would be used for an EX-OR operation.
Y= (a+b) (~ab)

IV.   OPTIMIZED BEC

The EX-OR gate in BEC of Modified SQRT CSLA is replaced with the optimized   EX-OR gate in AOI of Modified Area Efficient SQRT CSLA .With BEC there is reduction of gates by replacing n bit RCA with n+1 bit BEC [2]. When the optimized EX-OR gate is used in Modified SQRT CSLA, it is verified that there is large reduction in number of gates. The MUX is used to select either the BEC output or the inputs given directly to a BEC circuit [2]. In this design, the major function of MUX is to derive the adder speed.

V.   AREA EVALUATION OF MODIFIED SQRT CSLA

The structure of 16 bit Modified SQRT CSLA (M- SQRT CSLA) is shown in the Figure 2 and the area evaluation is also illustrated. The group2 has one 2-bit RCA which has 1 Full Adder (FA) and 1 Half Adder (HA) for C_{in} =0.Instead of another 2-bit RCA with C_{in} =1 a 3-bit BEC is used which adds one to the output.
The area count is determined for group2 is as follows:
Gate count=43(FA+HA+MUX+BEC)
FA=13(1*13)
 HA=6(1*6)
AND=1
NOT=1
XOR=10(2*5)
MUX=12(3*4)

Similarly the gate count is determined for other groups. In this paper, the area evaluation is done with the AOI gates into consideration. In Modified Area Efficient SQRT CSLA an EX-OR gate in Figure 2 has been used, such that the total gate count is reduced. So the reduction in the total number of gates in Modified Area Efficient SQRT CSLA (MA- SQRT CSLA) compared to the M- SQRT CSLA and R-SQRT CSLA [2] has been illustrated in the following table 2. Table 2: Comparison of 16 Bit Gate Count

Groups	Regular SQRT CSLA	Modified SQRT CSLA	Modified Area Efficient SQRT CSLA
Group 1	26	26	26
Group 2	57	43	40

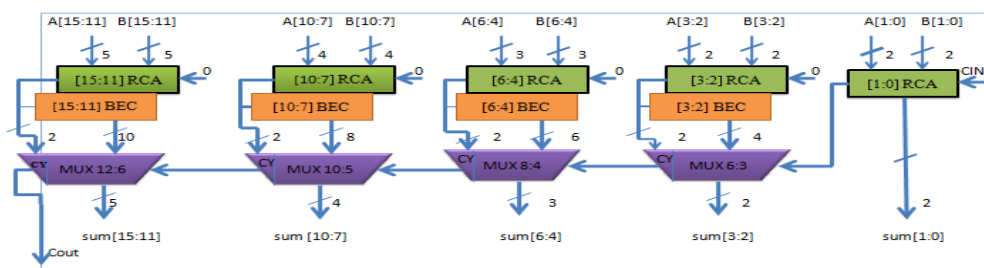|			
Group 3	87	66	61
Group 4	117	89	82
Group 5	147	112	103
TOTAL	434	336	312

Fig. 1: Modified SQRT Carry Select Adder (M- SQRT CSLA)

VI. AREA EVALUATION OF MODIFIED AREA EFFICIENT SQRT (MA- SQRT CSLA) CSLA

The structure of 16 bit Modified Area efficient SQRT CSLA (MA- SQRT CSLA) is shown in the Figure 3 and the area evaluation of each group is also illustrated in Figure3a, Figure 3b, Figure 3c, Figure 3d .The group2 has one 2-b RCA which has 1 FA and 1 HA for C_{in}=0.Instead of another 2-bit RCA with C_{in}=1 a 3bit AOI is used which adds one to the output. The architecture of modified area efficient CSLA is shown in Figure 3.
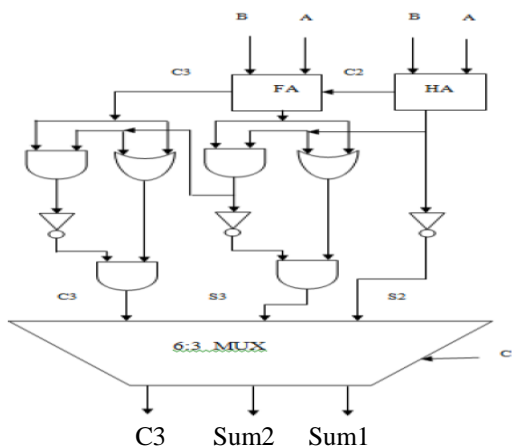
The gate count for group2 is as follows Group 2:

Gate count = 37(FA+HA+MUX+EX-OR)
FA = 11 (1 * 11)
HA = 5 (5 * 1)
EX-OR = 9 (NOT=3, AND=4, OR=2) MUX=12(3*4)
 Similarly, the gate counts for other groups are determined. The result is observed in table 2.

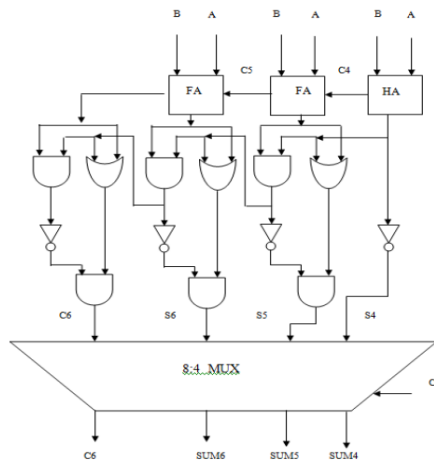In Figure 3a. GROUP 2. It is verified that when C1=0 the 2 bit sum arrives from RCA. When C1=1 the 2 bit sum arrives from EX-OR.
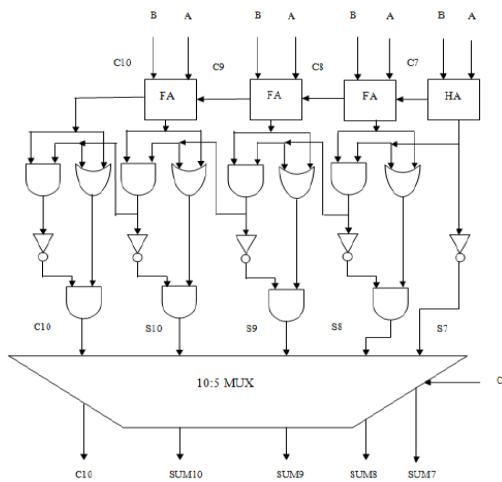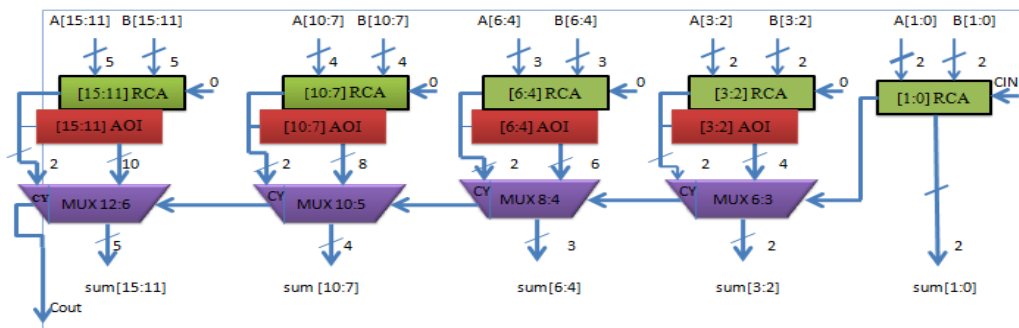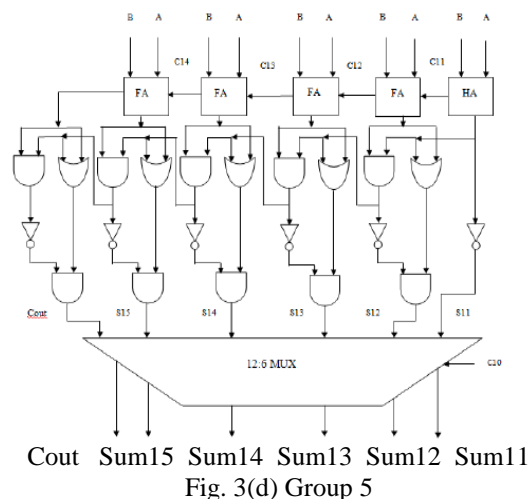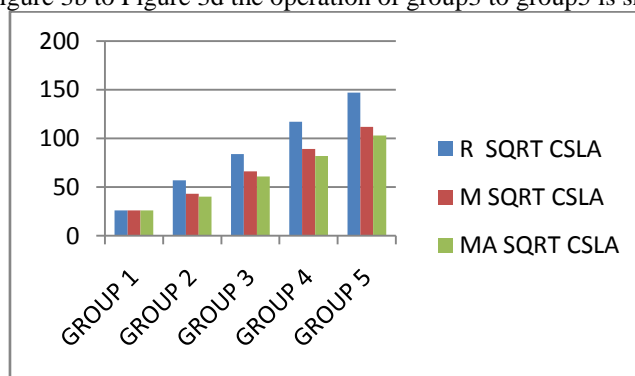
Fig. 3(b) Group 3

Fig. 3(C) Group 4

Fig. 3: Modified Area Efficient SQRT Carry Select Adder (MA-SQRT CSLA)

Fig. 3(d) Group 5

In Figure 3b to Figure 3d the operation of group3 to group5 is shown.

Graph 1: 16 Bit Graphical Representation of Table 2

VII.   FPGA IMPLEMENTATION RESULTS

The design proposed in MA- SQRT CSLA is successfully tested using atlys (Xilinx) Spartan 6   LX 45 series target and verilog HDL. The MA-SQRT CSLA architecture is simulated using isimulator. The result analysis of Modified CSLA (M- SQRT CSLA) Fig. 4 and Modified Area efficient CSLA (MA- SQRT CSLA) Fig. 5 is compared below.
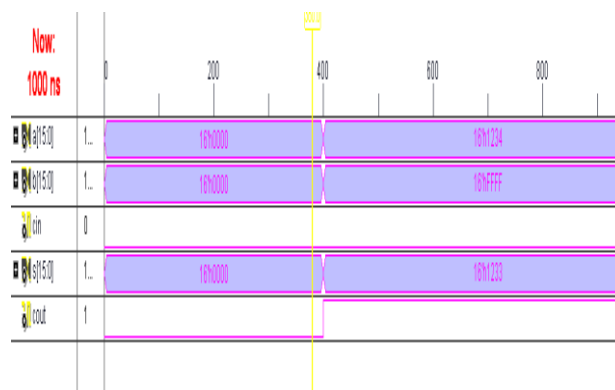

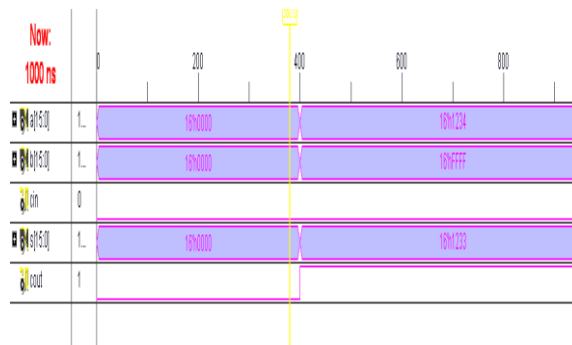Fig. 4: Simulation result of Modified SQRT CSLA

Fig. 5: simulation result of Modified Area Efficient SQRT CSLA

VIII.   RESULTS

This work has been developed using Xilinx tool. **Table III** shows the comparison between the various adders like conventional CSLA, Regular SQRT CSLA, M SQRT CSLA and MA - SQRT CSLA for 16-bit, 32-bit, 64-bit and 128 bit. Graph 2 depicts that the MA- SQRT CSLA has less number of gates and hence less area.

Table 3: Comparison of Gate Count

VARIES TYPES OF CSLA	16 BIT	32 BIT	64 BIT	128 BIT
CSLA	468	936	1872	3744
R SQRT CSLA	434	844	1720	3642
M SQRT CSLA	336	665	1339	2801
MA SQRT CSLA	312	620	1246	2588
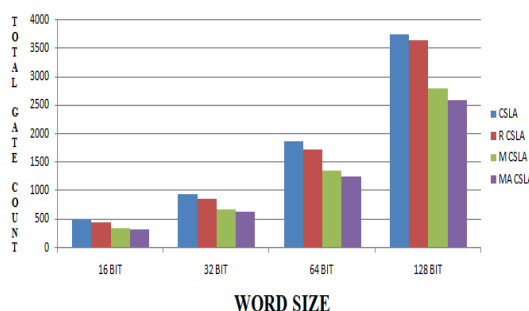
Comparison of adders for area (no. of gate count)

Graph 2 Comparison of adders for area count.

VIII.   CONCLUSION

A simple approach is proposed in this paper to reduce the area of Modified SQRT CSLA architecture. The vast reduction in the total number of gates is advantageous in terms of both areas. The 16 bit addition operation simulated using Xilinx is implemented in the FPGA kit. The MA-SQRT CSLA architecture is simple and efficient compared to 16-bit Modified SQRT CSLA. In MA-SQRT CSLA, the implementation of 32-bit/64-bit/wider bit additions would produce enhanced results than the R-SQRT CSLA and M-SQRT CSLA.

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