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VHDL Implementation of DSDV Ad-Hoc Routing Protocol

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Abstract: *An Ad-Hoc network deals with the collection of mobile nodes without any centralized structure. This can be well suited for environment where changes are frequent and establishment of infrastructure is not very cost effective. In short it can turn the dream of 'anytime anywhere' into reality[1]. Here we deal with the VHDL implementation of DSDV(destination sequenced distance vector) routing protocol to fulfill these requirements of Ad-hoc network more effectively.*
Keywords: *Adhoc, DSDV,FPGA,VHDL,Routing*

I. Introduction

For the Ad-hoc network we need to deal with various issues of routing protocol, security etc. For handling the changes in Ad-hoc network efficiently some protocols had been developed as a solution known as routing protocols. It is mainly categorized in two types: 1) **Link State Routing Protocol 2) Distance Vector Routing Protocol**. Based on these divisions various protocols had been developed so far, one of these is DSDV. DSDV is the proactive routing protocol in which data packets are exchanged between various nodes or stations of the network. It is introduced mainly from conventional Routing information Protocol(RIP) and is using advanced version of Bellman Ford algorithm. It includes sequence number to each route table entry with metric number, destination Id, Source Id and number of hops required for completion of route [2]. Based on these table entries route is maintained and erased. By the use of sequence number the mobile nodes can distinguish between the stale route information and thus preventing the routing of negative loops.

II. VLSI Architecture of DSDV

The VLSI architecture of DSDV protocol [3]has been depicted in Fig.1. It consists of Data Link in buffer to store the input control information to be transmitted from nodes and received by node in tabular format. Data Link out buffer is use to store output control information that is forwarded to neighbours (nodes). RIM (route information memory) stores the information necessary to identify the next hop address for optimized route.

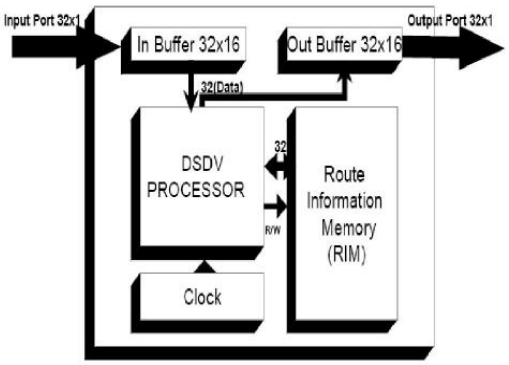

Figure1. The implemented architecture of MANET node[1]

The FSM of DSDV control unit had been depicted in Fig.2. It processes the three states with the help of three processors. It has four states 1) Idle state 2)Table Transmission (periodic update) 3) Receive Input 4) Checking Stale Node.[5,7]

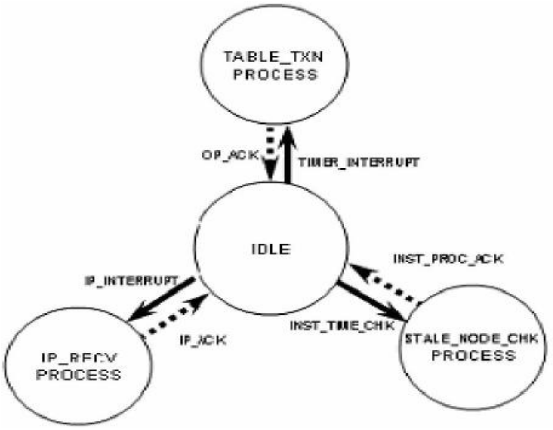

Figure2. Sequence of three main functions in DSDV processor [4]

III. FPGA Implementation

The shown architecture of DSDV control unit is implemented using VHDL coding with simulation performed on ModelSim Simulator and synthesis report had been obtained by Leonardo Spectrum of Mentor Graphics.

3.1 Simulation Report

Simulation waveform of DSDV control unit has been depicted in Fig.3.

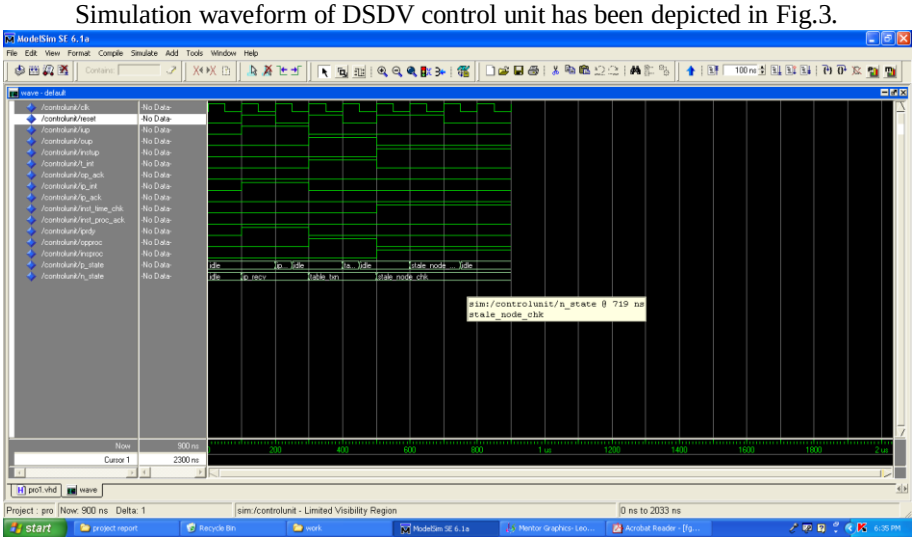

Figure 3Simulation waveform of control unit

3.2 Synthesis Report

The synthesis performed on Leonardo Spectrum gives the following report

3.2.1 Synthesis Report

Cell: controlunit View: behavioral Library: work
Cell: controlunit View: behavioral Library: work

Cell	Library	References	Total Area
Cell	Library	References	Total Area
AN3T0	scl05u	2 x 6	12 gates
AN4T0	scl05u	2 x 8	16 gates
FD1B0	scl05u	2 x 9	17 gates
IV1N0	scl05u	3 x 3	9 gates
LD1A0	scl05u	5 x 7	33 gates
MX2L0	scl05u	1 x 6	6 gates
ND2N0	scl05u	1 x 5	5 gates
NR2R1	scl05u	1 x 5	5 gates
NR3R0	scl05u	1 x 6	6 gates
OA1R0	scl05u	1 x 6	6 gates

```
OAI3N0    scl05u    1 x     8     8 gates
OAOI0     scl05u    1 x     8     8 gates
 Number of ports :                 14
 Number of nets :                  33
 Number of instances :             21
 Number of references to this view :    0
Total accumulated area :
 Number of gates :                 131
 Number of accumulated instances :     21
Info, Command 'report_area' finished successfully
->report_delay  -num_paths 1 -critical_paths -clock_frequency
Using default wire table: SCL_CORE_4K

  Clock Frequency Report
Clock              : Frequency
    ------------------------------------
          clk              : 461.8 MHz
 Critical Path Report
Critical path #1, (unconstrained path)
Critical path #1, (unconstrained path)

NAME      GATE      ARRIVAL      LOAD
clock information not specified
delay thru clock network                    0.00 (ideal)
reg_p_state(0)/Q          FD1B0     0.00  0.48 dn        0.26
ix332/X                   NR2R1      0.52  1.00 up        0.34
ix350/X                   OAOI0      0.35  1.29 up        0.06
ix69/X                    OAI3N0     0.42  1.71 dn        0.06
ix337/X                   IV1N0     0.40  2.11 up        0.28
lat_iprdy/G               LD1A0      0.00  2.11 up        0.00
data arrival time                    2.11
data required time                   not specified
-----------------------------------------------------------------
data required timenot specified
data arrival time                    2.11n sec
 ----------
unconstrained path
-----------------------------------------------------------------
```

RTL synthesis, circuit representation and block diagram view of DSDV Control unit has been depicted in Fig.4,Fig.5 andFig. 6 respectively.

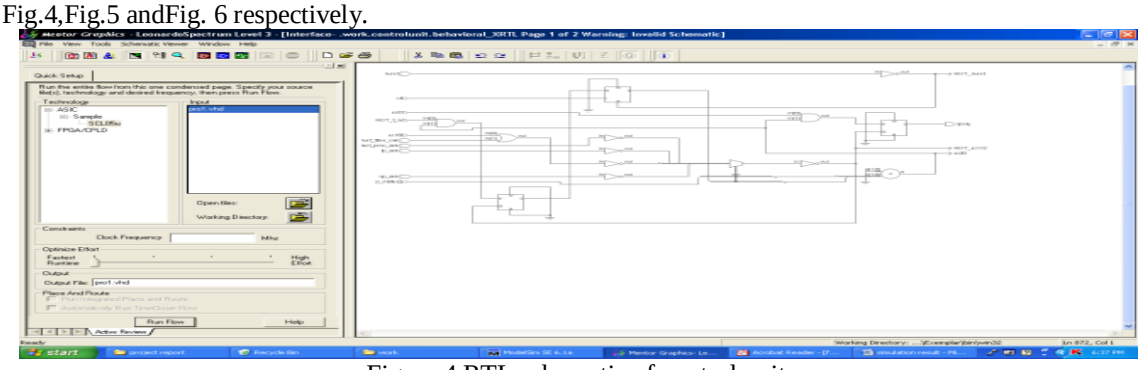

Figure 4 RTL schematic of control unit

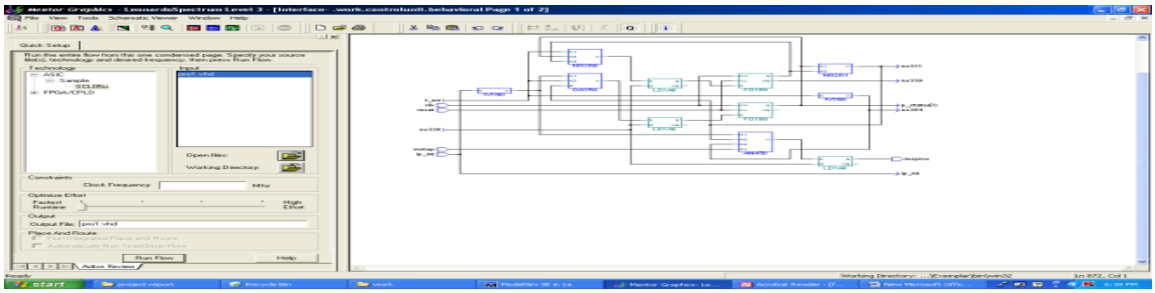

Figure 5 Technological view of control unit

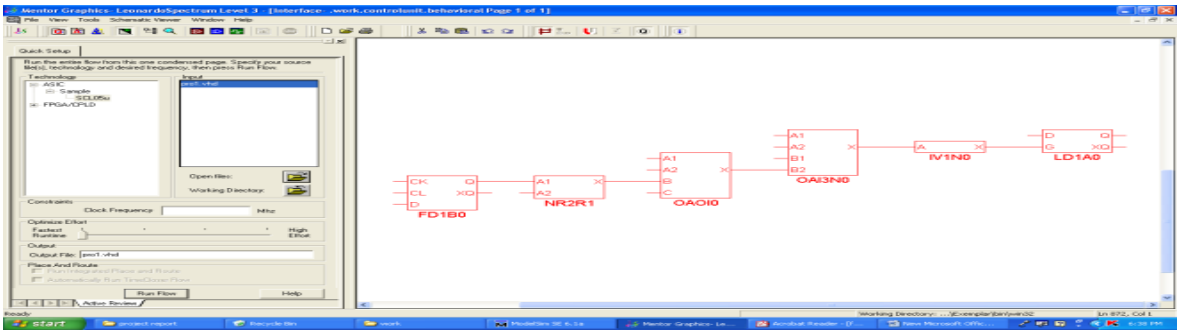

Figure 6 Critical path of control unit

This report had obtained a much optimized arrival time of **2.11 nsec** only and clock frequency of **461.8 MHz**.

IV. Conclusion

From the results obtained from synthesis we can conclude that FPGA implementationof DSDV control unit can give the operating frequency in MHz and arrival time in nsecs, which is much optimized then its counterpart implementationtechnique.

V. Future Scope

The proposed architecture of control unit of DSDV gives reduced call setup time and quick handling of dynamic topology under huge traffic, thus improved speed and efficiency of router can be obtained. In future more optimized concept can be introduced by using reconfigurable protocol which can switch according to the requirement and condition of environment. This future advancement can provide a better clock frequency and arrival time by using FPGA implementation instead of software implementation such as using NS2.

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