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A Review Paper on the Implementation of a High-Speed Floating Point Multiplier Using Vedic Mathematics

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Abstract - *This review article focuses on the use of Vedic Mathematics sutras to create high-speed floating point multipliers. Numerous Vedic multiplication methods, including Urdhva Tiryagbhyam, Nikhilam, and Anurupye, have been thoroughly studied for arithmetic multiplications. The Urdhva Tiryagbhyam Sutra has been discovered to be the most effective Sutra (algorithm), delivering the least amount of delay for multiplying all kinds of numbers. The Mantissa is multiplied using the Urdhva-triyakbhyam sutra. Cases involving underflow and overflow are handled. With the Urdhva Tiryakbhyam sutra, many Vedic multipliers with great speed have been presented. Compressor-based Vedic multipliers outperform conventional ones in terms of speed and area efficiency, according to observations.*

Keywords -*Vedic Mathematics, Urdhva-triyakbhyam, Floating Point Number*

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I. INTRODUCTION :

Vedic mathematics describes a method of computation based on a collection of 16 sutras, or aphorisms, known as algorithms, and their upa-sutras, or corollaries, which were formed from these sutras. With the use of these sutras, any mathematical issue (including algebra, arithmetic, geometry, and trigonometry) can be resolved mentally. Modern mathematics lacks the coherence of Vedic mathematics. Vedic Mathematics provides a novel and incredibly effective method for learning mathematics across a broad spectrum. It begins with simple addition and ends with the solution of nonlinear partial differential equations, which is a relatively complex subject. The Vedic plan is a system, a coherent approach, not just a collection of quick fixes. In every practical application, Vedic mathematics extensively makes use of the properties of numbers. High-speed multipliers have become increasingly vital in modern architectural design, and scientists are still exploring various ways to speed up the operation of these foundational components. For increased effectiveness, high-speed multiplier design algorithms have been improved. There have been suggested new array structures. Many hybrid adders have been created to replace the functions of a simple multiplier. Increased application complexity necessitates not only faster multiplier chips but also more intelligent and effective multiplication algorithms that can be built into the processors. The multiplier's implementation depends on the current situation's demands, the application being used, and the trade-offs that must be taken into account. In general, the variations in speed, size, and configuration are used to categorize the efficiency of multipliers.

II. LITERATURE REVIEW

Two formats, single and double precision, are used to represent floating point numbers in the binary number system. The exponent, mantissa, and sign fields define these formats. 32 bits make up the single precision, together with a 23-bit mantissa, an 8-bit exponent, and one sign bit. The 64-bit double precision has a 52-bit mantissa, an 11-bit exponent, and one sign bit. The number's sign is represented by the sign bit. Positive numbers are represented by "0" in the most significant bit (MSB) position, and negative numbers are symbolized by "1". The floating point numbers are represented by the following in IEEE-754 format: Single Precision: Sign Exponent Mantissa (1-bit) (8-bits) (23-bits) Double Precision: Sign Exponent Mantissa (1-bit) (11-bits) (52-bits) In the instance of Single, the mantissa is represented in 23 bits, and one bit is added to the MSB for normalization. The Exponent is expressed in 8 bits, biased to 127, but in reality, the exponent is represented in an excess 127 bit format, and the MSB of the single bit is saved for the sign bit. When the sign bit is set to 1, it indicates that the number is negative, and when it is set to 0, it indicates that the number is positive. The mantissa is represented in 64 bits using 52 bits, the exponent is expressed in 11 bits biased toward 1023, and the MSB of the double is saved for the sign bit. When the resulting exponent is greater than or less than 8 bits in the case of a single floating point number, an overflow or underflow case arises. When adding two exponents, there is a chance of overflow, which can be corrected by deducting the bias from the exponent result. The overflow flag is raised when overflow occurs. When the number falls below zero, the underflow can happen after the bias has been subtracted from the exponent. In this scenario, adding 1 during the normalization stage can correct the issue. The underflow flag increases when an underflow situation occurs.

III. FLOATING POINT MULTIPLICATION:

The sign bit, exponent, and mantissa of the product are calculated during floating point multiplication of numbers expressed in either single precision format or double precision format. The result is then normalized and rounded off. The sign bits of two operands are combined to create the sign bit. To get the product exponent, the exponents of the two operands are added. To get the biassed exponent, the resultant total is subtracted from 127 for single precision and 1023 for double precision. For single and double precisions, respectively, an 8-bit and an 11-bit ripple carry adder are used in the addition operation. High speed adders can be used to increase performance. Any of the multiplication algorithms is used to multiply the mantissa.

IV. USING VEDIC ALGORITHM:

The Urdhva Tiryakbhyam sutra of Vedic mathematics is discussed in the current study and used to multiply floating point numbers using mantissas. Multiplication both vertically and across is known as Urdhva Tiryakbhyam. Both vertical and crosswise multiplication are applied to each bit of each operand. There is evidence that the Vedic multiplier is more effective in terms of space and time delay. Vedic mathematics sutras can also be used to multiply numbers near to powers of ten in a straightforward manner, removing the need to follow cumbersome traditional multiplication procedures.

V. CONCLUSION:

The Vedic methods of multiplication shorten the computation time and reduce the space. It saves space by employing fewer logic components and accelerates processing through the use of shortcut techniques. In addition, the multiplier's complexity and associated hardware costs can be decreased. To display overflow and underflow situations, the overflow and underflow flags are incorporated into the design. The study demonstrates the effective application of the Vedic multiplication method to multiples of two floating-point numbers. Less hardware is needed, which lowers the amount of energy used. Even though the power is significantly lowered, the delay is not greatly compromised. In terms of speed and area, the Urdhva Tiryakbhyam sutra is regarded as a promising technique. The application of such multipliers in arithmetic logical units, multiply accumulator unit designs, and comparison of the outcomes with already existing designs for the same are further ways to extend the work.

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