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Design of Dvr for Improvement of Voltage Profile Using Synchronous Reference Frame Based Control Strategy

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Abstract: *This work also includes development of a novel voltage control scheme that can compensate for voltage sag, swell, harmonics, and transient conditions in three-phase power systems. Faults occurring in power distribution systems or facilities in plants cause the voltage sag or swell. If a fault occurs, it can damage the power system or user's facility. For sensitive loads, even voltage sags of short duration can cause serious problems in the entire system. Normally, a voltage interruption triggers a protection device, which causes shutdown of the entire system. In order to mitigate power interruptions, this research proposes a scheme called "DYNAMIC VOLTAGE RESTORER (DVR)". The proposed scheme is able to quickly recognize the voltage sag, swell, harmonic and transient condition, and it can correct the voltage by either boosting the input voltage during voltage sag events or reducing the input voltage during voltage swell events. Among existing methods, the scheme based on the inverter system requires an inverter, a transformer, a liner control scheme. The proposed scheme can be applied at any voltage and provides cost and size advantages over existing methods.Simulations and experiments have been carried out to verify the validity of the proposed scheme.*

Keywords*: FACTS; DVR; Reactive Power; Compensation;*

I. Introduction

A power distribution system is a very complex system. It is important to remove any system faults or abnormalities so that the rest of the power distribution network is not interrupted or damaged. When a fault or an abnormality event occurs somewhere in a power distribution network, the voltage is affected throughout the power system. Among various power quality problems, the majority of events are associated with either voltage sag or a voltage swell, and they often cause serious power interruptions, if proper care will not be taken in time [1].DVR is a series-connected power electronic converter based mitigation device [2, 3] that is considered an effective custom power device for mitigating the impacts of upstream voltage disturbances on sensitive loads [4]. Although the main function of DVR is to mitigate the voltage sags and swells, sometimes, additional functions such as harmonic compensation and reactive power compensation are also integrated to the device [5, 6]. The basic operation of DVR is to inject a voltage of the required magnitude, phase angle and frequency in series with distribution feeder to maintain the desired amplitude and waveform for load voltage even when the voltage is unbalanced or distorted [7–10].

II. DVR (Dynamic Voltage Restorer)

Among the power quality problems (sags, swells, harmonics…) voltage sags are the most severe disturbances. In order to overcome these problems the concept of custom power devices is introduced recently. One of those devices is the Dynamic Voltage Restorer (DVR), which is the most efficient and effective modern custom power device used in power distribution networks. DVR is a recently proposed series connected solid state device that injects voltage into the system in order to regulate the load side voltage. It is normally installed in a distribution system between the supply and the critical load feeder at the point of common coupling (PCC). Other than voltage sags and swells compensation, DVR can also added other features like: line voltage harmonics compensation, reduction of transients in voltage and fault current limitations.

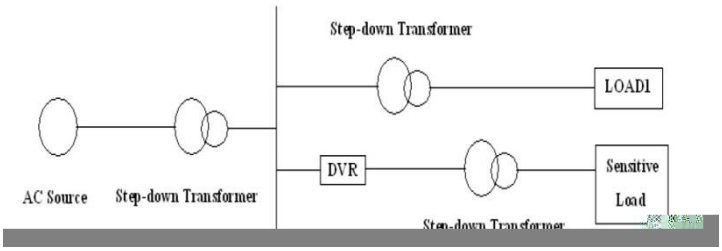

Fig.2.1 Location of DVR

Let us assume that the load current lags the load voltage. To draw a phasor diagram of the steady state operation, we assume that the load voltage is fixed at V per unit and the source voltage is allowed to vary. Since the primary target is to make the magnitudes of $V_l$and V, equal, the locus of desirable P's is the arc NB as shown in Fig. 2.3.

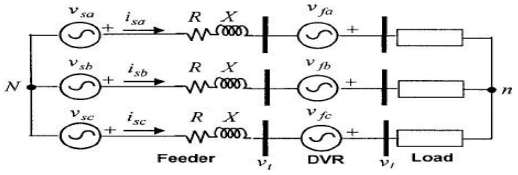

Fig. 2.3 Equivalent circuit diagram of DVR

To make the magnitude of the load voltage equal to that of the source voltage, the RIs drop must be less than NM. If the drop is less than this limiting value, the DVR must compensate the entire reactive drop in the feeder and provide additional injection such that the source voltage becomes V per unit. It can be seen from Fig. 2.4 that there are two possible intersection points with the arc – one at A and the other at B. This implies that two possible values of DVR voltage can be obtained for each feeder drop. For the first value, the source voltage will be along OA, while for the other value, it will along OB. It is needless to say that the best choice is the A intersection requiring much smaller voltage injection from the DVR.

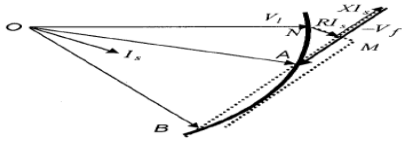

Fig. 2.4 Phasor Diagram Showing Multiple Solutions

We now connect a DVR aiming to regulate the load voltage to 1.0 per unit. Let us assume that the rms load voltage is given by 1.0 per unit. The line current is then

$$I_s = \frac{1\angle 0^\circ}{R_l + jX_l}$$

For zero DVR power, its voltage must be in quadrature to the line current. We then have

$$\vec{V}_f = \left|\vec{V}_f\right| e^{j\angle\left(\vec{I}_s + 90^\circ\right)} = \left|\vec{V}_f\right| \angle\Theta \qquad = \left|\vec{V}_f\right| (a_1 + jb_1) \tag{2.1}$$

where $a_l + jb_l$ is a unit phasor at 90" to I_S. Again from Fig. 1.3 we get

$$\vec{V}_s + \vec{V}_f = \vec{V}_l + (R + jX)\vec{I}_s = \vec{V}_l + a_2 + jb_2 \tag{2.2}$$

Where $a_2 + jb_2$ represents the feeder drop. Substituting (1) in (2) and rearranging we get.

$$\vec{V}_s = \vec{V}_l + a_2 + jb_2 - \left|\vec{V}_f\right|(a_1 + jb_1) \tag{2.3}$$

The following quadratic equation is then obtained from the from the magnitude condition of (2.3).

$$\left|\vec{V}_f\right|^2 - 2\left\{a_1\left(\left|\vec{V}_l\right| + a_2\right) + b_1 b_2\right\}\left|\vec{V}_f\right| = 0 \tag{2.4}$$

If Pin and P_{load} are the input power from the source and the load power respectively and similarly, if Q_{in} and Q_{load} are the input reactive power from the source and load reactive power respectively, then

$$P_{dvr} = P_{in} - P_{load} = 3 \cdot V_2 \cdot I \cdot \cos(\phi) - \sum_i V_{1i} \cdot I_i \cdot \cos(\phi - \alpha + \delta_i) \tag{2.5}$$

$$Q_{dvr} = Q_{in} - Q_{load} = 3 \cdot V_2 \cdot I \cdot \sin(\phi) - \sum_i V_{1i} \cdot I_i \cdot \sin(\phi - \alpha + \delta_i) \tag{2.6}$$

Where i=I,2,3. For minimum power operation and given ϕ, δ, α, V_1, and V_2 we have

$$\frac{dP_{dvr}}{d\alpha} = 0$$

Then

$$\sum_i V_{1i} \cdot I_i \cdot \sin(\phi - \alpha + \delta_i) = 0$$

If $P_{dvr} > 0$, then

$$\alpha_{opt} = \phi + \beta$$

Where $\beta = \arctan\frac{Y}{X}$

$$X = \sum_i V_{1i} \cdot \cos(\delta_i), Y = \sum_i V_{1i} \cdot \sin(\delta_i)$$

Else if $P_{dvr} = 0$, then

$$\alpha_{opt} = \phi + \beta - \arccos\left(\frac{3 \cdot V_2 \cdot \cos(\phi)}{\sqrt{X^2 + Y^2}}\right) \quad (2.7)$$

III. Control Algorithm

The basic functions of a controller in a DVR arethe detection of voltage sag/swell, distortion, harmonic events in thesystem; computation of the correcting voltage,generation of trigger pulses to the sinusoidalPWM based DC-AC inverter, correction of anyanomalies in the series voltage injection andtermination of the trigger pulses when the eventhas passed. The controller may also be used toshift the DC-AC inverter into rectifier mode tocharge the capacitors in the DC energy link in theabsence of voltage sags/swells.The d-q-o transformation or Park's transformationis used to control of DVR.

The dqo method gives the sag depth and phaseshift information with start and end times. Thequantities are expressed as the instantaneousspace vectors. Firstly convert the voltage from a-b-c reference frame to d-q-o reference. Forsimplicity zero phase sequence components isignored.Figure 3.1 illustrates a flow chart of the feedforward d-q-o transformation for voltagesags/swells detection. The detection is carried outin each of the three phases.

The control scheme for the proposed system isbased on the comparison of a voltage referenceand the measured terminal voltage(Va,Vb,Vc).The voltage sags is detected when the supply drops below the reference valuewhereas voltage swells is detected when supplyvoltage increases up to 25% of the referencevalue. The error signal is used as a modulationsignal that allows to generate a commutationpattern for the power switches (IGBT's)constituting the voltage source converter. Thecommutation pattern is generated by means of thesinusoidal pulse width modulation technique(SPWM); voltages are controlled through themodulation.The block diagram of the phase locked loop(PLL) is illustrated in Figure 4. The PLL circuit isused to generate a unit sinusoidal wave in phasewith mains voltage.

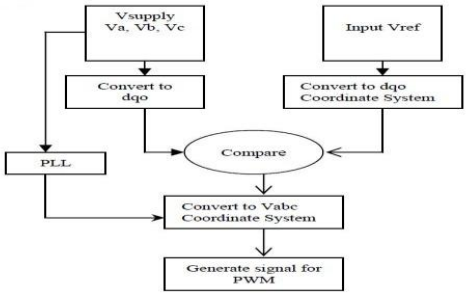

Fig. 3.1Flow chart of feed forward controltechnique for DVR based on dqo transformation

IV. Modeling & Simulation of DVR

The model consists of generating source of 13 kv, which is stepped up to 132kv. This power has to transmit over two 100 k.m transmission lines, Again the power has to be distribute over two distribution line length of 30 k.m and 20 k.m. On the 10 k.V distribution line faults have created, to measure the performance. The detail model is shown in Figure 4.1.

4.1 System Parameters and Constant values

A detailed system as shown in Figure 3 has beenmodeled by **MATLAB/SIMULINK** to study the efficiency of suggested control strategy. The system parameters and constant value are listed in Table 1.It is assumed that the voltage magnitude of the load bus is maintained at 1 puduring the voltage sags/swells condition. The results of the most important simulations are represented in Figures 5-8. The load has been assumed linear with power factor pf =0.85lagging and its capacity of 10 KVA. Detail has been shown in table-1

Table-1

System parameters

Main supply Voltage	13kv
Step-up transformer for feeder	13kv/ 132kv
3-phase transmission line-1	100 k.m Line
3-phase transmission line-2	100 k.m Line
Step-down transformer for line-1	132kv / 10 kv

Step down transformer for line-2	132 kv / 11 k.v
Distribution line-1	30 k.m Line
Distribution line-2	20 k.m Line
Load on distribution line-1	10 KW , pf= .9 lag
Load on distribution line-2	10 K.W Load, PF= .85 lag
Series Injection Transformer	0.5 kv / 0.5 kv
DC Supply for Inverter	500v
Universal Bridge	3 arm, 6-pulse IGBT Inverter

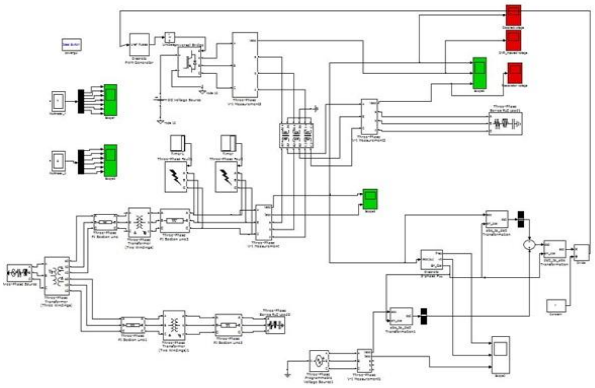

Fig.4.1 MATLAB Model

4.2 Single Line-Ground Fault

The first simulation show of single phase voltage sag is simulated. The simulation started with the supply voltage 100% sagging as shown in Figure5.1 (a). In Figure 5.1 (a) also shows a 100% voltage sag initiated at 0.1s and it is kept until 0.15s, withtotal voltage sag duration of 0.05s. Figures 5.1 (b)and (c) show the voltage injected by the DVR andthe corresponding load voltage withcompensation. As a result of DVR, the loadvoltage is kept at 1 pu. It is also seen from the figure that the voltage wave form contains high transients & high distortions with harmonics. Here the Dynamic Voltage Restorer is not only able to compensate the voltage sag & swell but also able to compensate the harmonics and transients presents in the voltage wave form.

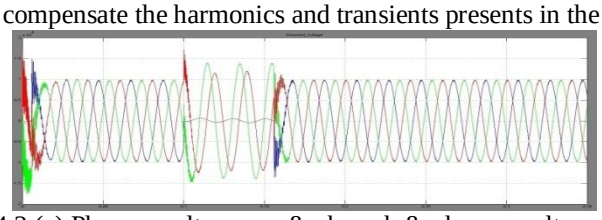

Fig. 4.2 (a) Phase-a voltage sag & phase-b & phase-c voltage swell

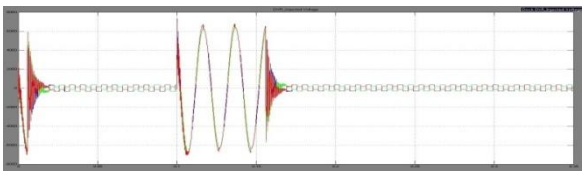

Fig. 4.2 (b) DVR injected voltage

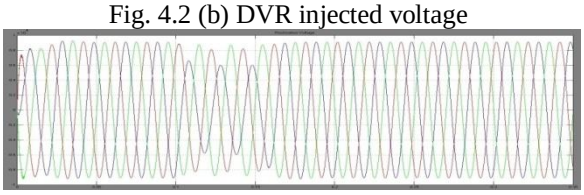

Fig. 4.2 (c) Load voltage

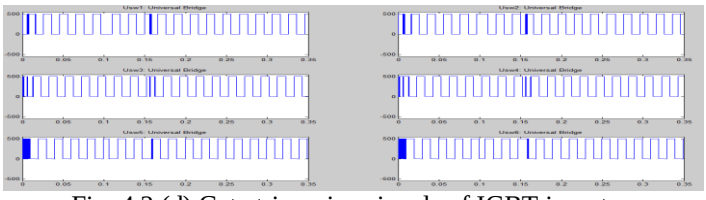

Fig. 4.2 (d) Gate triggering signals of IGBT inverter

4.3 Two Single Line-Ground Faults

For two Single Line-Ground fault the phase A-Ground fault created from 0.1s to 0.15s and phase B-Ground fault created from 0.2s to 0.25s.

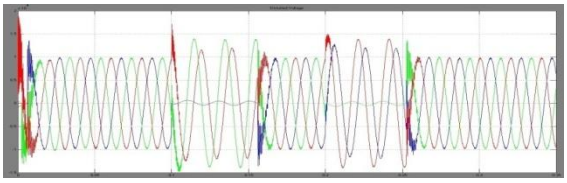

Fig. 4.3 (a) Phase-a to ground and phase-b to ground at different time intervals

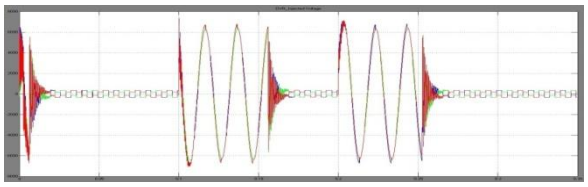

Fig. 4.3 (b) DVR injected voltage

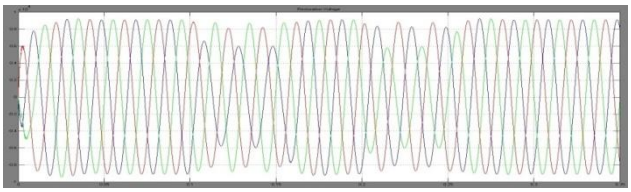

Fig. 4.3 (c) Load voltage

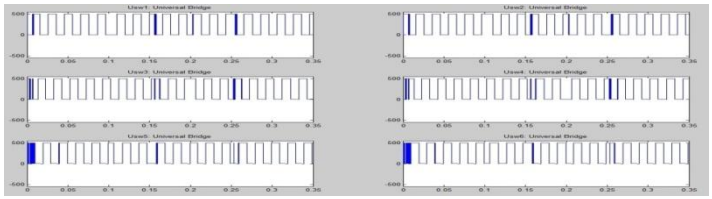

Fig. 4.3 (d) Gate triggering signals of IGBT inverter

4.4 Double Line-Ground Fault

The double line-ground fault created from 0.2s to 0.25s, i.e. Phase-a to Phase-b. So that there is 100% sag in phase-a and phase-b and swell in phase-c. this sag and swell conditions well compensated by the DVR.

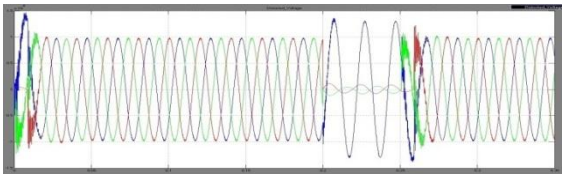

Fig. 4.4 (a) Phase-a & phase-b to ground fault & voltage swell in phase-c

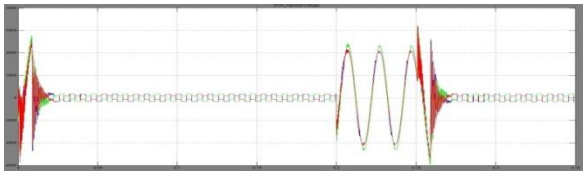

Fig. 4.4 (b) DVR injected voltage

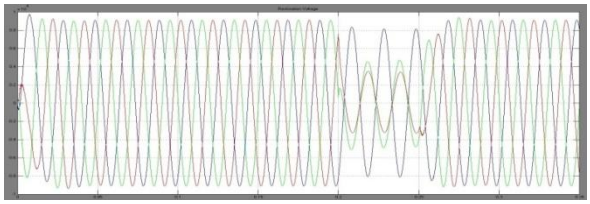

Fig. 4.4 (c) Load voltage

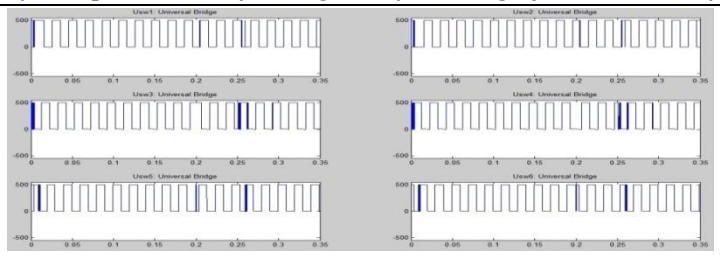

Fig. 4.4 (d) Gate triggering signals of IGBT inverter

4.5 L-G, LL-G, LLL-G Faults at various time intervals

A phase-a to ground fault created from 0.1s to 0.15s, so that there is sag in phase-a and swells in phase-b and phase-c. Another LL-G Fault, i.e. phase-a and phase-b to ground fault has created from 0.2s to 0.25s, so that there is sag in the two phase-a and phase-b, and swell in phase-c. Again LLL-G fault has been created from 0.3s to 0.35s so that there is complete sag in all three phases. Particularly this test was to see the robustness of DVR.

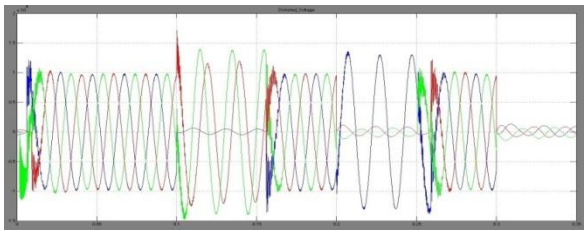

Fig. 4.5 (a) L-G, LL-G, LLL-G Faults at various time intervals

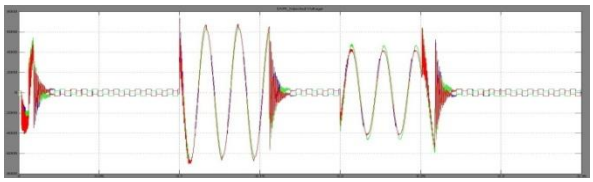

Fig. 4.5 (b) DVR injected voltage

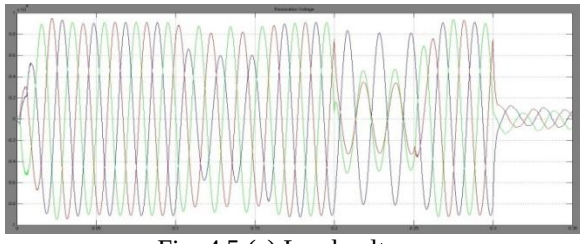

Fig. 4.5 (c) Load voltage

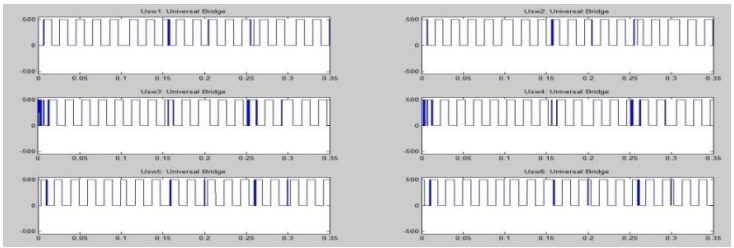

Fig. 4.5 (d) Gate triggering signals of IGBT inverter

V. Conclusion

The simulations have been done to show that the proposed voltage sag and swell supporter scheme regulates the output voltage with quick reaction and high precision during voltage sag and swell events. Also we can see that the harmonic and transient content in the load voltage has been reduced. We have presented a simple control algorithm i.e., Synchronous reference base control strategy, which is very simple and cost effective to implement.

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