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Analysis Design and Implementation of Snubber Less Current-Fed Bidirectional Full Bridge Dc-Dc Converter

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Abstract: *Novel Soft-Switching Bidirectional Snubberless Current-fed full-bridge voltage doublers. A novel secondary modulation technique is proposed to clamp the voltage across the Primary side switches naturally with Zero Current Commutation (ZCC). It eliminates the necessity for active-clamping or passive snubber to absorb the switch turn-off voltage. A major challenge in current fed converters, Zero-Current Switching (ZCS) of primary side devices and Zero-Voltage Switching (ZVS) of Secondary side devices are achieved, which significantly reduce switching losses. Primary device voltage is clamped at low voltage, which enables the use of low voltage devices with low on-state resistance. Soft-switching and voltage-clamping is inherent and load independent.*

Keywords: *DC-DC converter; Zero Current Commutation (ZCC), Zero-Current Switching (ZCS), Zero-Voltage Switching (ZVS)*

I. Introduction

Soft switching bidirectional snubber less current-fed full-bridge DC-AC-DC voltage source. The proposed design dc–dc converter presents the following features: low number of active devices compared to the converters usually applied to reduce switching losses, DC - DC converter is essential equipment in the system of DC load which has a function as step up and step down voltage. A dc-to-dc converter is required electrical couple to the system dc load. Dual active bridge DC-DC converters are mainly used for renewable energy applications. In the full bridge DC-AC-DC converter which allows energy transfer between the source and the load [1-2]. The performance of the converter will be analyzed by comparing various modulation strategies like phase shift, triangular and trapezoidal methods [3-4]. A high frequency transformer is used as isolation in DC-DC full bride converter. Various modulation strategies have been discussed for the dual active bridge DC-DC converter [5-6]. The performance parameters have been analyzed in terms of output voltage ripple and switching losses. A suitable high frequency transformer is designed. Simulation studies have been carried out using POWERSIM to verify the results.

The phenomenon of resonant reset in forward converter possesses several advantages over various reset schemes such as:

- Simple and low cost
- Magnetizing and leakage energy is fully recycled
- Easy to extend maximum duty cycle
- Widely used in wide input range

Compared to voltage-fed converters, current-fed converters have lower input current ripple, lower HF transformer turns ratio, negligible diode ringing, and easier current control ability [7-8]. Therefore, current-fed converters are meritorious for low voltage and high current application. The major limitations of current-fed converters are hard switching and snubber requirements to absorb the switch turn-off voltage spike [9].

A dual half-bridge bidirectional dc/dc converter is proposed to minimize the number of switching devices [10]. This topology requires four split capacitors to handle full-load current and occupy a considerable volume of the converter. It may need an additional control to avoid the possibility of voltage imbalance across the capacitors. Also, the topology is not modular in nature and so not easily scalable for higher power [11]. Peak current through the primary switches are > 2.5x the input current and top and bottom switches share unequal currents. In this paper, a novel secondary modulation based soft- switching bidirectional snubberless current-fed full-bridge voltage doublers is proposed as shown in Fig. 2. Voltage doublers or half-bridge is selected to reduce number of switches.

II. Specifications

This converter is designed for the following specifications:

- Input voltage range : 10 V to 12V
- No of outputs : 2 outputs
- Primary Output-I : 40v
- Secondary Output-II : 90v
- Output voltage : 180v
- Topology : Full bridge
- Operating frequency : 100KHZ

III. Block Diagram and Description

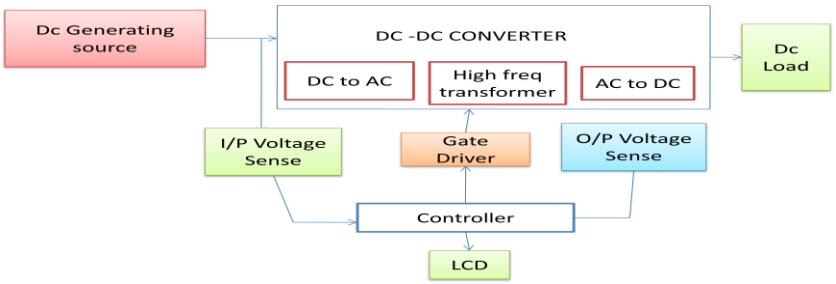

Figure 1. Block Diagram

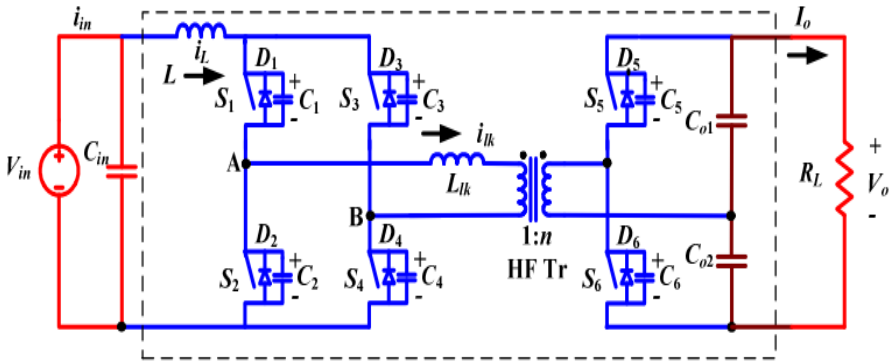

Figure 2. Snubberless bidirectional full-bridge DC-DC converter

Steady-state operation and analysis with zero current commutation (ZCC) and natural voltage clamping (NVC) concept has been explained. Before turning-off of a diagonal switch pair (S1-S4 or S2 -S3) at primary side, the other pair of primary side switches is turned on. The reflected output voltage Vo/2n appears across the transformer primary. It diverts the current from one switch pair to the other pair through transformer causing current through just triggered switch pair to rise and the current through conducting switch pair to fall to zero naturally resulting in ZCC. Later the body diodes across switch pair start conducting and their gating signals are removed leading to ZCS turn-off of devices. Then the device voltage rises and clamped at reflected output voltage.

The proposed converter offers the following merits:

1) Switching losses are reduced significantly owing to ZCS of primary switches and ZVS of secondary switches. It permits high switching frequency operation to realize a compact and high power density system.

2) Voltage across primary devices is independent of duty cycle with varying input voltage and output power and naturally clamped. It avoids the need of passive snubber or active-clamping circuit making it snubberless and enables the use of semiconductor devices of low voltage rating.

IV. Switching Operation

For the simplicity of study of operation and analysis, the following assumptions are made for the operation and analysis of the converter: a) Boost inductor L is large enough to keep constant current. b) All components are assumed ideal. c) Series inductor L includes the leakage inductance of the HF transformer. With appropriate design of the HF transformer, external series inductor could be avoided d) Magnetizing inductance is infinitely large negative. This net 4 volts for 10 µsec drives the mag amp core out of saturation and resets it by an amount equal to 40V-µsec. The primary switches pairs S1-S4 and S2 -S3 are

operated with identical gating signals phase shifted with each other by 180o.The duty cycle is kept higher than 50%. The operation during different intervals in a one half cycle is explained with equivalent circuits shown in Fig. 4.

Interval 1 (Fig. 4a; t o < t < t 1): In this interval, primary side H-bridge switches S2 and S3 and anti-parallel body diode D6 of secondary side switches are conducting. The current through series inductor L is negative and constant. Power is fed to the load through HF transformer.

Interval 2 (Fig.4b; t 1 < t < t 2): At t = t1 , primary switches S1 and S4 are turned on. The corresponding snubber capacitors C1 and C4 discharge in a very short period.

Interval 3 (Fig.4c; t2 < t < t 3): Now all four primary switches are conducting. Reflected output voltage Vo/2n appears across series inductor (leakage inductor) L and diverts the current through switches S2 and S3 into switches S1 and S4 .Therefore, Primary current I starts increasing linearly. It causes currents through previously conducting devices S2 and S3 to reduce linearly while switches S1 and S4 start conducting with zero current which helps reducing associated turn-on loss. The currents through various components are given by

$$i_{lk} = -I_{in} + \frac{V_o}{2n \cdot L_{lk}} \cdot (t - t_2) \quad (1)$$

$$i_{S1} = i_{S4} = \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_2) \quad (2)$$

$$i_{S2} = i_{S3} = I_{in} - \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_2) \quad (3)$$

$$i_{D6} = \frac{I_{in}}{n} - \frac{V_o}{2n^2 \cdot L_{lk}} \cdot (t - t_2) \quad (4)$$

Interval 4 (Fig.4d; t 3<t<t4): In this interval, secondary side device S 6 is turned on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, the primary devices S2 and S3 commutate naturally and their respective currents iS2 andiS3 reach zero.

Interval 5 (Fig.4e; t4<t <t 5): In this interval, the primary or series inductor current ilk increases further with the same slope and anti-parallel body diodes D2 and D3 start conducting causing extended zero voltage to appear across the outgoing or commutated switches S 2 and S 3 to ensure ZCS turn off. Now, the secondary device S6 is turned-off. At the end of this interval, currents through transformer, switches S1 and S4 reach their peak value. This interval should be short to limit the peak current though the components reducing the current stress and kVA ratings.

The currents through operating components are given by

Interval 6 (Fig. 4f; t 5 < t < t 6): During this interval, switches S 2 , S 3 and S6 are turned off. Anti-parallel body diode of switches S 5 takes over the current immediately. Therefore the voltage across the transformer primary reverses polarity and the current through it starts decreasing. The currents through the switches S 1 and S 4 and body diodes D 2 and D 3 also start decreasing.

Interval 7 (Fig. 4g; t 6 < t < t 7): In this interval, snubber capacitors C 2 and C 3 charge to V o /2n. Switches S 2 and S 3 gain forward blocking mode.

Interval 8 (Fig. 4h; t 7 < t < t 8): In this interval, currents through S1 and S4 , and transformer are constant at input current I in and current through anti-parallel body diode of the secondary switch D 5 is I in /n.

The final values are: iS1= iS4 =I in, iS2 = iS3 =0, ilk =I in , iD5= I in /n.

Voltage across the switches S 2 and S 3 V S2 =V S3 = Vo/2n.

The currents through operating components are given by

$$i_{lk} = I_{in} + \frac{V_o}{2n \cdot L_{lk}} \cdot (t - t_4) \quad (5)$$

$$i_{S1} = i_{S4} = I_{in} + \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_4) \quad (6)$$

$$i_{D2} = i_{D3} = \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_4) \quad (7)$$

$$i_{S6} = \frac{I_{in}}{n} + \frac{V_o}{2n^2 \cdot L_{lk}} \cdot (t - t_4) \quad (8)$$

$$i_{lk} = I_{lk,peak} - \frac{V_o}{2n \cdot L_{lk}} \cdot (t - t_5) \quad (9)$$

$$i_{S1} = i_{S4} = I_{sw,peak} - \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_5) \quad (10)$$

$$i_{D2} = i_{D3} = I_{D2,peak} - \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_5) \quad (11)$$

$$i_{D5} = \frac{I_{lk,peak}}{n} - \frac{V_o}{2n^2 \cdot L_{lk}} \cdot (t - t_5) \quad (12)$$

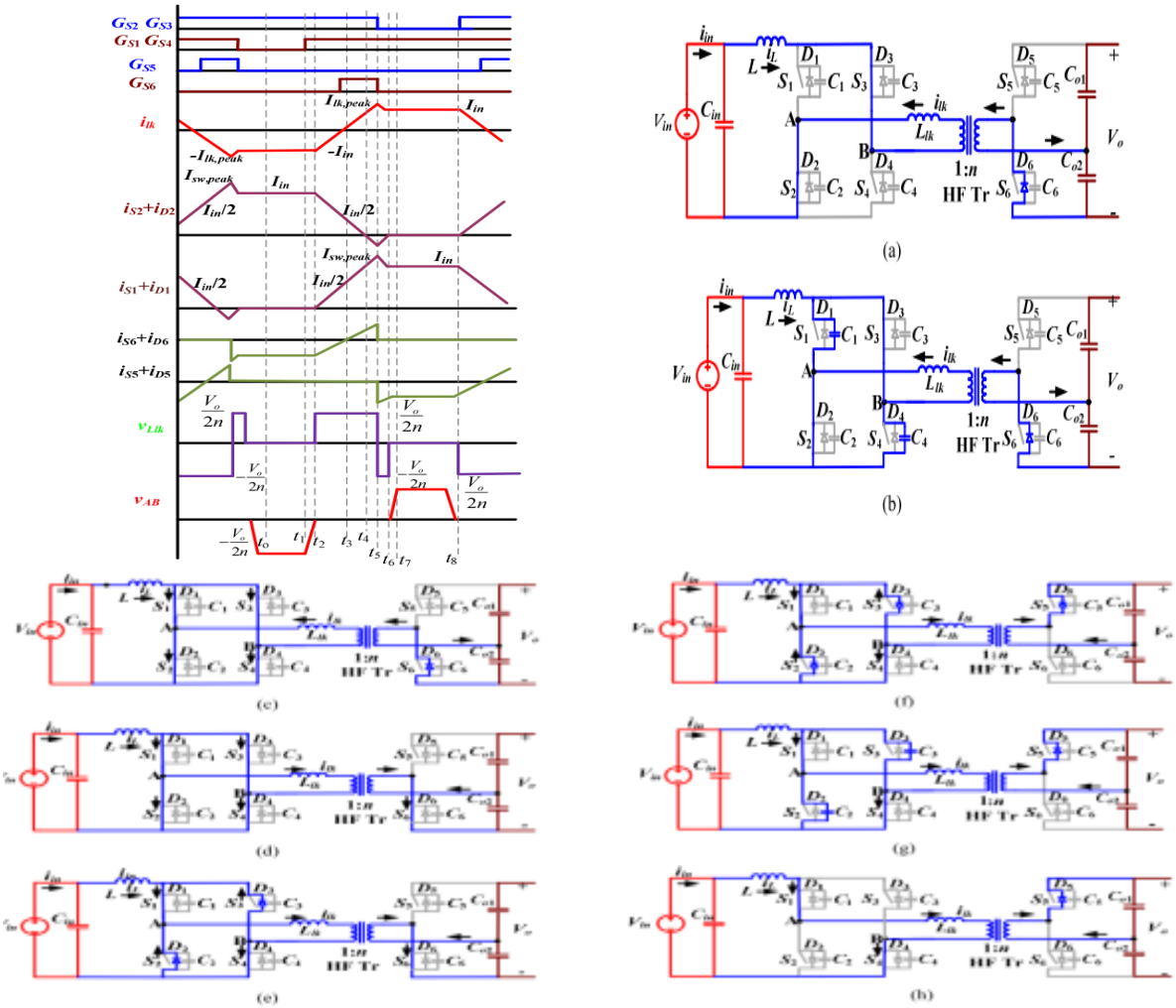

FIGURE 3 OPERATING WVEFORM

Figure 4(a-h) Equivalent circuits during different intervals of the operation of the proposed converter for the steady-state operating waveforms

V. DESIGN PROCEDURE

Design example considering the following specifications:

Po = 250W, V in=12 V, V o = 150 ~ 300V, f s =100 kHz

The design equations are presented to determine or calculate the components' rating.

(1) Average input current is I in=Po/(η Vin). Assuming an Ideal efficiency η of 95%, Iin = 21.9 A.

(2) Maximum voltage across the primary switches is

$$V_{P,SW} = \frac{V_o}{2 \cdot n} \qquad (13)$$

$$V_o = \frac{n \cdot V_{in}}{1-d} \qquad (14)$$

Where d is the duty cycle of primary switches. Equation (14) is derived assuming body diode conducts for (interval 6) quite short time just to ensure ZCS of primary switches without significantly increasing the peak current. However, at light load, the diode conduction time is relatively large and (14) is not valid any more. Due to the existence of longer body diode conduction period, the output voltage is boosted to higher value than that of nominal boost converter.

$$V_o = \frac{n \cdot V_{in}}{(1-d-d')} \qquad (15)$$

Where d' is given by,

$$d' = d - 0.5 - \frac{4 \cdot n \cdot I_{in} \cdot L_{lk\_T} \cdot f_s}{2 \cdot V_o} \qquad (16)$$

(4) Series inductance L is calculated using

$$L_{lk} = \frac{V_o \cdot (d - 0.5)}{4 \cdot n \cdot I_{in} \cdot f_s} \qquad (17)$$

(5) The current and voltage stress of major components are given in Table I.

Components	Current Stress			Voltage Stress
	Peak Current	Average Current	RMS Current	Peak voltage
Primary Switches $S_1 \sim S_4$	I_{in}	$I_{P,av} = \frac{I_{in}}{2}$	$I_{P,rms} = I_{in}\sqrt{\frac{2-d}{3}}$	$V_o/2n$
Secondary Switches $S_5 \sim S_6$	I_{in}/n	$I_{S,av} = \frac{P_o}{2 \cdot V_o}$	$I_{S,rms} = \frac{I_{in}}{2n}\sqrt{\frac{2d-1}{3}}$	V_o
Secondary Switches Body Diodes $D_5 \sim D_6$	I_{in}/n	$I_{D,av} = \frac{I_{in} \cdot (7-6d)}{8n}$	$I_{D,rms} = \frac{I_{in}}{2n}\sqrt{\frac{11-10d}{3}}$	V_o
HF transformer	VA rating : $VA_{x-mer} = \frac{V_o \cdot I_{in}}{2n}\sqrt{\frac{2 \cdot (5-4d) \cdot (1-d)}{3}}$			

TABLE I.CURRENT AND VOLTAGE STRESS OF MAJOR COMPONENTS

(6) The output power can be derived as

$$P = \frac{4n \cdot v_{in}^{\ 2} - v_o \cdot v_{in} \cdot (3 - 4 \cdot d)}{16 \cdot n \cdot L_{lk} \cdot f_s} \qquad (18)$$

Transformer turns ratio is selected based on conduction losses, which mainly consist of the conduction losses in the primary switches because they carry higher currents. Increasing the turns ratio may reduce the maximum voltage across the primary switches allowing low voltage switches with low on-state resistance (from (13)). But, higher turns ratio yields higher switch rms current. Voltage regulation over varying input voltage is another concern. An optimum turns ratio n = 5 and duty ratio d= 0.8 are selected to achieve low overall conduction losses. Output voltage can be regulated from 150V to 300V by modulating the duty ratio.

(7) Value of boost inductor is given by

$$L = \frac{V_{in} \cdot (d - 0.5)}{\Delta I_{in} \cdot f_s} \qquad (19)$$

Where ΔIin is the boost inductor ripple current. For ΔI = 1 A, L = 36 μH.

(8) VA rating of each HF transformer is given by

$$VA_{x-mer} = \frac{V_o \cdot I_{in}}{2n}\sqrt{\frac{2 \cdot (5-4d) \cdot (1-d)}{3}} \qquad (20)$$

Transformer Design:

Transformer is designed by calculating the Area Product (Ap) and by selecting the suitable core by using the following formula.

$$A_P = \frac{\left(\sqrt{D_{max}} \times P_{OUT} \times \left(1 + \frac{1}{Eff}\right)\right)}{K_W \times J \times 10^{-6} \times B_M \times f_{SW}} \qquad (21)$$

An appropriate core will be selected which must have area product greater than the calculated Ap. Area product (Ap) is given as the product of the core cross section (Ac) and the window area (Aw).

Proposed Converter is designed for maximum duty cycle 65% and efficiency of 75%.

Selected Torpid Core: OR42213UG.

Now, Primary number of turns (N_P) is calculated by using

$$N_P = \frac{V_{IN(min)} \times D_{max}}{B_m \times A_c \times 10^{-6} \times f_{SW}} \qquad (22)$$

Turns ratio is given as (3)

$$T_{RATIO} = \frac{N_S}{N_P} = \frac{\left(V_{OUT} + (V_D \times D_{max})\right)}{D_{max} \times V_{IN(min)}} \qquad (23)$$

Number of turns on secondary is calculated by using,

$$Ns = Tratio \times Np \qquad (24)$$

Mosfet Selection :

MOSFET is selected based on the maximum voltage stress when switch is turned-off.
Selected core: IRFP540N, 200V, R_{DS}=0.04E, 50A

VI. Experimental Results:

The proposed work of the converter has been simulated in PSIM Version 9.3.2.100 and later planed to develop the prototype of 100V and tested .The specification of the prototype are the same with the Design Simulation done with full bridge converter from 12v dc to 42v peak to peak with frequency 10 MHz given to the primary side transformer and the 92v peak to peak Secondary to the transformer. The voltages across output capacitors Co 1, Co2 and the total output voltage 90V. It can be seen that voltage across Co1 and Co2 are equal and balanced.

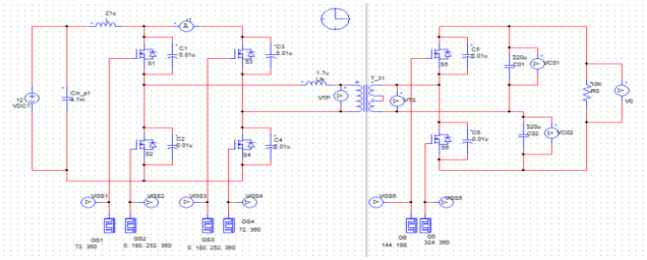

Figure 1

WAVEFORMS:

Output Voltage Gate Signal Vgs1 and Vgs2

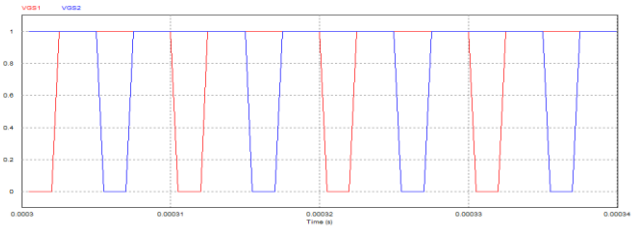

Figure 2

Output Voltage gate Signal Vgs3 and vgs4:

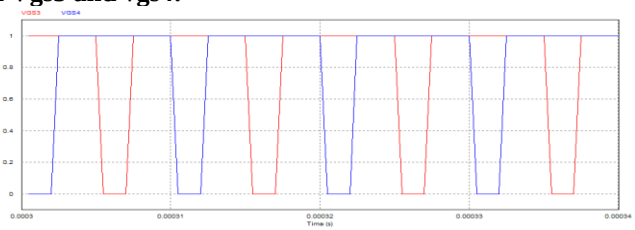

Figure 3

Output voltage Gate signal Vgs5 and Vgs6:

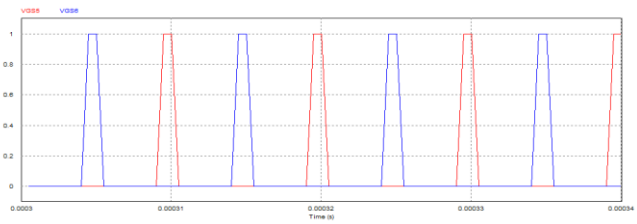

Figure 4

Final Simulation Result

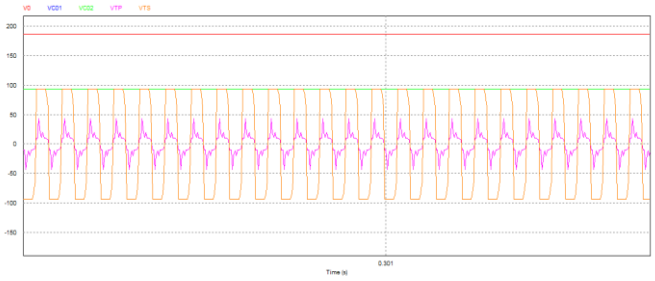

Figure 5

Hardware and experimental result:

The hardware implementation of proposed converter is shown in Fig.8.2. In proposed converter all subsystems such as transformer, Mosfet switch, and capacitor and controller part are implemented.

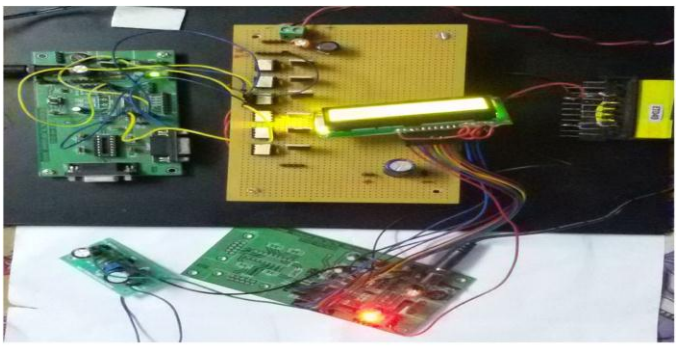

Figure 6

1. Pulse Generation for switch S1, S2, S3, S4

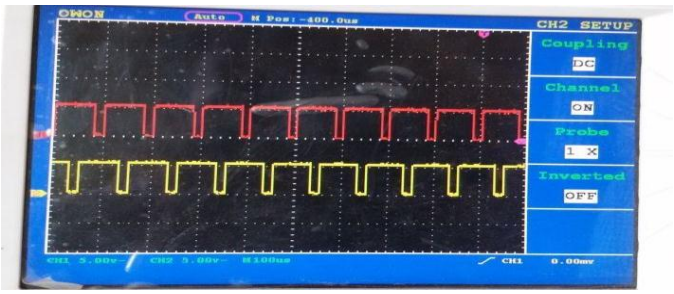

Figure 7

2 Pulse Generation for switch S5, S6

Figure 8

Converter in Operating Condition

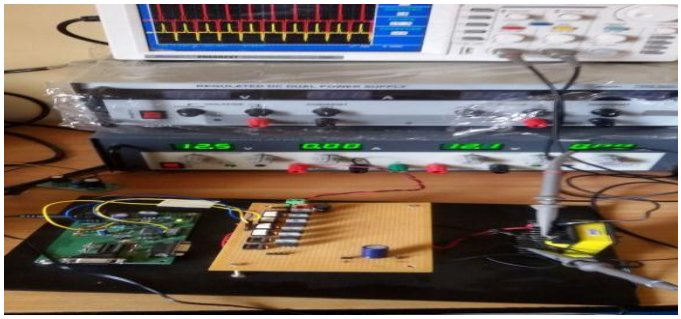

Figure 9

Final Hardware Result for Primary and secondary

Figure 10

VII. Conclusion

Novel soft-switching bi-directional current-fed full-bridge isolated voltage doublers are proposed. Steady-state operation, analysis, and design are illustrated. Experimental results clearly demonstrate that the proposed converter maintains ZCS of primary devices and ZVS of secondary devices over wide variation of output power. Proposed modulation technique clamps the voltage across the primary side devices naturally with ZCC and therefore eliminates the necessity for active-clamp or passive snubber required to absorb device turn-off voltage spike. Soft-switching and voltage clamping is inherent and is maintained independent of load Usage of low voltage devices leads to low conduction losses in primary devices, which is significant due to higher currents on primary side. The converter is suitable for higher boost ratio and higher current applications, i.e., interfacing low voltage to higher voltage dc bus with higher current such as fuel cell vehicles.

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